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The IR1175: A Novel Integrated Controller For Synchronous Rectifiers Boosts Supply Efficiency

by Edgar Abdoulin , International Rectifier Corporation
233 Kansas St. El Segundo, California 90245

ABSTRACT

This paper discusses a novel method for controlling power MOSFETs used as synchronous rectifiers in isolated DC/DC converters with fixed frequency. An integrated controller (IR1175) that has been designed and tested employing the techniques is also presented. Finally, comparisons are made between the self-driven (cross-coupled) method of driving synchronous rectifiers and the novel controller showing efficiency improvements resulting from its use in actual applications.

1 .INTRODUCTION

The advantages of using power MOSFETs as synchronous rectifiers in DC/DC converters with isolated buck topology derivatives are well known. Power MOSFETs result in higher efficiency systems due to lower losses offered by their on-resistance. The recent trends towards lower output voltages and higher currents have made the power MOSFET a highly desirable option for rectification in the secondary side. For power MOSFETs to operate properly in these topologies, an appropriate gate drive is necessary. By far, the most widely used method for generating the gate drive is the cross-coupled (CC) or self-driven scheme (Fig. 1). In this method the transformer secondary is used to drive the gates through appropriate gate resistors. The method, although simple and functional, does have some drawbacks:

- **Disappearing gate drives:** In topologies with core reset mechanisms employing a third winding and no additional provisions, the gate drive disappears after the core is reset, turning off the MOSFET. This causes the output current to flow through the body drain diode of the MOSFET. Since this diode has a forward voltage drop far greater than MOSFET itself, it results in higher losses and lower system efficiencies. One solution is to parallel lower forward drop diodes (e.g. Schottkys) with the MOSFET to reduce losses.
- **Finite MOSFET switching times:** This poses a problem during transformer transitions. Due to finite MOSFET switching times, the body drain diodes conduct the output current for a brief period until the MOSFETs are turned on. The loss of efficiency is most noticeable at high frequencies since the fixed switching times constitute a larger portion of the duty cycle.
- **Effects of stray inductance in secondary side:** This inductance associated with the MOSFET and the transformer poses a unique problem for effective control of the synchronous rectifiers. The effect of the stray inductance is to maintain the current in the branch even if the MOSFETs have zero turn-on/off times. This also results in body diode conduction until the current dissipates.
- **Appropriate gate drive levels**: With the Self driven topology, the gate drives levels are essentially, replications of the transformer output. In certain applications, these outputs might not be appropriate to drive power MOSFETs as is, more often requiring additional and sometimes elaborate circuitry to generate the proper gate drives.

The new methodology described herein attempts to rectify the drawbacks associated with the self-driven method, resulting in higher efficiency systems.

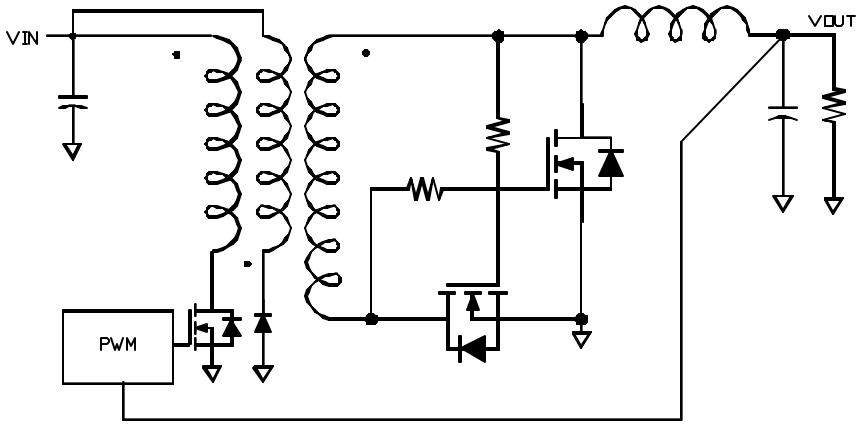


Fig 1 - Single Ended Forward Converter with self driven synchronous rectifiers.

2 . DESCRIPTION OF THE NEW CONTROL METHOD

In summary, the new method offers the following characteristics:

- Compensates for finite MOSFET switching times so they switch on with the actual transition of the transformer rather than later (Pre-firing)
- Minimizes effects of stray inductance in the secondary side by providing necessary dead times/overlap between gate drives.
- Maintains a steady gate drive throughout both power transfer and reset cycles, regardless of transformer output status.
- Generates gate drives that are compatible with logic level power MOSFETs independent of transformer output levels.
- Follows the transitions of the transformer and maintains the duty cycle requirements set by the system PWM controller.
- Is transparent to the system PWM controller under normal and transient conditions.
- Is a stand-alone circuit with no ties to the primary.

2.1 - COMPENSATING FOR MOSFET SWITCHING TIMES

The compensation is accomplished by providing gate drives that lead the transformer transitions in a controllable manner. The gate drives are generated by using modified Phase Locked Loops (PLLs). Fig. 2 depicts a conventional and the modified PLL. In a conventional PLL, the phase comparator ensures that the signals present at its inputs are in phase by providing necessary error signals to drive the VCO. This results in a VCO output that is in phase with the input signal. This modified PLL employs a delay block in the feedback

path of the VCO to the phase comparator. The phase comparator forces its two inputs to be in phase , consequently providing an error signal to the VCO which compensates for the delay block, resulting in a signal that leads the input in phase. Moreover, the lead time can be adjusted by simple adjustments of the delay block. The amount of lead time required depends on the type of MOSFET used and to a lesser degree, on output current range.

2.2 - MINIMIZING SECONDARY SIDE STRAY INDUCTANCE EFFECTS

The effect of stray inductance is to maintain current flow in the output branches even after the transformer reverses. This current flow is maintained regardless of the status of the power MOSFET and can cause unnecessary losses in the body diodes. Fig 3 shows the body diode current resulting in a control system with a dead time between the gate drives. When the device turns off, the stray inductance will force the current through the body diode. Current will ramp down in one branch while ramping up in the other. By maintaining both devices on at the same time for a short period (i.e. overlapped gate drives) the currents are allowed to dissipate through the MOSFET rather than the body diode reducing losses. It is important to note that an excessive overlap beyond the requirement to dissipate the currents in the stray inductance will present a short across the transformer that will result in a loss of efficiency due to unwanted current spikes. Employing proper design practices to minimize secondary stray inductance will reduce the required gate drive overlap and eliminate current spikes in the transformer.

2.3 - CONTROLLER BLOCK DIAGRAM

Fig 4 shows a block diagram of the control circuit. The transformer outputs (X1 and X2) are squared and detected in the input block. A double pulse suppression circuit ensures only one pulse per transition. The rising edge of X1 and X2 are used to synchronize with the input signals. The PLLs generate two 50% duty cycle pulse trains that lead the inputs by an externally preset amount. The S/R latch is used to recombine the leading waveforms to generate the gate drive signals while maintaining duty cycle information. The final blocks are used to adjust the dead-time/overlap and provide necessary drive to the power MOSFETs.

2.4 - TRANSIENT CONTROL

Transients due to line or load changes cause the primary PWM controller to react by adjusting the duty cycle to compensate for the changes and maintain a steady output voltage. Slow transients can adequately be accounted for by the Phase lock loops employing a suitable loop filter e.g., with a natural frequency set to ~1/10 of the switching frequency. Ultra fast transients are primarily the domain of the output capacitors. With mid level transients, there is a possibility of the phase locked loops to lose track of the incoming signal for a short period of time. During this period it is important to maintain a proper gate drive to avoid the possibility of shorting the transformer outputs. The transient control block in Fig 4 detects an unlocked condition and changes the gate drive source for the MOSFETs to the squared pulses obtained from the input block (No lead time - similar to self driven). This condition is probed on a cycle-by-cycle basis until both PLLs are again locked. Having detected a successful lock, the transient response block reverts the gate drives to the PLL outputs on the next cycle.

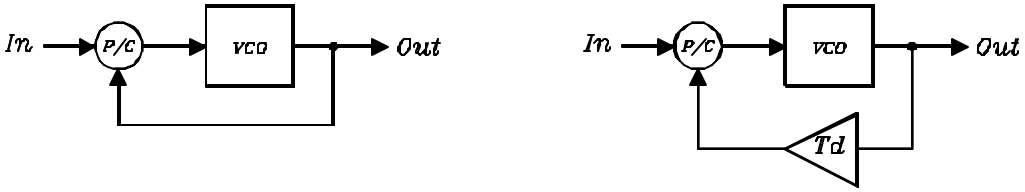


Fig 2 - Conventional Phase Locked Loop has Vco output fed back to the phase comparator. Modified PLL has adjustable delay block in feedback path forcing Vco output to lead input signal.

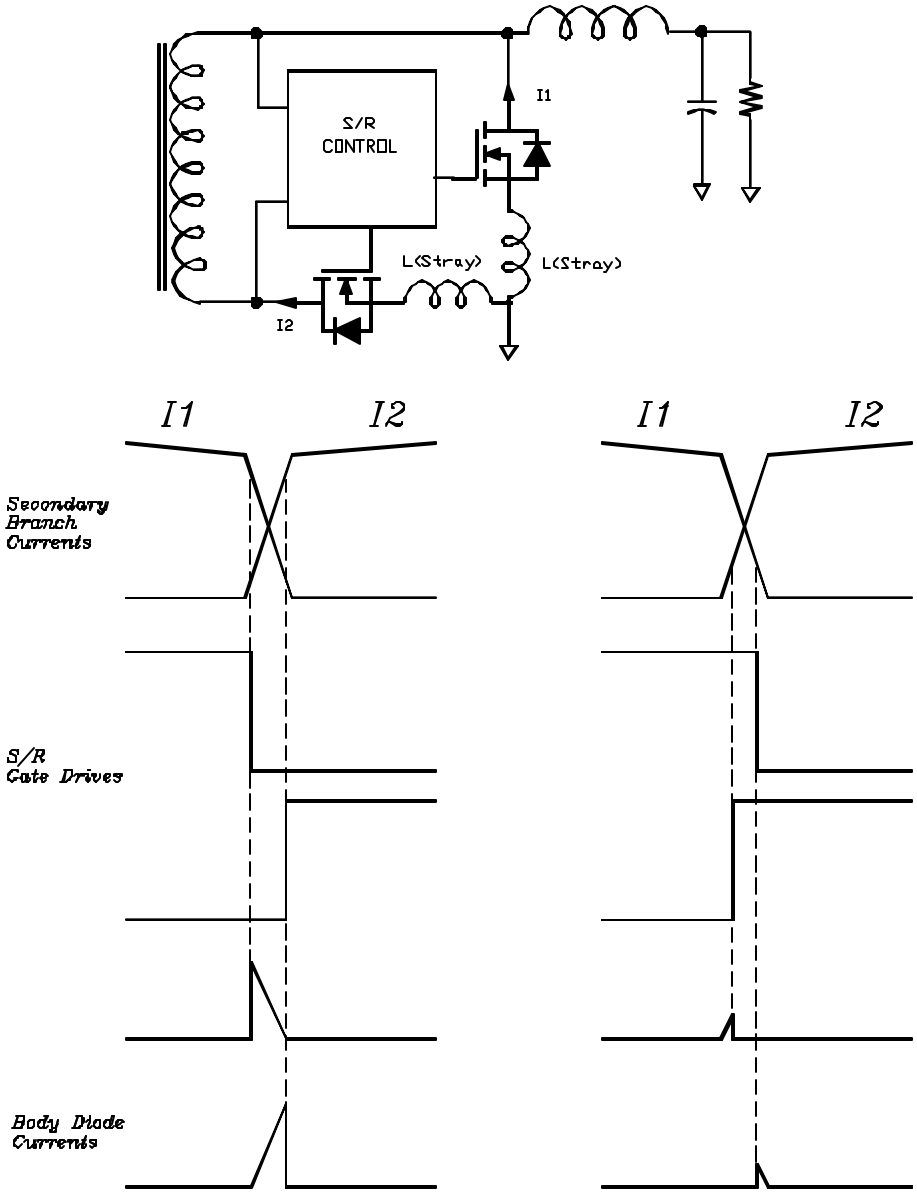


Fig 3 - Stray Inductance causes secondary branch currents to ramp up or down slowly during transformer transitions. MOSFET body diode conduction with dead-time in gate drives shows high peak currents. The overlapped gate drives show reduced conduction and hence losses.

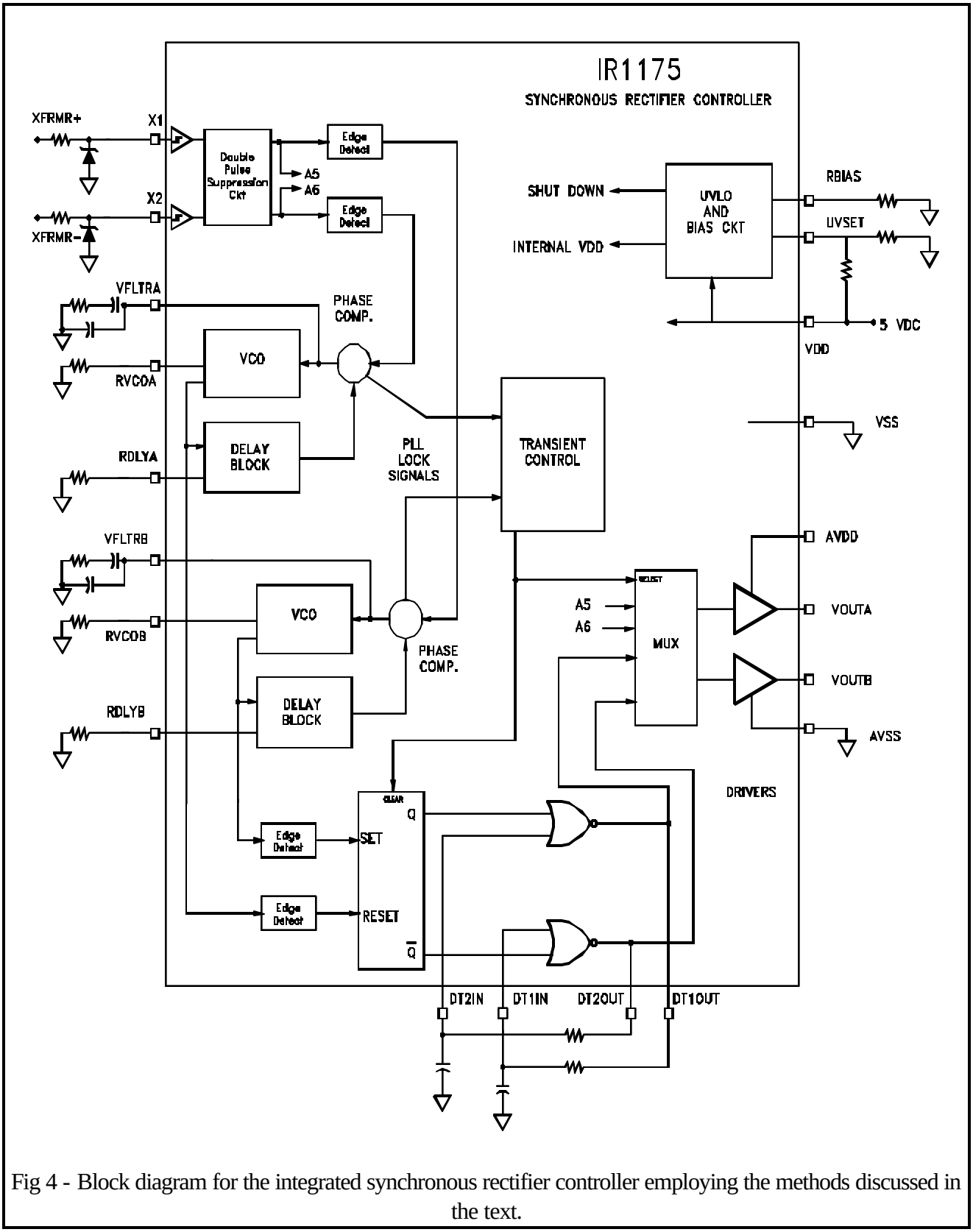


Fig 4 - Block diagram for the integrated synchronous rectifier controller employing the methods discussed in the text.

3 . EXPERIMENTAL RESULTS

A 5V CMOS integrated circuit (IR1175) has been fabricated employing the foregoing methods and based on the block diagram shown in Fig 4. Preliminary results have shown significant improvements in system efficiency over a conventional self-driven scheme in fixed frequency applications.

The experimental converter is shown in Fig. 5. The system was used to compare the efficiencies of the self - driven vs. the control-driven modes of operation. Both cases were tested under the same input and output conditions, i.e. Vin=48 VDC , Vout=3.3VDC, fosc=250 ~ 300 kHz and load currents of up to 20 ADC.

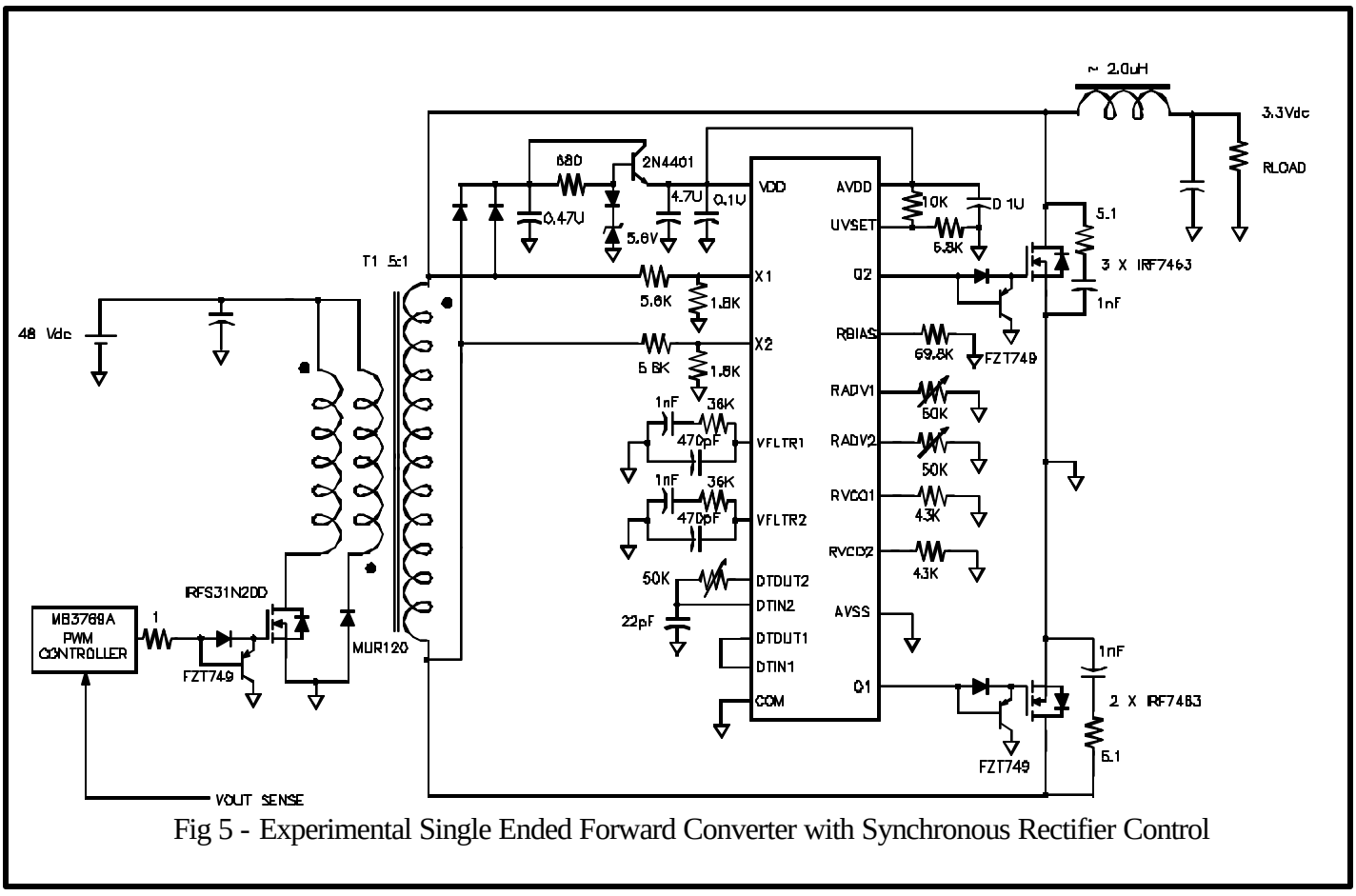


Fig 5 - Experimental Single Ended Forward Converter with Synchronous Rectifier Control

3.1 - MAIN CONVERTER AND COMPANION IR1175 BOARD

The experimental converter measures ~ 2.3" X 3.3" and consists of 8 layers of 4oz copper. E22/6/16 cores were used for all magnetics. The transformer turns ratio is 5:1 and the inductor measures ~2.0uH. The converter has two dedicated slots. The primary controller (PWM) and its associated circuitry are inserted in one. The other slot is dedicated to the IR1175 and its relevant circuitry.

3.2 PRIMARY SIDE COMPONENTS

An IRFS31N20D (200V , 80mΩ , Nch) surface-mount HEXFET® power MOSFET in a D^2PAK was used as the primary side switch. The device was driven through an appropriate gate driver with a 1 ohm gate resistor and a PNP transistor to speed the turnoff. The reset diode was an MUR120. The primary controller was powered from an external 12VDC supply. The current draw was measured to be ~32 mADC at 250kHz. For efficiency calculations, the primary controller power consumption was increased by 30% to account for conversion losses in the final circuit where the power must be derived from the main input source (35-72VDC).

3.3 - IR1175 COMPONENT SELECTION

3.3.1 - POWER SUPPLY , RBIAS AND UNDERVOLTAGE LOCKOUT.

IR1175 power was derived directly from the transformer secondary side through a linear regulator. Supply voltage was set to 5.1 VDC for applications where load currents of 10ADC or less. For higher load currents, where multiple HEXFET MOSFETs were used in parallel and PNP transistors were employed for fast turnoff, the supply voltage was boosted by one diode drop to maintain sufficient gate voltage for the synchronous rectifiers. RBIAS is a 69.8K +/- 2% resistor and is fixed for all applications. The UVSET pin is used to define the undervoltage lockout through a resistive divider from Vdd. Pulling this pin below 1.25VDC will disable the controller and ground Q1/Q2 outputs (external shutdown). Pulling the UVSET pin above 2.5 VDC disables the internal PLLs and directs the squared inputs from X1 and X2 to Q1 and Q2 respectively. The resistive divider should be calculated such that the UVSET is between 1.25 and 2.5 VDC under normal operating conditions (Vdd= 4.0 ~ 5.5 VDC). Below Vdd=4.0 VDC the IR1175 outputs are undefined.

3.3.2 - X1/X2 INPUTS

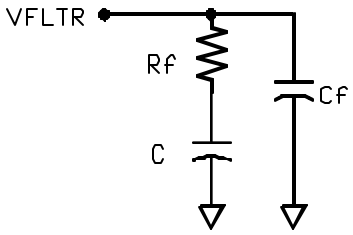
The IR1175 data sheet specifies the threshold of X1 and X2 inputs at 1.2VDC with a +/-200mV hysteresis. The maximum voltage for these inputs is specified as Vdd plus one diode drop. Depending on the transformer output levels some means of protection might be necessary. A number of options are available to the designer to avoid damaging X1 and X2 including simple resistor dividers or protective series resistors and Zener diodes shunted across the inputs. Regardless of the techniques employed, one has to account for the capacitance associated with the network at the inputs. The result of any capacitance at X1 and X2 is an RC network which delays the incoming pulse and will have to be compensated for by additional advance (Pre-fire) settings. Since the maximum advance setting per the IR1175 data sheet is 500nsec, if Zeners are required, then low capacitance ones are recommended to allow adequate headroom to compensate for the actual MOSFET switching times in the secondary side. This is especially important if multiple parallel devices are used. The experimental converter used a simple resistive divider which limits X1 and X2 to 1.75 - 3.6 VDC in the converter input range of 35~72 VDC.

3.3.3 - PLL COMPONENTS , VCO CENTER FREQUENCY AND LOOP FILTERS

RVCO1 and RVCO2 define the PLL center frequency. The value for these components can be calculated using the following equation:

$$RVCO(k\Omega) = 13.3\ E3\ /fvco(kHz)$$

A center frequency of fvco=300kHz results in a resistor value of ~44.3KΩ. For fvco=250kHz the value becomes 53.2KΩ. The experimental converter uses a standard 43KΩ resistor for both frequencies. Tests have shown no significant instabilities resulting form using the same resistor at both frequencies.
Loop filter components were calculated using the following relationships:



Kvco_ac (PLL small signal gain - kHz/Volt) = $62E3/(7*Rvco(k\Omega))$

ωn (PLL natural frequency) = $2\pi fn(KHz) = \sqrt{50 * Kvco\_ac(kHz/V) / C(nF)}$

ζ (Pll damping factor) = π E-3 *Rf (kΩ)*C(nF)*fn(kHz)

Value of Cf is normally chosen such that $Cf \cong C/16$

The selected loop filter components for the experimental converter result in a low center frequency of 14~15 khz and a damping factor of 1.7 ~ 2 (overdamped). These values were chosen to remove transient effects of the IR1175 from the overall performance. The transient response of the PLLs and its effects on converter performance will be published separately.

3.3.4 - ADVANCE TIMING COMPONENTS

The amount of advance (Pre-fire) is set by Radv1 and Radv2 resistors. The value for the resistors is calculated using the following relationship:

$$tadv(nsec) = Radv\ (K\Omega)*10 - 10$$

This value represents the advance from input pins X1 and X2 to output pins Q1 and Q2 respectively.
Dead time for each output is set by choosing a proper low pass RC filter between the DTOUT and DTIN pins. The amount of dead time is calculated from the following:

$$tdt(nsec) = 0.69*Rdt(K\Omega) * Cdt(pF) + 5 \quad \text{(Valid for Vdd=5 VDC)}$$

With Rdt=0 and Cdt=0 (DTIN shorted to DTOUT) the output gate drives Q1 and Q2 will cross at Vdd/2. With a Vdd equal to 5VDC this constitutes a slight overlap for logic level gate drives with gate thresholds in the ~1.7VDC range. A note regarding the advance and dead time settings is in order: The proper advance setting for pre-firing the synchronous rectifiers is calculated as follows:

$$tadv(req) = tpf + tdt$$

Where tpf is the required pre-fire time. In other words, inserting a dead time increases the value of the advance set between X1/X2 and Q1/Q2 by the amount of the dead time. As an example, if a 50 nsec pre-fire is required to drive the MOSFETs with a 100 nsec dead time, then the proper advance resistor (Radv) should be calculated using 150 nsec value. The experimental converter uses variable resistors to allow measurements under various advance and dead-time settings.

3.3.5 SECONDARY SIDE MOSFETS.

The following various types of SO-8, N channel HEXFET® power MOSFETs were used in the secondary side with varying results:

- IRF7811A - 30V, 10mΩ with Vgsmax=20 VDC - Two in parallel per leg - for load currents up to 12 ADC.
- IRF7455 - 20V, 5mΩ , Logic level gates - Two or Three in parallel per leg, for load currents up to 20ADC
- IRF7463 - 20V, 8mΩ , Logic level gates - Same as IRF7455.

3.3.6 IR1175 OUTPUT DRIVERS

A fast turn-on and specially turn off of the synchronous rectifiers is important for achieving high efficiency in converters. The IR1175 internal gate drivers can source and sink 2A. This is quite adequate for devices with input capacitances in the 1000 - 3000pF range. For multiple parallel devices, however there might be a need for even faster switching times. In this case external higher power gate driver must be used. Section 6.0 discusses the importance of fast turn off to reduce dead time requirements and hence, body diode losses. Fast turnoff can be accomplished by adding pnp transistors at the gates. This is the method used in the experimental converter.

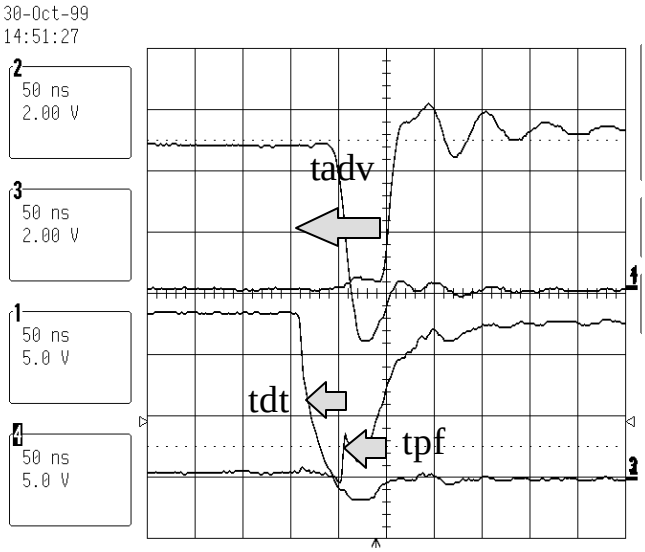


Fig 6 - Explanation of advance, dead time and pre-fire settings.
Top 2 traces: Transformer outputs
Bottom traces : IR1175 gate drive outputs (Q1 and Q2)

4.0 – WAVEFORMS

Figure 7 shows the primary and secondary waveforms for the self-driven mode. Fig 8 shows the waveforms obtained by using the IR1175. As evident, the steady gate drives generated by the controller eliminate the diode conduction seen in the self driven mode.

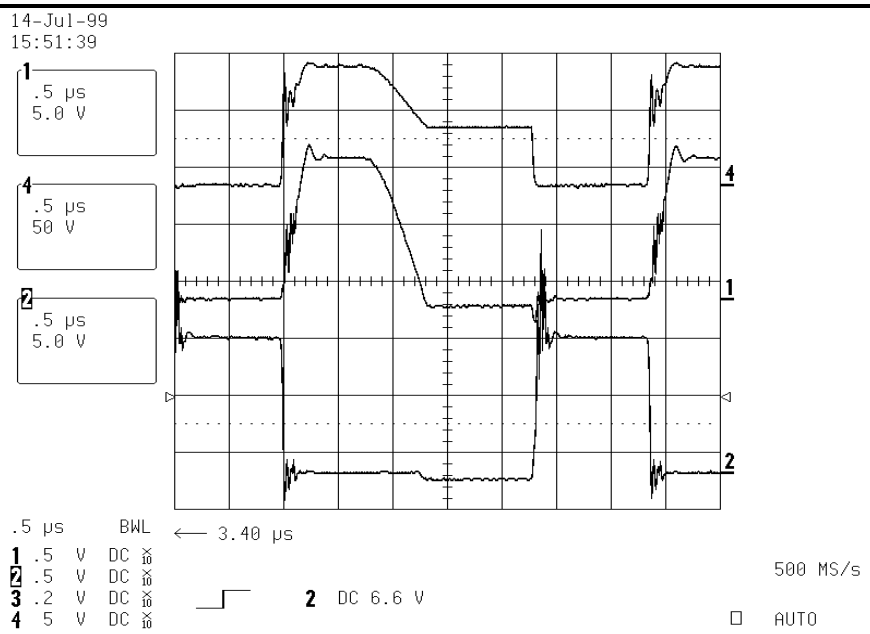
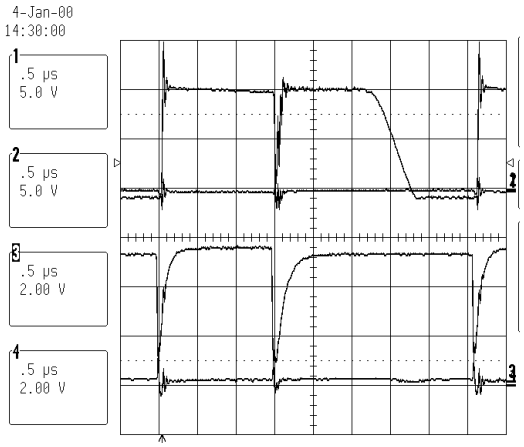
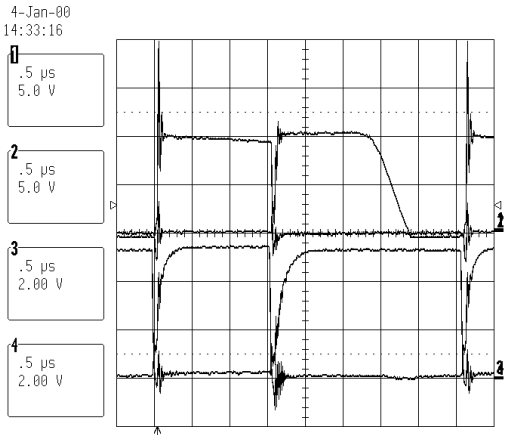


Fig 7 - Self Driven mode: Top trace: Primary side switch Drain to source voltage (Vds) - Middle trace: Transformer output during reset cycle. Bottom trace: Transformer output during power transfer cycle. Bottom trace shows diode conduction when gate drive during reset cycle disappears.
Devices used: 3 IRF7811A (Vgsmax=20VDC)in parallel in rectifying leg
3 IRF 7811A in parallel in recirculating leg.. A 2.2 ohm gate resistor was used for each leg.

Iout=6ADC **Iout=20ADC**

(A)





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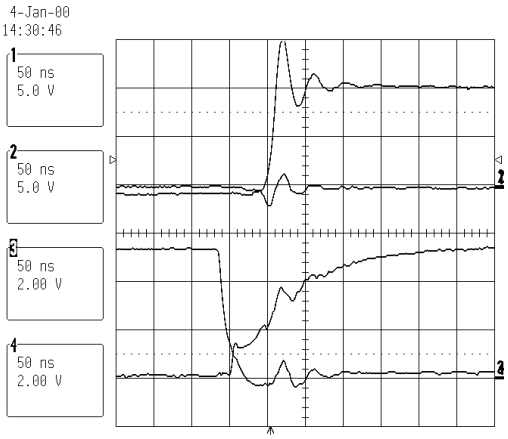
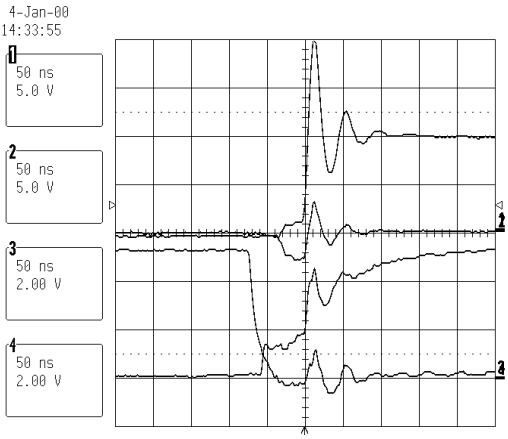
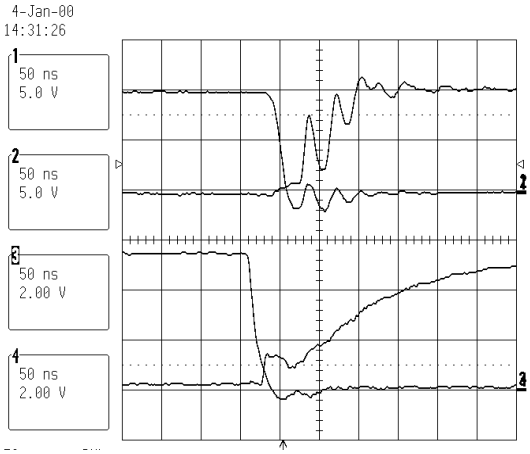




(C)



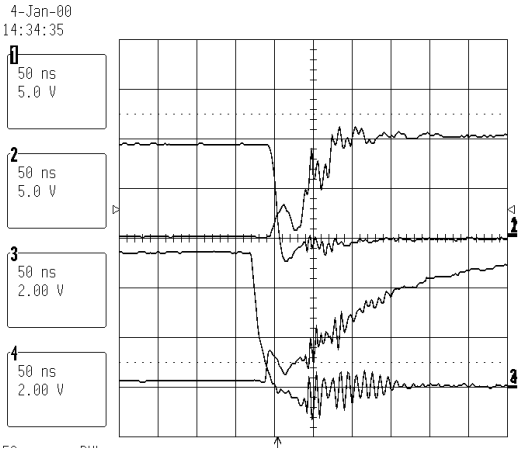
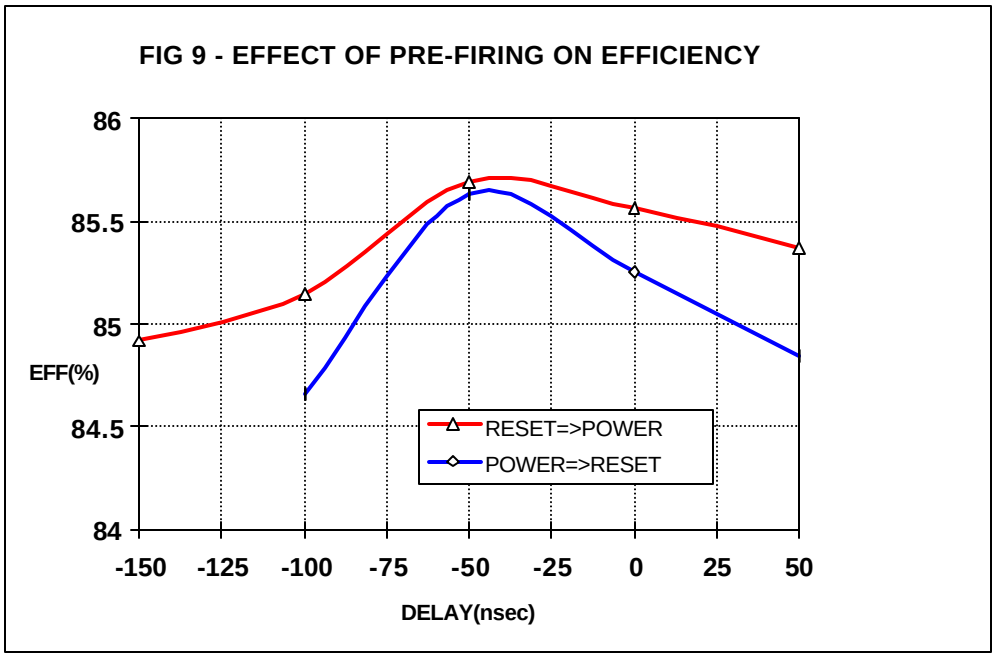


Fig 8 - IR1175 generated gate drives at various output currents showing proper advance settings for maximum efficiency. (Vin=48 VDC , Vout=3.3 VDC, f=250KHz)
(A) Traces 1 and 2: Transformer outputs - Traces 3 and 4: IR1175 Q1/Q2 outputs
(B) Close-up of reset-to-power transfer cycle transition.
(C) Close-up of power transfer-to-reset cycle.
Devices: 2 IRF7463 in parallel in rectifying leg - 3 IRF7463 in parallel in recirculating leg.

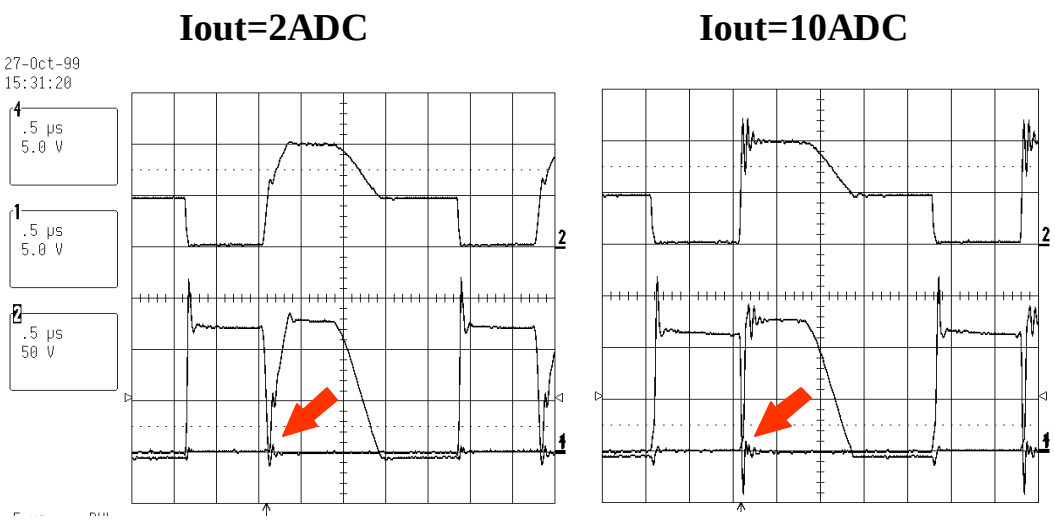
5.0 - EFFECTS OF PRE-FIRING

Fig 9 depicts the effects of pre-firing the HEXFET® power MOSFETs (negative delay) on the converter efficiency. The measurements were obtained at a load current of 10ADC with two IRF7811As in parallel per leg. As evident, the efficiency varies by the amount of pre-fire and shows an optimum point at ~ 38 nsec. Each graph depicts the effect of pre-firing on one transition, i.e. power transfer cycle to reset cycle transition and visa versa. The total efficiency gain at the optimum point is the sum of both increases. In this case, a total of ~1.2% . Another point worth mentioning is that both graphs peak at approximately the same advance setting this is simply because identical devices were used in both legs of the secondary side.

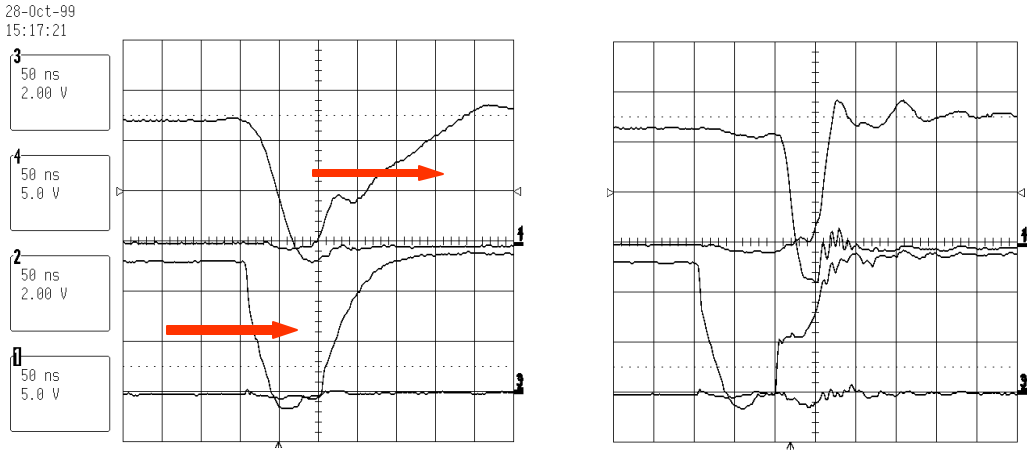


6.0 - IR1175 TRIGGERING OPTIONS

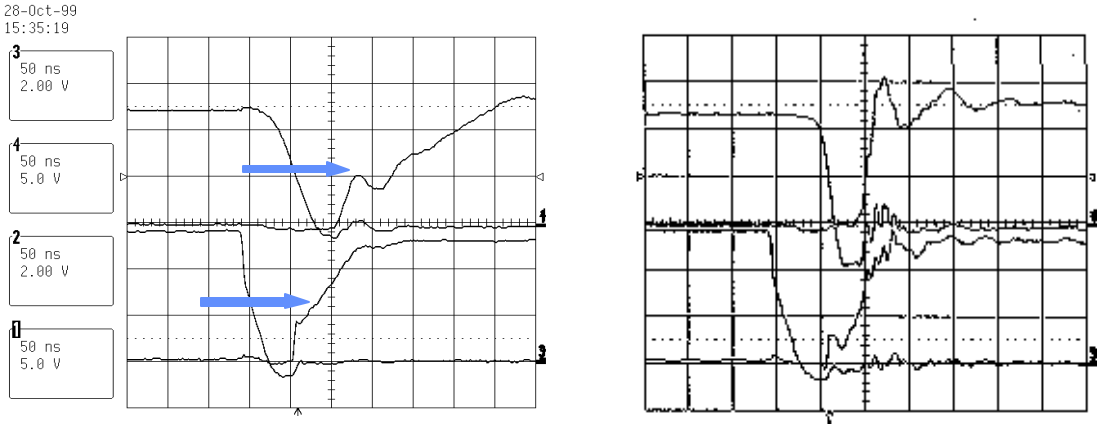
X1 and X2 inputs of the IR1175 can be derived from various sources with varying results. In Fig 5, inputs are derived from the leading edge of both transformer outputs. The inputs can also be triggered from only one transformer output through an appropriate inverter as shown in fig 11. This method will also result is valid outputs since a single transformer output does indeed have the necessary duty cycle information imposed by the primary side PWM controller. The difference can best be explained by considering the waveforms in figure 10. (A) shows the voltage across the primary switch along with the transformer secondary outputs. The waveforms are shown for two load currents (2 and 10 ADC). As noticeable, the slope of the transformer output changes with varying current due to the magnetizing and leakage inductance in the circuit. The effect of this slope change is to "push" or "pull" the gate waveforms as load current is changed. The slope change does not effect the advance settings, however, In the case where IR1175 outputs are derived from both leading edges (B in figure 10) adequate dead time should be included to avoid the possibility of the wrong device being on when the transformer reverses. But the effect of dead time is always body diode losses. In the case where the inputs to the IR1175 are derived from only one transformer output (C in fig 10) , the slope change is far less. This imposes less restriction on dead time requirements and results in a higher efficiency. Another method to minimize dead time requirements is to ensure that the secondary devices turn off relatively fast by utilizing pnp pull downs in their gates. This is the method used in the experimental converter.



A - Primary and Secondary Waveforms at Low and High Output Currents Showing Location Of Expanded Regions



B - Leading Edge Triggering Requires Larger Dead-Times Due To Large Variations (Less Efficient)



C - Trailing Edge Trigger Requires Less Dead-Time Due To Less Slope Variations (More efficient)

Fig 10 - Effects Of Load Current Change On IR1175 Outputs.

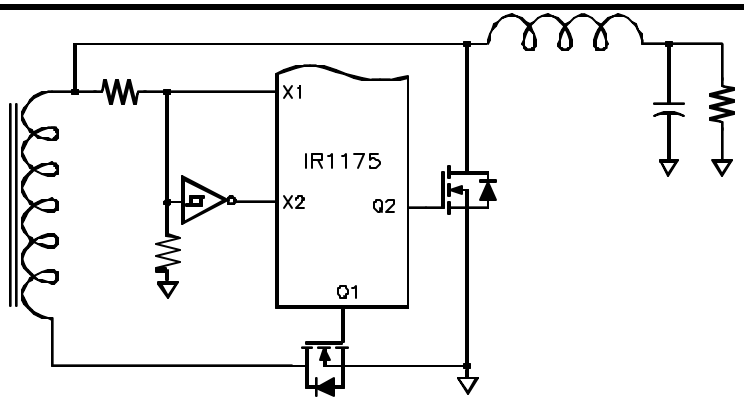


Fig 11 - Alternate method of generating inputs to the IR1175 - Leading and Falling edge trigger.

7.0 CONVERTER EFFICIENCY

The efficiency of the converter in fig. 5 was measured under different load conditions and with several types of HEXFET® power MOSFETs used as synchronous rectifiers . Fig 12 shows the results of the measurements. Results for the same converter with self-driven synchronous rectifiers are also included. In the legend, the first number in parenthesis represents the number of parallel devices in the rectifying leg while the second number reflects the same for the recirculating branch. As evident, the efficiency gain due to the IR1175 controller can be quite significant.

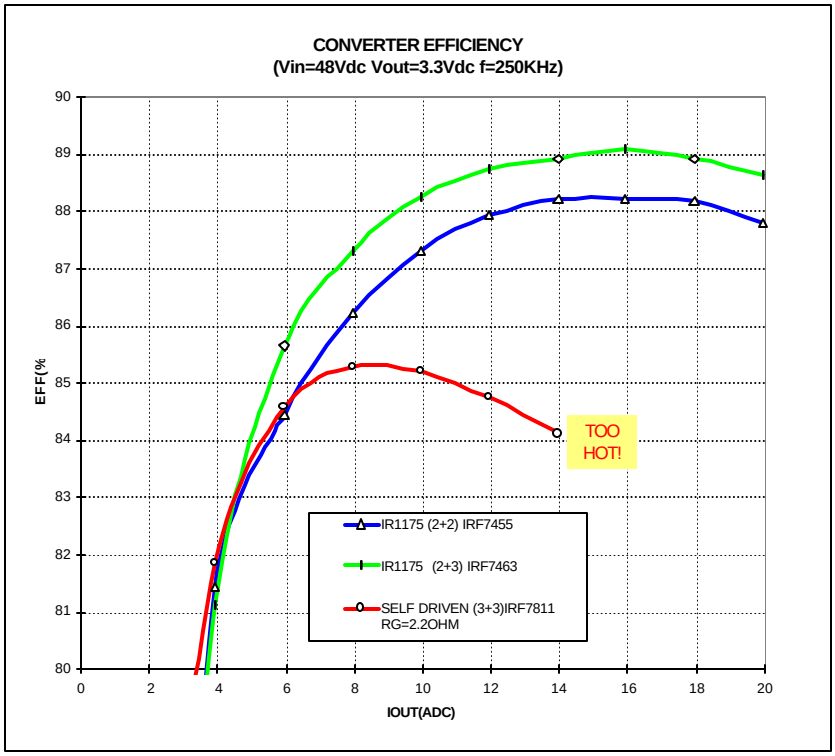


Fig 12: Efficiency of various synchronous rectifiers in the experimental converter.

4 . CONCLUSIONS

A method for controlling power MOSFETs used as synchronous rectifiers has been introduced which shows great promise in minimizing losses due to body diode conduction and increasing efficiency of DC/DC converters. The control method is a stand-alone transparent subsystem requiring no interaction with the primary side PWM controller. The controller generates required gate drives for the power MOSFETs without exerting unnecessary topological requirements on the primary side. The controller is capable of driving MOSFETs with different input characteristics while maintaining an efficiency increase over the self driven methodology. Moreover, the controller can be used in a adaptive environment where advance and dead times are externally varied to suit a number of system requirements.