Using Monolithic High Voltage Gate Drivers

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INTRODUCTION

The purpose of this paper is to highlight the most common subjects driving a half bridge power stage in motor drive applications (with monolithic IC gate driver) and to suggest appropriate solutions to solve the issues.

In the following sections different topics are discussed: the sizing of some fundamental components, as bootstrap circuit and on/off gate resistors; the half bridge parasitic elements are presented with their effects and some possible solutions are proposed. In the end section some layout tips are presented.

All the situations and the solutions proposed are, unless otherwise specified, for a typical IR monolithic gate driver with floating bootstrap supply.

BOOTSTRAP CIRCUIT

The bootstrap supply is formed by a diode and a capacitor connected as in figure 1.

This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor.

Proper capacitor choice can reduce drastically these limitations.

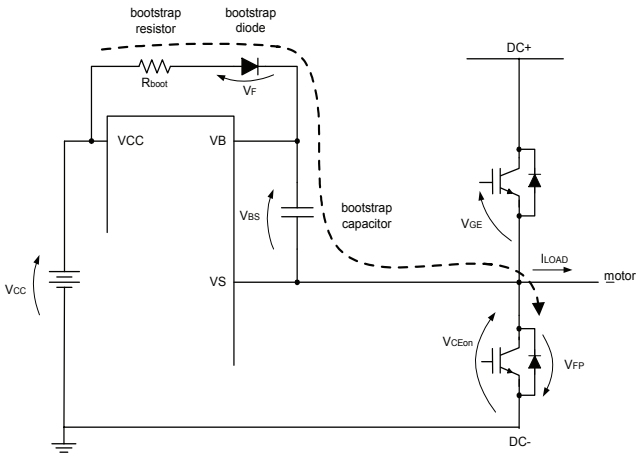


Figure 1: bootstrap supply schematic

Bootstrap capacitor sizing

To size the bootstrap capacitor, the first step is to establish the minimum voltage drop (ΔV_{BS}) that we have to guarantee when the high side IGBT is on. If VGEmin is the minimum gate emitter voltage to maintain, the voltage drop must be:

$$\Delta V_{BS} \leq V_{CC} - VF - V_{GEmin} - V_{CEon}$$

under the condition:

$$V_{GEmin} > V_{BSUV-}$$

where V_{CC} is the IC voltage supply, V_F is bootstrap diode forward voltage, V_{CE}on is emittercollector voltage of low side IGBT and V_{BSUV}- is the high-side supply undervoltage negative going threshold.

Now we must consider the influencing factors contributing V_{BS} to decrease:

- IGBT turn on required Gate charge (Q_G);
- IGBT gate-source leakage current (I_{LK_GE});
- Floating section quiescent current (I_{QBS});
- Floating section leakage current (I_{LK})
- Bootstrap diode leakage current (I_{LK_DIODE});
- Desat diode bias when on (I_{DS-})
- Charge required by the internal level shifters (Q_{LS});
- Bootstrap capacitor leakage current (I_{LK_CAP});
- High side on time (T_{HON}).

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic

capacitor (paralleling electrolytic and low ESR ceramic may result in an efficient solution).

Then we have:

$$Q_{TOT} = Q_G + Q_{LS} + (I_{LK\_GE} + I_{QBS} + I_{LK} + I_{LK\_DIODE} + I_{LK\_CAP} + I_{DS-}) \times T_{HON}$$

The minimum size of bootstrap capacitor is:

$$C_{BOOT\,min} = \frac{Q_{TOT}}{\Delta V_{BS}}$$

An example follows:

a) using a 25A @ 125C IGBT (IRGP30B120KD) and a high voltage half-bridge gate driver (IR2214):

- I_{QBS} = 800 µA (Datasheet IR2214);
- I_{LK} = 50 µA (Datasheet IR2214);
- Q_{LS} = 20 nC; Q_G = 160 nC (Datasheet IRGP30B120KD);
- I_{LK_GE} = 100 nA (Datasheet IRGP30B120KD);
- I_{LK_DIODE} = 100 µA (with reverse recovery time <100 ns);
- I_{LK_CAP} = 0 (neglected for ceramic capacitor);
- I_{DS}- = 150 µA (Datasheet IR2214);
- T_{HON} = 100 µs.

And:

- V_{CC} = 15 V
- V_F = 1 V
- $V_{CEonmax}$ = 3.1 V
- V_{GEmin} = 10.5 V

the maximum voltage drop ΔV_{BS} becomes

$$\Delta V_{BS} \leq V_{CC} - V_F - V_{GEmin} - V_{CEon} = 15V - 1V - 10.5V - 3.1V = 0.4V$$

And the bootstrap capacitor is:

$$C_{BOOT} \geq \frac{290\ nC}{0.4\ V} = 725\ nF$$

Notes:

1. Here above VCC has been chosen to be 15V. Some IGBTs may require higher supply to properly work with the bootstrap technique. Also Vcc variations must be accounted in the above formulas.

2. This kind of bootstrap sizing approach does not take into account neither the duty cycle of the PWM, nor the funda mental frequency of the current. It considers only the amount of charge that is needed when the high voltage side of the driver is floating and IGBT gate is driven once. Considerations on PWM duty cycle, kind of modulation (six-step, 12-step, sine-wave) must be considered with their own peculiarity to achieve best bootstrap circuit sizing.

Considerations about bootstrap circuit

a. Voltage ripple

Three different situations can occur in the bootstrap capacitor charging (see figure 1):

- I_{LOAD} < 0; the load current flows in the low side IGBT displaying relevant V_{CEon}

$$V_{BS} = V_{CC} - V_F - V_{CEon}$$

In this case we have the lowest value for VBS. This represents the worst case for the bootstrap capacitor sizing. When the IGBT is turned off the Vs node is pushed up by the load current until the high side freewheeling diode gets forwarded biased

- I_{LOAD} = 0; the IGBT is not loaded while being on and V_{CE} can be neglected

$$V_{BS} = V_{CC} - V_F$$

- I_{LOAD} > 0; the load current flows through the freewheeling diode

$$V_{BS} = V_{CC} - V_F + V_{FP}$$

In this case we have the highest value for V_{BS}. Turning on the high side IGBT, I_{LOAD} flows into it and V_S is pulled up.

To minimize the risk of undervoltage, bootstrap capacitor should be sized according to the I_{LOAD}<0 case.

b. Bootstrap Resistor

A resistor (R_{boot}) is placed in series with bootstrap diode (see figure 1) so to limit the current when the bootstrap capacitor is initially charged. The choice of bootstrap resistor is strictly related to V_{BS} time-constant. The minimum on time for charging the bootstrap capacitor or for refreshing its charge must be verified against this time-constant.

c. Bootstrap Capacitor

For high T_{HON} designs where is used an electrolytic tank capacitor, its ESR must be considered. This parasitic resistance forms a voltage divider with R_{boot} generating a voltage step on V_{BS} at the first charge of bootstrap capacitor. The voltage step and the related speed (dV_{BS}/dt) should be limited. As a general rule, ESR should meet the following constraint:

$$\frac{ESR}{ESR + R_{BOOT}} \cdot V_{CC} \leq 3\,V$$

Parallel combination of small ceramic and large electrolytic capacitors is normally the best compromise, the first acting as fast charge tank for the gate charge only and limiting the dV_{BS}/dt by reducing the equivalent resistance, while the second keeps the VBS voltage drop inside the desired ΔV_{BS}.

d. Bootstrap Diode

The diode must have a BV > DC+ and a fast recovery time (trr < 100 ns) to minimize the amount of charge fed back from the bootstrap capacitor to V_{CC} supply.

GATE RESISTANCES

The switching speed of the output transistor can be controlled by properly size the resistors controlling the turn-on and turn-off gate current. The following section provides some basic rules for sizing the resistors to obtain the desired switching time and speed by introducing the equivalent output resistance of the gate driver (RDRp and RDRn respectively of p and n channel). The examples always use IGBT power transistor. Figure 2 shows the nomenclature used in the following paragraphs. In addition, V_{ge}* indicates the plateau voltage, Q_{gc} and Q_{ge} indicate the gate to collector and gate to emitter charge respectively.

Sizing the turn-on gate resistor

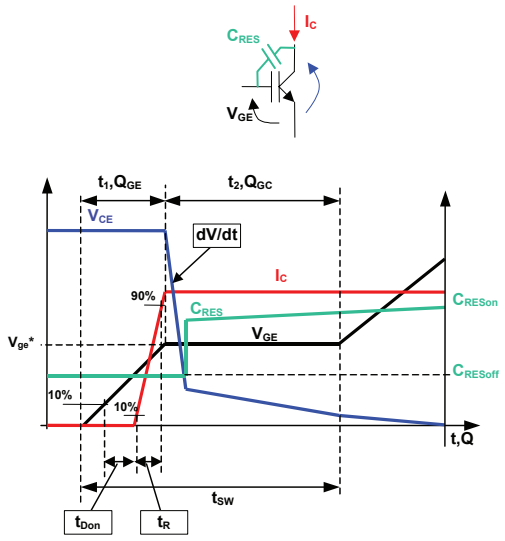


Figure 2: Nomenclature

Gate resitances may be chosen in order to fix either the switching-time or the output voltage slope. Hereafter are presented both the methods.

Switching-time

For the matters of the calculation included hereafter, the switching time tsw is defined as the time spent to reach the end of the plateau voltage (a total Qgc + Qge has been provided to the IGBT gate). To obtain the desired switching time the gate resistance can be sized starting from Qge and Qgc, Vcc, Vge* (see figure 3):

$$I_{avg} = \frac{Q_{gc} + Q_{ge}}{t_{sw}}$$

and

$$R_{TOT} = \frac{Vcc - V_{ge}^{*}}{I_{avg}}$$

where TOT DRp Gon R = R + R , RGon = gate on-resistor and RDRp = driver equivalent on-resistance (from the gate driver datasheet)

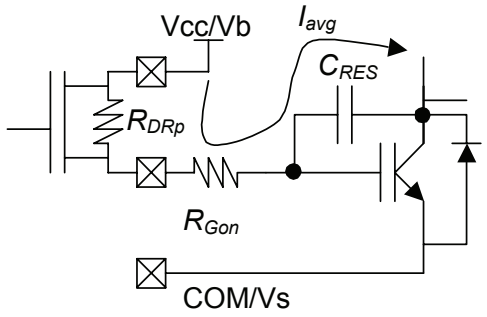


Figure 3: R_{Gon} sizing

Table 1 reports the gate resistance size for two commonly used IGBTs (calculation made using typical datasheet values and assuming Vcc=15V).

Output voltage slope

Turn-on gate resistor RGon can be sized to control output slope (dV_{OUT}/dt).

While the output voltage has a non-linear behaviour, the maximum output slope can be approximated by:

$$\frac{dV_{out}}{dt} = \frac{I_{avg}}{C_{RESoff}}$$

inserting the expression yielding I_{avg} and rearranging:

$$R_{TOT} = \frac{Vcc - V_{ge}^{*}}{C_{RESoff} \cdot \frac{dV_{out}}{dt}}$$

As an example, table 2 shows the sizing of gate resistance to get dVout/dt=5V/ns when using two popular IGBTs, typical datasheet values and assuming Vcc=15V.

Sizing the turn-off gate resistor

The worst case in sizing the turn-off resistor R_{Goff} is when the collector of the IGBT in off state is forced to commutate by external events.

In this case, dV/dt of the output node induces a parasitic current through CRESoff flowing in RGoff and RDRn (see figure 4)1.

If the voltage drop at the gate exceeds the threshold voltage of the IGBT, the device may self turn on causing large oscillation and relevant cross conduction.

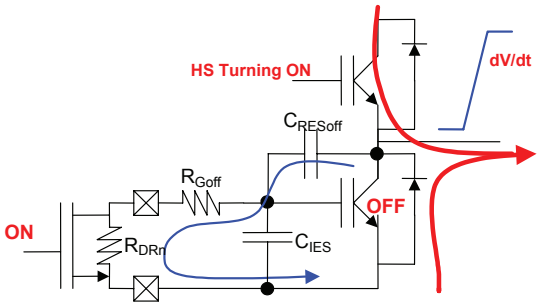


Figure 4: R_{Goff} sizing: current path when Low Side is off and High Side turns on

Hereafter is described how to size the turn-off resistor when the output dV/dt is caused by the companion IGBT turning-on (as shown in figure 4).

Other dV/dt cases may be present and must be taken into account. As an example, the dV/dt generated by long motor cable coupling (high frequency spikes).

For this reason the off-resistance must be properly sized according to the application worst case.

The following equation relates the IGBT gate threshold voltage to the collector dV/dt:

$$V_{th} \geq (R_{Goff} + R_{DRn}) \cdot I = (R_{Goff} + R_{DRn}) \cdot C_{RESoff} \frac{dV_{out}}{dt}$$

Rearranging the equation yields:

$$R_{Goff} \leq \frac{V_{th}}{C_{RESoff} \cdot \frac{dV}{dt}} - R_{DRn}$$

As an example, table 3 reports RGoff for two popular IGBT to withstand dV_{out}/dt = 5V/ns.

NOTES: The above-described equations are intended to be an approximated way for the gate resistances sizing. More accurate sizing may take into account more precise device

Table 1: t_{sw} driven R_{Gon} sizing (for R_{DRp} = 7 Ω)

IGBT	Qge	Qgc	Vge*	tsw	Iavg	Rtot	RGon → std commercial value	Tsw
IRGP30B120K(D)	19nC	82nC	9V	400ns	0.25A	24Ω	RTOT - RDRp = 17 Ω → 18 Ω	→420ns
IRG4PH30K(D)	10nC	20nC	9V	200ns	0.15A	40Ω	RTOT - RDRp = 33 Ω	→200ns

Table 2: dV_{OUT}/dt driven R_{Gon} sizing (for R_{DRp} = 7 Ω)

IGBT	Qge	Qgc	Vge*	CRESoff	Rtot	RGon → std commercial value	dVout/dt
IRGP30B120K(D)	19nC	82nC	9V	85pF	14Ω	RTOT - RDRp = 7 Ω → 8.2 Ω	→4.5V/ns
IRG4PH30K(D)	10nc	20nC	9V	14pF	85Ω	RTOT - RDRp = 78 Ω → 82 Ω	→5V/ns

Table 3: R_{Goff} sizing

IGBT	Vth(min)	CRESoff	RGoff
IRGP30B120K(D)	4	85pF	RGoff ≤ 4 Ω
IRG4PH30K(D)	3	14pF	RGoff ≤ 35 Ω

modelling and parasitic component dependent on the PCB and power section layout and related connections.

Another way to size the gate resistors is following power dissipation constraints. This way is not investigated here.

[1]This is true under the assumption that gate voltage remains fixed during dV/dt. The result is reasonable whenever CIES is at least two order of magnitude greater than CRES).

PARASITIC ELEMENT EFFECTS

In figure 5 a single-phase motor drive power stage and its driver is shown. Some of the characteristics of the driver and the power stage will be analyzed. To properly drive the power stage it is very important to know the effects of inductive parasitic elements. In normal operation mode the fast voltage variations, induced by a fast current change, may influence the gate driver performances.

In presence of high and low power signals both referenced to the same ground, it is important to avoid ground loops on board or ground planes close to the switching portions of the board. This solution reduces the noise coupled to the local ground of the driver. Moreover it is suggested to make star connections between ground pins and board ground for all gate drivers (see layout tips).

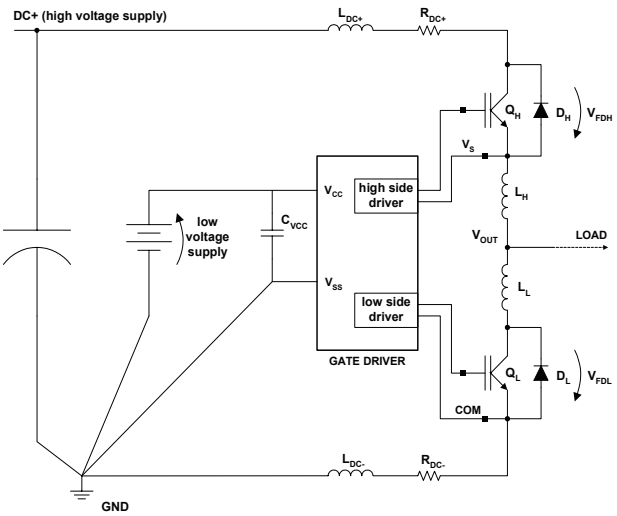


Figure 5: Parasitic elements in the power stage

COM below Ground (Vss-COM)

Low side IGBT is considered to explain COM below Vss event. Figure 6 shows one of the possible configurations of the parasitic elements in the half bridge configuration (here

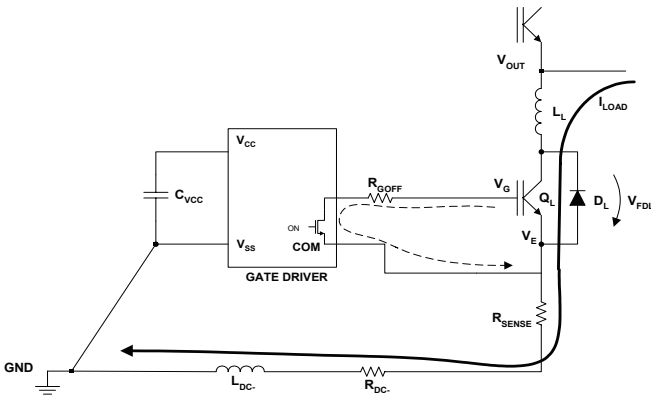


Figure 6: Parasitic elements during low-side turn-off

emitter sense shunt is included for completeness).

Consider to turn off (dotted arrow) the low side IGBT when load current is flowing through it (bold arrow). As the power device turns off the current flowing in the parasitic inductance (L_{DC-}) changes rapidly and the induced voltage pushes COM below ground.

The amount of voltage flyback is governed by the well known law:

$$V_{L_{dc-}} = L_{DC-} \cdot \frac{dI_{L_{DC-}}}{dt}.$$

This equation relates COM undershoot (strictly dependent on inductance voltage) to the slope of load current.

For this reason, the first solution is to turn off more softly the IGBT, by increasing the low side turn off resistor (respecting the superior limit, see sizing the turn-off gate resistor section), to limit the dI_L/dt.

This solution may be not sufficient when in presence of a phase-DC+ short circuit.

These kind of short circuits are usually broken turning off the low side IGBT. Short circuit detection may react when current has exceeded several times the rated current for normal operation inducing faster current change at turn-off.

In that case the solution shown in figure 7 prevents COM pin to follow IGBT emitter filtering the under-Vss spike.

RCOM should be taken into account when sizing the turn-off

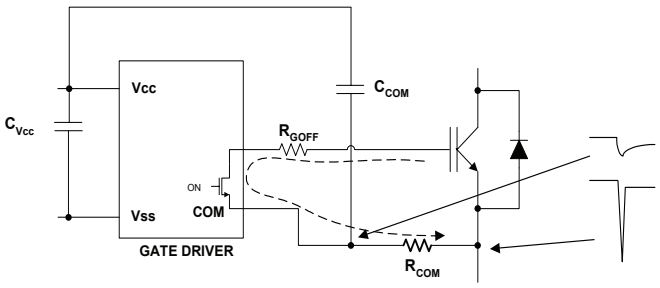


Figure 7: C_{COM} and R_{COM} added

resistance (that becomes RGOFF + RCOM).

RCOM and CCOM sizing establishes the time constant of COM pin that can be set to some hundred of ns.

To avoid noise coupling to VCC size the rule $\frac{C_{COM}}{C_{VCC}} << 1$ as required by the application.

NOTES: IGBT short circuit desaturation easily generate high collector dV/dt. IGBT gate is pulled above the local supply by the gate-collector stray capacitance.

In some cases (usually when turn-on resistor is low) a fast diode is needed between IGBT gate and local supply to protect the driver output (figure 8).

As an alternative solution a zener clamp can be placed be-

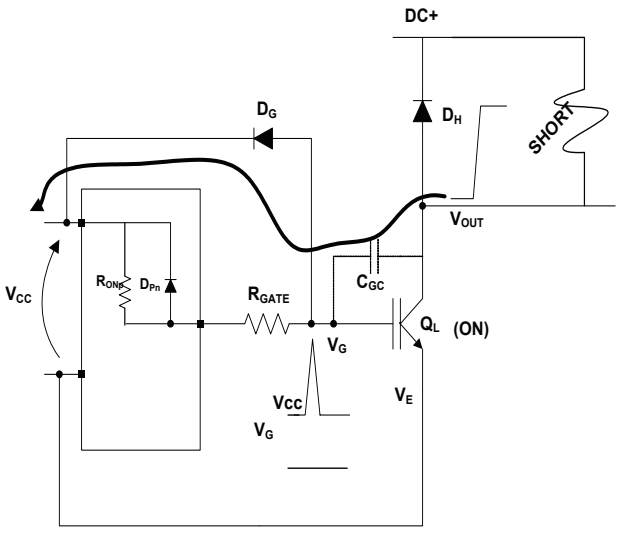


Figure 8: Driver output protection in case of IGBT desaturation

tween IGBT gate and emitter. It should be sized accordingly to IGBT gate-emitter absolute maximum ratings.

The advantage of the zener is both to protect the driver output, sinking the current generated by the collector dV/dt, and to keep IGBT gate-emitter voltage under control.

This is particularly important during IGBT turn-off after short circuit detection, while IGBT emitter spikes under VSS due to

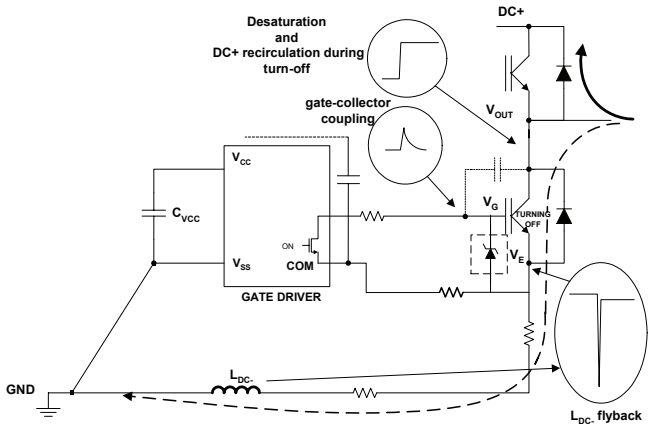


Figure 9: zener protection for IGBT gate-emitter

DC- stray inductance (L_{DC-}, see figure 9).

VS below Ground (Vs-COM/VSS)

A well known event that triggers Vs to go below Vss or COM is the forward biasing of the low side

freewheeling diode. This usually happens when current flows out of the half-bridge towards the

load.

In steady state Vs is clamped below Vss of about:

$$V_S^{steady} - V_{SS} = -V_{FDL} - \left(R_{SENSE} + R_{DC-}\right) \cdot I_{LOAD}$$

And below COM:

$$V_S^{steady} - COM = -V_{FDL}$$

where I_{LOAD} is positive flowing towards the load.

The maximum voltage difference between V_s and V_{ss} or COM can be found in the datasheet looking for V_S absolute maximum ratings and recommended operating conditions.

Major issues may appear during commutation, just before the freewheeling diode starts clamping.

In this case the inductive parasitic elements shown in figure 10 (L_{dc-}, L_L and L_H) may act pushing down V_s below V_{ss} even more than as above mentioned for steady state condition.

The derivative terms of the following equation may be the highest contribute during commutation transient:

For Vss:

$$V_S^{tran} - V_{SS} = -V_{FDL} - \left(R_{SENSE} + R_{DC-}\right) \cdot I_L - \left(L_{DC-} + L_L\right) \cdot \frac{dI_L}{dt} - L_H \cdot \frac{dI_H}{dt}$$

For COM:

$$V_S^{tran} - COM = -V_{FDL} - L_L \cdot \frac{dI_L}{dt} - L_H \cdot \frac{dI_H}{dt}$$

In order to reduce the slope of current flowing in the parasitic inductances so to minimize the derivative terms, R_{GOFF} can be increased, respecting previously discussed constraints (R_{GOFF} sizing section).

Resistor between Vs and Vout

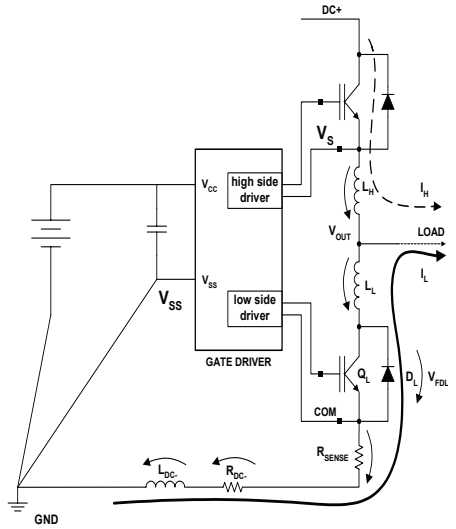


Figure 10: Elements causing V_s going under V_{ss}

While the above mentioned solution may work in normal operating conditions, it can be not sufficient, as an example, when a short circuit between phase and ground occurs while the highside IGBT is on. Once the high side IGBT has been turned off, the high amount of current that was flowing through it starts flowing through the low-side freewheeling diode.

The high $\frac{dI}{dt}$ may even pull VB (the floating stage supply) below ground by means of the bootstrap capacitor. This happens when:

$$V_S^{tran} - V_{SS} < -V_{CC}$$

It should be noted that we are considering high frequency events, so that the bootstrap diode may reasonably keep turned off.

Real damage for monolithic ICs is caused by the amount of current stolen from VB pin (via Cboot coupling with VS). In order to minimize this current a resistor (R_{VS}) can be placed between VS and Vout as shown in figure 11.

Suggested values for R_{VS} are in the range of some Ohms.

NOTES:

1. R_{VS} works in series to the bootstrap resistor and must be considered in sizing the bootstrap resistance (R_{BOOT}*= R_{BOOT}+R_{VS}).

2. It is also important to notice that the current developed across RVS during initial bootstrap charge may be such that a relevant voltage is developed between the high side IGBT emitter and the VS pin. This voltage may be brought to the high side output (usually HO) through the HO-VS ESD protection diode. In this case it must be verified that IGBT gate doesn't turn on at bootstrap start-up (gate resistor and gate-emitter capacitance help to filter out this pulse). This may cause a short shoot-through at inverter output.

3. RVS takes also part in turn-on (R_{GON}+R_{VS}) an turn-off resistor sizing (R_{GOFF}+R_{VS}) as shown in figure 12.

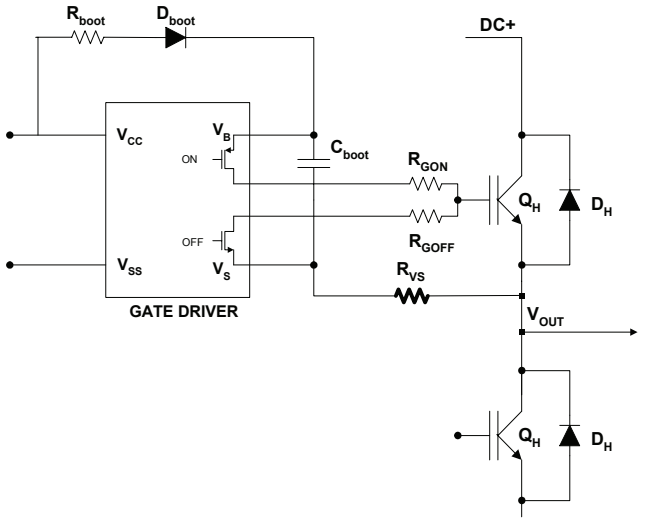


Figure 11: R_{VS} connection

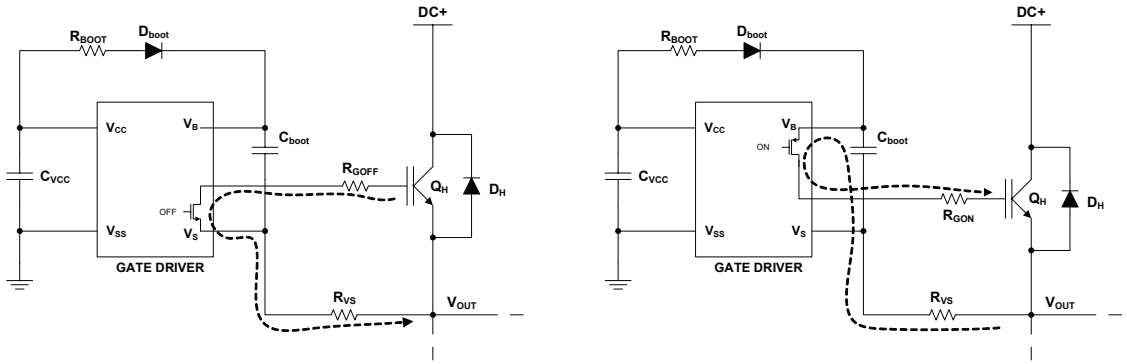


Figure 12: Gate turn-on and turn-off with R_{VS}

Clamping diode for Vs

In the previous paragraph it has been supposed that D_{BOOT} keeps switched off considering such events acting at high frequency.

Whenever this assumption is not verified, while V_S follows V_{OUT}, V_B can be tied to V_{CC} by the boostrap diode. In this case the difference between V_B and V_S should be kept inside the absolute maximum specification (see IC datasheet):

$$V_B - V_S < V_{VBS\_abs\max}$$

In order to keep in specification, a clamp device should be positioned between V_{SS} and V_S as shown in figure 13, where a zener diode and a 600V diode are placed.

Zener voltage must be sized following the rule:

$$V_Z \le V_{VB\_abs\max} - V_{CC}$$

In most of the cases the use of a zener is not necessary, and only the HV diode is used.

The clamp must be connected to COM pin (just in some cases to Vss pin) according to device datasheet. This information can be usually found under the absolute maximum ratings.

PCB LAYOUT TIPS

Distance from high to low voltage

To minimize the noise coupled between the signals referred to ground and those floating it's strongly recommended to place components tied to floating voltage in the high voltage side of device (V_B, V_S side) while the other components in the opposite side.

Ground plane

Ground plane must not be placed under or nearby the high voltage floating side to minimize noise coupling.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition	Min.	Max.	Units
VB	High Side Floating Supply Voltage	-0.3	625	

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to Vss, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
Vs	High side offset voltage	VB - 25	VB + 0.3	

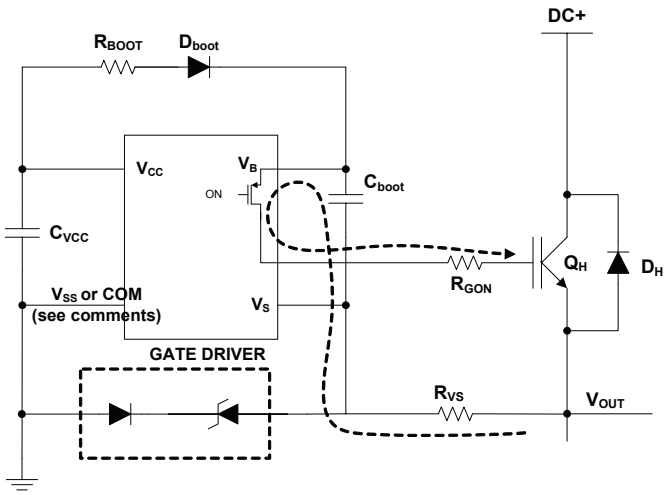


Figure 13: Clamping structure with zener diode

Supply capacitors

If the output stages are able to quickly turn on IGBT with high value of current, the supply capacitors must be placed as close as possible to the device pins (V_{CC} and V_{SS} for the ground tied supply, V_B and V_S for the floating supply) in order to minimize parasitic inductance/resistance.

Gate drive loops

Current loops behave like an antenna able to receive and transmit EM noise. In order to reduce EM coupling and improve the power switch turn on/off performances, gate drive loops must be reduced as much as possible. Figure 14 shows the high and low side gate loops.

Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to develop a voltage across the gate-emitter increasing the possibility of self turn-on effect. For this reason is strongly recommended to place the gate resistances close together and to minimize the loop area (see figure 14).

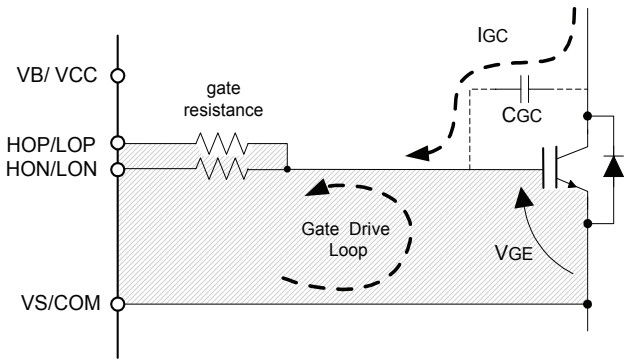


Figure 14: gate drive loop

Routing and placement example

We consider, as example, the IR2214 a high voltage and high output current gate driver, see the lead assignments in figure 15.

Figure 16 shows one of the possible layout solutions using a 3 layer PCB. This example takes into account all the previous considerations. Placement and routing for supply capacitors and gate resistances in the high and low voltage side minimize respectively supply path and gate drive loop. The bootstrap diode is placed under the device to have the cathode as close as possible to bootstrap capacitor and the anode far from high voltage and close to V_{CC}.

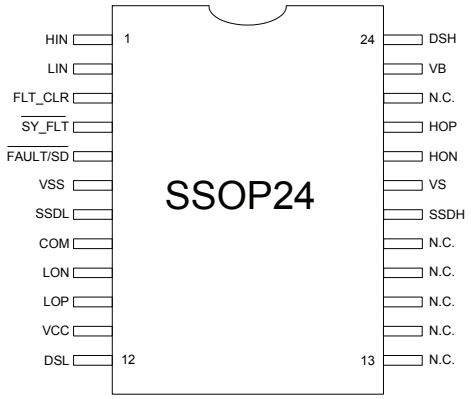


Figure 15: IR2214 lead assignments

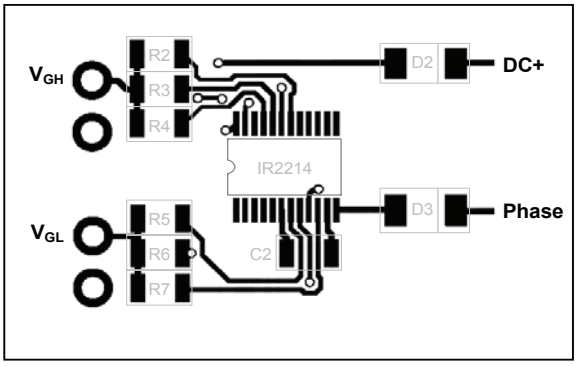


Figure 16(a): TOP

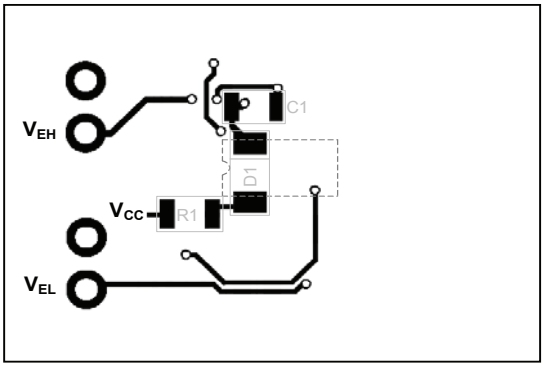
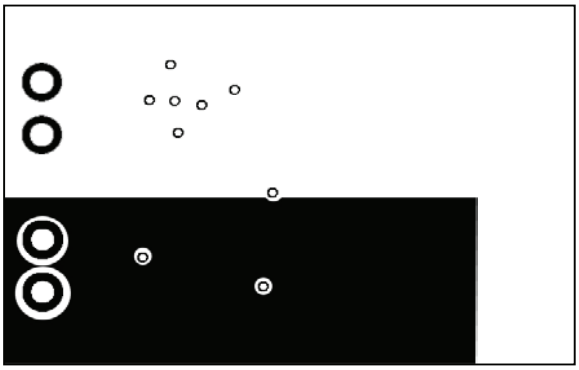


Figure 16(b): BOTTOM



Referred to figure 16:
Bootstrap section: R1, C1, D1
High side gate: R2, R3, R4
High side Desat: D2
Low side supply: C2
Low side gate: R5, R6, R7
Low side Desat: D3

Figure 16(c): Ground plane