QR-0005:
Reliability Qualification Report for IRS2113SPBF

Date: June 19th, 2006

Qualification Vehicle: IRS2113SPBF in 16L-SOICW Package:

Based on the reliability test results, the IRS2113SPBF has passed standard International Rectifier industrial-level qualification with MSL3 at 260 °C peak reflow temperature (PRT).
The handling, packing, shipping and use of the moisture/reflow sensitive surface mount devices need to be per IPC/JEDEC J-STD-033A spec.

Device and Lot Information

Rel Number	10268-1-2-3	
Product/Part #	IRS2113SPBF	
Qualification Level	Lead-Free Industrial per COP800-08-Rev00	
Silicon Technology	600 V HVIC	
Silicon Generation	Gen 5	
Wafer Fab	Fab11	
Wafer-Lot#	Qual Lot#1 (Lot ID 1): 311445.1 Qual Lot#2 (Lot ID 2): 311455.1 Qual Lot#3 (Lot ID 3): 311482.1	
Package	IRS2113SPBF: 16L-SOICW	
Lead Finish Plating	100% Sn	
Assembly-Lot#	Qual Lot#1 (Lot ID 1): IC1205AO Qual Lot#2 (Lot ID 2): IC1205AP Qual Lot#3 (Lot ID 3): IC1205CG	D/C: 0551 D/C: 0551 D/C: 0604
Moisture Sensitivity Level	IRS2113S/16L-SOICW: MSL3 @ 260 °C Per JEDEC spec JA113 / JEDEC J-STD-020C (Test samples were subjected to preconditioning prior to AC, TC & THB reliability tests, HTB and HTSL samples do not require preconditioning).	
Reliability Test Location	IR Temecula, USA	

Reliability Test Results:

Samples from three wafer lots and three assembly lots were tested in the following reliability tests to determine typical lifetime performance under industrial level qualification. The tests samples passed AC, TC, THB, HTB and HTSL reliability test requirements.

THE STRESS TESTS CONDITIONS AND RESULTS ARE AS FOLLOWS:

Reliability Test #1 - Autoclave Test:

Test Duration: 96 Hours
Test Condition: +121 °C, 100% RH and 15 PSIG
Bias Condition: None
Electrical Testing: @ Room

Device	Lot ID	Hour	SS	Reject	Remark
IRS2113SPBF	311445.1	96	80	0	
	311455.1	96	80	0	
	311482.1	96	80	0	

Reliability Test #2 - Temperature Cycling:

Test Duration: 1000 Cycles
Test Condition: -55 °C to 150 °C (ΔT=205 °C, Dry-Air to Dry-Air)
Bias Condition: None
Electrical Testing: @ Room

Device	Lot ID	Cycle	SS	Reject	Remark
IRS2113SPBF	311445.1	1000	80	0	
	311455.1	1000	80	0	
	311482.1	1000	80	0	

Reliability Test #3 - Temperature Humidity Bias (THB) Test:

Test Duration: 1000 Hours
Test Condition: 85 °C, 85% RH
Bias Condition: V_{CC}=20 V, V_{DD}=20 V & V_S=0 V (Com)
Electrical Testing: @ Room

Device	Lot ID	Hour	SS	Reject	Remark
IRS2113SPBF	311445.1	1000	80	0	
	311455.1	1000	80	0	
	311482.1	1000	80	0	

Reliability Test #4 - High Temperature Bias (HTB) Test:

Test Duration: 1008 Hours
Test Condition: T_j=150 °C
Bias Condition: V_{CC}=20 V, V_{DD}=20 V, V_{BS}=20 V, V_S=480 V
Electrical Testing: @ Room

Device	Lot ID	Hour	SS	Reject	Remark
IRS2113SPBF	311445.1	1000	80	0	5 FNC_15_15 on bench within spec. Vth_Ls on product mask had a tweak to center this parameter.
	311455.1	1000	80	0	
	311482.1	1000	80	0	

Reliability Test #5 - **High Temperature Storage Life (HTSL) Test:**
Test Duration: 1008 Hours
Test Condition: TJ/A=150 °C
Bias Condition: No bias required
Electrical Testing: @ Room

Device	Lot ID	Hour	SS	Reject	Remark
IRS2113SPBF	311445.1	1000	80	0	

Other Required Test Results:

1. **Resistance to Solder Heat/Wave-Solder:** Test 30 devices from one lot per package/device-vehicle in accordance with JEDEC, JESD22A111 – Passed (reference report: 10268-1-RSH).
2. **Solderability:** Test 10 devices from one lot per package/device-vehicle in accordance with JESD-106-B – Passed (reference family report data: 10303-2-SLDR).
3. The following is the results of ESD tests that were performed by the R/D (Design Center) group.

Human Body Model ESD (100 pF/1500 Ω)	
Device: IRS2113 D/C # 0614 Lot#: 311970 Number of samples: 3 per test model Test date:04/17/6	
Test Pin Combination	Rating
VB to COM, HO	3500 V
All other power pins configuration	2 kV to 4 kV

Machine Model ESD (200 pF/ 0 Ω)	
Device: IRS2113S D/C# 0614 Lot#: 311970 Number of samples: 3 per test model Test date: 04/17/6	
Test Pin Combination	Rating
HIN, LIN, SD to VSS	350 V
All other power pins configuration	200 V to 400 V

4. **LATCH-UP:** The following is the results of the LU test that was performed by the R/D (Design Center) group.

Device: IRS2113S
D/C # 551Q
Lot#: C05AP
Number of samples: 6
Test Date: 01/11/06

	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6
HO > VB	2 A	2 A	2 A	2 A	2 A	2 A
HO < VS	2 A	2 A	2 A	2 A	2 A	2 A
LO > VCC	2 A	2 A	2 A	2 A	2 A	2 A
LO < COM	2 A	2 A	2 A	2 A	2 A	2 A

End of report.