QR-0003:
Reliability Qualification Report for IRS20954SPBF

Date: March 30th, 2006

Qualification Vehicle: IRS20954SPBF in 16L-SOICN package:

Based on the reliability test results, the IRS20954SPBF has passed standard International Rectifier industrial-level qualification with MSL3 at 260 °C peak reflow temperature (PRT).
The handling, packing, shipping and use of the moisture/reflow sensitive surface mount devices need to be per IPC/JEDEC J-STD-033A spec.

Device and Lot Information

Reliability Number	10272-1-2-3/3612A-1
Product/Part #	IRS20954SPBF
Qualification Level	Lead-Free Industrial per COP800-08-Rev00
Silicon Technology	200 V HVIC
Silicon Generation	Gen 5
Wafer Fab	Fab11
Wafer-Lot#	Qual Lot#1 (Lot ID 1): 311425.1 Qual Lot#2 (Lot ID 2): 311456.1 Qual Lot#3 (Lot ID 3): 311461.1
Package	SOICN-16L
Lead Finish Plating	100% Sn
Assembly-Lot#	Qual Lot#1 (Lot ID 1): IC005DB Qual Lot#2 (Lot ID 2): IC1105AC Qual Lot#3 (Lot ID 3): IC1105AI
Moisture Sensitivity Level	MSL3 @ 260 °C Per JEDEC specification JA113 / JEDEC J-STD-020C (Test samples were subjected to preconditioning prior to AC, TC & THB reliability tests, HTB and HTSL samples do not require preconditioning).
Reliability Test Location	IR Temecula, USA

Reliability Test Results:

Samples from three wafer lots and three assembly lots were tested in the following reliability tests to determine typical lifetime performance under industrial level qualification. The tests samples passed AC, TC, THB, HTB and HTSL reliability test requirements.

The Stress Tests Conditions and Results are as follows:

Reliability Test #1 - Autoclave Test:
Test Duration: 96 Hours
Test Condition: +121 °C, 100% RH and 15 PSIG
Bias Condition: None
Electrical Testing: @ Room

Device	Lot ID	Hour	SS	Reject	Remark
IRS20954SPBF	1	96	80	0	
	2	96	80	0	
	3	96	80	0	

Reliability Test #2 - Temperature Cycling:
Test Duration: 1000 Cycles
Test Condition: -55 °C to 150 °C (ΔT=205 °C, Dry-Air to Dry-Air)
Bias Condition: None
Electrical Testing: @ Room

Device	Lot ID	Cycle	SS	Reject	Remark
IRS20954SPBF	1	1000	80	0	
	2	1000	80	0	
	3	1000	80	0	

Reliability Test #3 - Temperature Humidity Bias (THB) Test:
Test Duration: 1000 Hours
Test Condition: 85 °C, 85% RH
Bias Condition: V_{CC}=20 V, V_{DD}=10 V, V_{IN}=5 V, V_B=20 V
Electrical Testing: @ Room

Device	Lot ID	Hour	SS	Reject	Remark
IRS20954SPBF	1	1000	80	0	
	2	1000	80	0	
	3	1000	80	0	

Reliability Test #4 - High Temperature Bias (HTB) Test:
Test Duration: 1008 Hours
Test Condition: T_j=150 °C
Bias Condition: V_{CC}=20 V, V_{DD}=10 V, V_{IN}=5 V, V_{SS}=160 V, V_{BS}=20 V, V_S=160 V
Electrical Testing: @ Room

Device	Lot ID	Hour	SS	Reject	Remark
IRS20954SPBF	1	1000	79	0	
	2	1000	79	0	
	3	1000	80	0	

Reliability Test #5 - **High Temperature Storage Life (HTSL) Test:**
Test Duration: 1008 Hours
Test Condition: TJ/A=150 °C
Bias Condition: No bias required
Electrical Testing: @ Room

Device	Lot ID	Hour	SS	Reject	Remark
IRS20954SPBF	1	1000	80	0	

Other Required Tests Results:

1. **Resistance to Solder Heat/Wave-Solder:** Test 30 devices from one lot per package/device-vehicle in accordance with JEDEC, JESD22A111 – Passed (reference report: 10272-1-RSH).
2. **Solderability:** Test 10 devices from one lot per package/device-vehicle in accordance with JESD-106-B – Passed (reference report: 10272-1-SLDR).
3. **ESD:** The following is the results of ESD tests that were performed by the R/D (Design Center) group.

Human Body Model ESD (100 pF/1500 Ω)	
Device: IRS20954SPBF D/C # 547Q Lot#: C05AC Number of samples: 3 per test model Test date:12/20/05	
Test Pin Combination	Rating
All Pin Combinations	2 kV to 4 kV

Machine Model ESD (200 pF/ 0 Ω)	
Device: IRS20954SPBF D/C# 547Q Lot#: C05AC Number of samples: 3 per test model Test date:12/20/05	
Test Pin Combination	Rating
All Pin Combinations	200 V to 400 V

4. **LATCH-UP:** The following is the results of the LU test that was performed by the R/D (Design Center) group.

Device: IRS20954SPBF
D/C # 547Q
Lot#: C05AC
Number of samples: 6
Test Date: 12/20/05

	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6
HO > VB	2.0 A	2.0 A	2.0 A	2.0 A	2.0 A	2.0 A
HO < VS	2.0 A	2.0 A	2.0 A	2.0 A	2.0 A	2.0 A
LO > VCC	2.0 A	2.0 A	2.0 A	2.0 A	2.0 A	2.0 A
LO < COM	2.0 A	2.0 A	2.0 A	2.0 A	2.0 A	2.0 A

End of report.