Total Ionizing Dose and Single-Event-Effects Test Report

S-Series DC-DC Converter

Revision A
July, 2003

International
IOR Rectifier
HI-REL PRODUCTS

Executive Summary of S-Series Radiation Test Results

The S-Series converters were tested for TID (Total Ionizing Dose) and for Single Event Effects (SEE).

TID

A total of 5 devices each of different model types were tested at McClellan AFB near Sacramento California. Three of the units tested were single output versions and two of the units were dual output versions. Of the single output models the 3.3V, 5V and 15V output models were selected for testing. For the Dual versions, the 5V dual and 15V dual models were selected for testing. All S-Series models of different output voltages are of similar circuit configuration. Differences are magnetic turns ratios, output filtering component values, and compensation circuit values to accommodate the specific output. The outputs of the units were loaded with a resistive load equal to ½ of the rated maximum. The units were irradiated in a dose rate chamber containing 19,200 Curies of Co_{60}. The chamber was set up to provide a dose rate of approximately 1k rad (SiO_2)/min. A screw driven automatic cart was used to position the units relative to the source to obtain the desired dose rate. Tests were conducted in accordance with MIL-STD-883, Method 1019.5, condition B. After radiation exposure the parts were annealed at 100°C for 160 hours.

SEE

Single event testing was performed at Texas A&M University in College Station, Texas. A total of three samples were evaluated. The samples selected were the 3.3V single, 15V single, and 15V dual. The units were biased at full load during irradiation. The parts were irradiated with xenon and gold ions producing LET levels of 47, 60 and 83 MeV·cm^2 / mg.

Conclusion

The S-Series parts passed the irradiation tests. Although not all the S-Series output voltages were tested, the results should be considered applicable to the complete S-Series product line by virtue of their similarity. Parametric changes after (TID) testing were minor. Some disturbances were observed during (SEE) testing however no upsets or latch-up was observed.

1.0 Scope

1.1 This document describes the test procedures, and results from a series of total ionizing dose irradiation exposures (TID) and heavy ion Single Event Effects (SEE) testing of the S-Series converters.

2.0 Applicable Documents

2.1 The following documents of the revision in effect at the time of the writing of this document form a part of this drawing to the extent specified herein. In the event of a conflict between any of these specifications and this document, this document shall take precedence.

2.2 Military Specifications

MIL-PRF-38534	Hybrid Microcircuits, General Specification For
MIL-STD-883	Test Methods and Procedures for Microelectronics

2.3 Advanced Analog Specifications

1-172449	Schematic, S-Series DC/DC, Single Output
1-172512	Schematic, S-Series DC/DC, Dual Output

2.4 Industry Standards

EIA/JESD57	Test Procedures for the Measurement of Single Event Effects in Semiconductor Devices from Heavy Ion Irradiation

3.0 Definitions / Terms

SOW- Statement of Work
SEE- Single Event Effect
LET- Linear Energy Transfer (units are MeV/(mg/cm^2))
TID- Total Ionizing Dose (units are Krads (Si))
DUT- Device Under Test
SCD- Source Control Drawing

4.0 General Information

4.1 The S28XXS uses a switch mode topology to convert a nominal 28-volt DC input into a low voltage DC output. The S28XXS is a single output device providing the following nominal output voltages and currents.

Model Number	Output Voltage/Output Current
S2803R3S	3.3V / 3A
S2805S	5V / 2A
S2812S	12V / 0.83A
S2815S	15V / 0.67A

Table 1. S-Series Single Output Standard models

4.2 The S28XXD uses a switch mode topology to convert a nominal 28-volt DC input into low voltage DC outputs. The S28XXD is a dual output device providing the following nominal output voltages and currents.

Model Number	Output Voltage/Output Current
S2805D	±5V / 1A
S2812D	±12V / 0.42A
S2815D	±15V / 0.33A

Table 2. S-Series Dual Output Standard models

4.3 The S-Series Single and Dual DC/DC Converters are constructed as power hybrids in accordance with MIL-PRF-38534, Level K

5.0 Test Samples

5.1 Sample Selection

Control Samples
- 1 Each S2803R3S - REF S/N 0310130
- 1 Each S2805S - REF S/N 0310103
- 1 Each S2815S - REF S/N 0341108
- 1 Each S2805D - REF S/N 0310105
- 1 Each S2815D - REF S/N 0310103

Total Dose Samples
- 1 Each S2803R3S - S/N 0310131
- 1 Each S2805S - S/N 0310105
- 1 Each S2815S - S/N 0341109
- 1 Each S2805D - S/N 0310101
- Each S2815D - S/N 0310105

Single Events Samples
- 1 Each S2803R3S - S/N 0310101
- 1 Each S2815S - S/N 0341106
- 1 Each S2815D - S/N 0310102

6.0 Total Ionizing Dose (TID) Test

{xe "4.0 Total Ionizing Dose (TID) Test:4.1 Test Objectives and Failure Criteria"} 6.1 TEST OBJECTIVES AND FAILURE CRITERIA

The goal of the TID exposures described herein is to establish that the S-Series hybrid DC/DC converters are capable of withstanding exposure to a steady state TID of greater than 100 kRads (Si) with no significant impairment of performance. Pass / Fail criteria are the electrical test parameters as defined in specification data sheet. The parametric limits as defined are incorporated into the Advanced Analog ATE software used for final acceptance testing.

{xe "4.0 Total Ionizing Dose (TID) Test:4.2 Test Facility and Dosimetry"} 6.2 TEST FACILITY AND DOSIMETRY

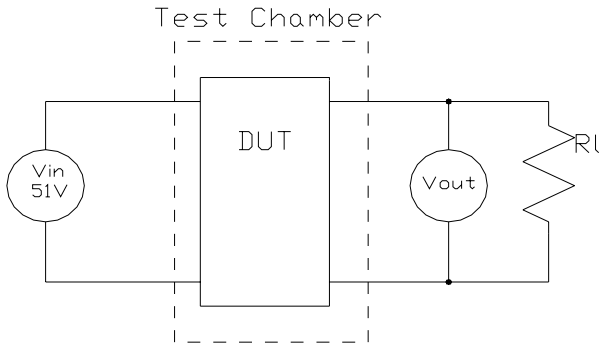
The test samples were irradiated at the McClellan AFB near Sacramento California. This facility uses a gamma ray source. The source element is 19,200 Curies of $Co_{60.}$ The source was setup to provide dose rates approximately 1krad (SiO_2) per minute. Customized ion chamber detectors are used to provide accurate dosimetry (+/- 5%). A screw driven cart drives the DUTs to the desired distance from the source for accurate and repeatable DUT positioning. (See Attached Dosimetry Report)

{xe "4.0 Total Ionizing Dose (TID) Test:4.3 Ionizing Dose Methodology"} 6.3 IONIZING DOSE METHODOLOGY

The total ionizing dose irradiation test sequence was patterned to conform to Method 1019.5 condition B of MIL-STD-883D.

{xe "4.0 Total Ionizing Dose (TID) Test:4.4 Irradiation Procedure"} 6.4 IRRADIATION PROCEDURE

The TID test samples were irradiated during four sessions. During the first session a total of 25krads was accumulated. During the second session the samples were exposed to an additional 25 krads for a total of 50 krads exposure. The third session had 50krads of exposure totaling 100krads. The final session added another 50krads for a total of 150krads exposure. A total of 5 devices consisting of five different models were exposed. The models tested were the 3.3V, 5V, and 15V single outputs and the 5V and 15V dual output DC/DC converters. During exposure the converters were biased with 28 volts nominal input, and loaded on each respective output with ½ of the rated load for that specific output. After the radiation exposure the parts were annealed at 100°C for 160 hours.



1. Vin = 28V
2. Rl is chosen for approximately ½ maximum output power
3. All inputs are common.
4. Input Current for all biased DUTs is monitored in parallel
5. Each converter is monitored for output Voltage
6. Five converters are irradiated at one time

Figure 1, TID Test Schematic

DUTs were mounted to an isoplanar test plate. The plate was positioned relative to the source as to assure uniform exposure of the DUTs. Fixed loads for the biased outputs, and the DUT input power source were coupled to the test plate via cables, and positioned outside the test chamber, thereby keeping the heat load external to the chamber. Nominal conditions during irradiation were ambient temperature and pressure. No heating or cooling other than the cooling provided by the fixturing itself was provided during exposure. The test plate was contained within a lead-aluminum shield to minimize dose rate enhancement effects as required by TM1019.5.

Complete parametric data for the DUTs was recorded for all converters at 0krads, 25krads, 100krads, 150krads, and after 160 hours anneal.

{xe "4.0 Total Ionizing Dose (TID) Test:4.5 Electrical Testing"} 6.5 ELECTRICAL TESTING

Initial, Interim, and Final electrical tests were performed using an Advanced Analog production ATE test setup and software. Tests were performed at room temperature and ambient pressure.

6.6 Total Ionizing Dose (TID) Results and Observations

Complete parametric data for all test samples, at initial and final irradiation levels are given in the appendix. Changes in any of the electrical parameters after TID exposure were minor. The following trends were noted:

1) There is a slight downward trend with increasing exposure for the output voltage set points. After the units were annealed the downward trend was reduced except for 3.3V output were the trend went slightly positive. See Table 3 for summary of output voltage change due to total ionizing dose irradiation.

Model Number	Pre Radiation	25 krads	100 krads	150 krads	Post anneal
S2803.3S	3.31	3.31	3.30	3.29	3.32
S2805S	5.00	5.00	4.97	4.95	5.00
S2815S	15.03	15.02	14.98	14.94	15.02
S2805D	+4.99 -4.99	Not Tested	Not Tested	+4.95 -4.95	+4.99 -4.98
S2815D	+15.00 -15.00	Not Tested	Not Tested	+14.93 -14.93	+14.97 -14.97

Table 3. Output Voltage Change Due to TID Irradiation

2) There was a slight shift upward in the free-running switching frequency (less than 5%) after the units were annealed. This is attributable to slight shifts in the switching thresholds of logic gates used to implement the clock oscillator circuitry.

3) The over-load thresholds shifted slightly lower (approx 5%) with increasing exposure.

4) There was a decrease in the short circuit power dissipation (approx 5%) with increasing exposure.

{xe "7.0 Heavy Ion (SEE) Test"} **7.0 HEAVY ION (SEE) TEST**

{xe "7.0 Heavy Ion (SEE) Test:7.1 Test Objectives"} **7.1 TEST OBJECTIVES**

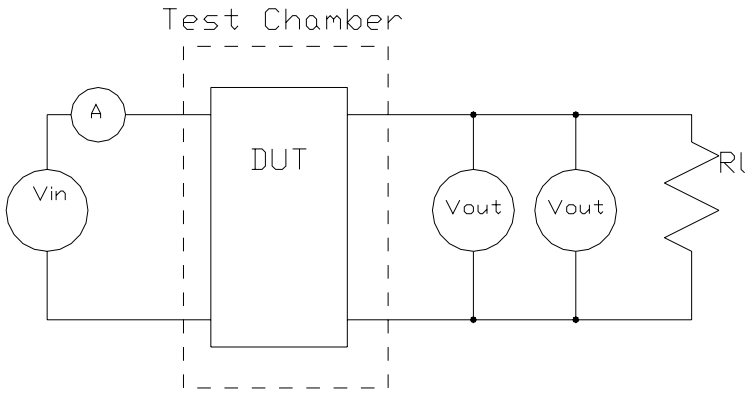
The S-Series DC/DC converters use a combination of bipolar and MOS integrated circuits and discrete devices. The objective of the heavy ion tests is to demonstrate that these DC/DC converters are not susceptible to single event effects (SEE) up to an LET 83 MeV-cm^2/mg.

{xe "7.0 Heavy Ion (SEE) Test:7.2 Test Facility"} **7.2 TEST FACILITY**

Single event testing was performed at Texas A&M University in College Station, Texas. Advanced Analog engineering personnel performed the tests with the assistance of Texas A&M Lab personnel.

{xe "7.0 Heavy Ion (SEE) Test:7.3 Heavy Ion Test Procedure"} **7.3 HEAVY ION TEST PROCEDURE**

The heavy ion exposures were in a vacuum at room temperature and the devices were without lids or covers. Three devices (S2803R3S, S2815S, and S2815D) were exposed while biased with input voltages of 18V, 28V and 40V with each output loaded to approximately 100% of its rated value. Device input current and output voltages were continuously monitored (See Figure 3, SEE Test Schematic and Figure 4, SEE Test and Monitoring Setup). An SEE failure consists of a change in the output voltage greater than 10% of the nominal output or a change in input current of 50% of the steady state input current. Digital counters were used to count the number of instances a failure occurred during a test run. The devices were exposed to Xenon ions with a LETs of 47 MeV-cm^2/mg and 60MeV-cm^2/mg. The devices were also exposed to gold with an LET of 83 MeV-cm^2/mg.



1. Vin = 18, 28, 40V
2. Rl is chosen for approximately maximum output power
3. All inputs are common.
4. Input Current for all biased DUTs is monitored in parallel
5. Each converter is monitored for output Voltage
6. Three converters are irradiated at one time

Figure 2. SEE Test Schematic

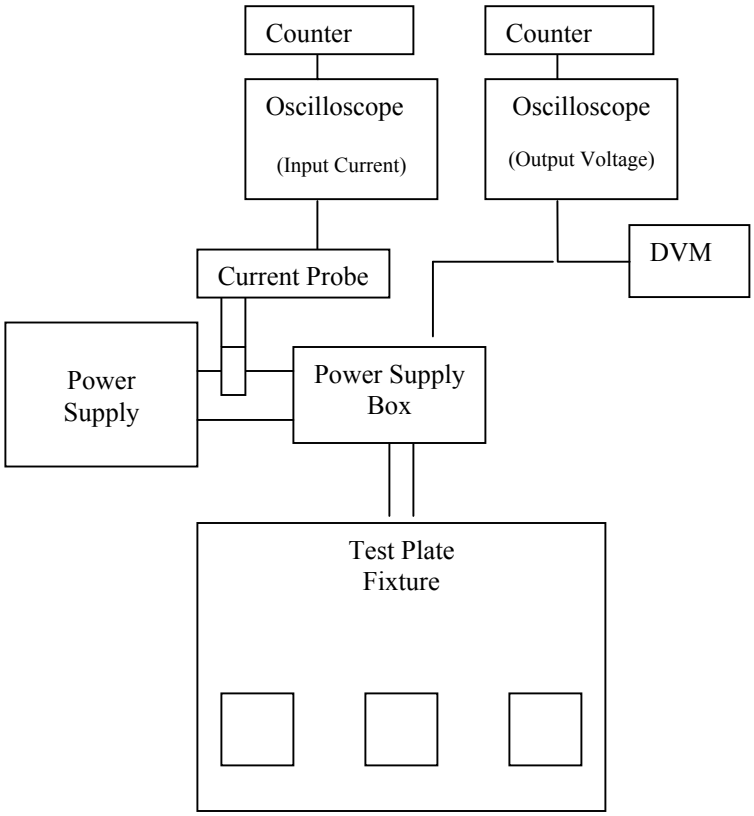


Figure 3, SEE Test and Monitoring Setup

{xe "7.0 Heavy Ion (SEE) Test:7.4 Heavy Ion Test Results"} 7.4 HEAVY ION TEST RESULTS

The converters functioned properly during heavy ion irradiations up to 10^6-ion/cm^2 fluence and LET 83 MeV (Gold) without failures. Table 4 summarizes the SEE testing performed and results.

Date: **6/21/03**
Model **S-Series S2803R3S, S2815S, S2815D**
Facility: **Texas A&M University**

Run #	Ion	LET MeV.cm²/mg	Energy Range MeV	Energy Range µm	Flux #/cm²/sec	Fluence #/cm²	Device Type	S/N	Vin Volts	upsets Vout	pass/ fail
1	Xe	47.3	1934	157	1.00E+04	1.00E+06	S2803R3S	101	18	0	Pass
2	Xe	47.3	1934	157	1.00E+04	1.00E+06	S2803R3S	101	28	0	Pass
3	Xe	47.3	1934	157	1.00E+04	1.00E+06	S2803R3S	101	40	0	Pass
7	Xe	47.3	1934	157	1.00E+04	1.00E+06	S2815S	106	18	0	Pass
8	Xe	47.3	1934	157	1.00E+04	1.00E+06	S2815S	106	28	0	Pass
9	Xe	47.3	1934	157	1.00E+04	1.00E+06	S2815S	106	40	0	Pass
12	Xe	47.3	1934	157	1.00E+04	1.00E+06	S2815D	102	18	0	Pass
13	Xe	47.3	1934	157	1.00E+04	1.00E+06	S2815D	102	28	0	Pass
14	Xe	47.3	1934	157	1.00E+04	1.00E+06	S2815D	102	40	0	Pass
35	Au	83	2574	135	1.00E+04	1.00E+06	S2803R3S	101	18	0	Pass
36	Au	83	2574	135	1.00E+04	1.00E+06	S2803R3S	101	28	0	Pass
37	Au	83	2574	135	1.00E+04	1.00E+06	S2803R3S	101	40	0	Pass
40	Au	83	2574	135	1.00E+04	1.00E+06	S2815S	106	18	0	Pass
41	Au	83	2574	135	1.00E+04	1.00E+06	S2815S	106	28	0	Pass
42	Au	83	2574	135	1.00E+04	1.00E+06	S2815S	106	40	0	Pass
45	Au	83	2574	135	1.00E+04	1.00E+06	S2815D	102	18	0	Pass
46	Au	83	2574	135	1.00E+04	1.00E+06	S2815D	102	28	0	Pass
47	Au	83	2574	135	1.00E+04	1.00E+06	S2815D	102	40	0	Pass

For All data Angle = 0° Beam Diameter = 1.75 in X 1.75 in

Table 4. SEE Testing Run Table

{xe "7.0 Heavy Ion (SEE) Test:7.5 Conclusions"} 7.5 CONCLUSIONS

The S-Series DC/DC converters do not fail due to SEE up to an LET of 83 MeV-cm²/mg. Similar performance can be expected from all S-Series models due to similarity of design.

7.6 Single Event Effects (SEE) Results and Observations

Table 4 shows the results of the SEE tests perfromed on 3 samples of S-Series converters. The tests were run with 3 DUTs mounted to the test plate simultaneously. During testing only the DUT being irradiated was biased and loaded. Test plate temperature was monitored throughout the duration of testing. Prior to commencement and following SEE testing full parametric data was taken on the test samples. This data is shown in the Appendix C. Monitoring of input current resulted in no value added to testing results. This was due to the trigger threshold being set too high in order to avoid false triggering. In future SEE testing the input current will not be monitored. Although the units tested passed the SEE testing, some disturbances were observed on the output at different LET levels. The table below summarizes the disturbances and occurrences for the S-Series converters tested. Typical disturbance waveforms are shown in Figures 3, 4 and 5.

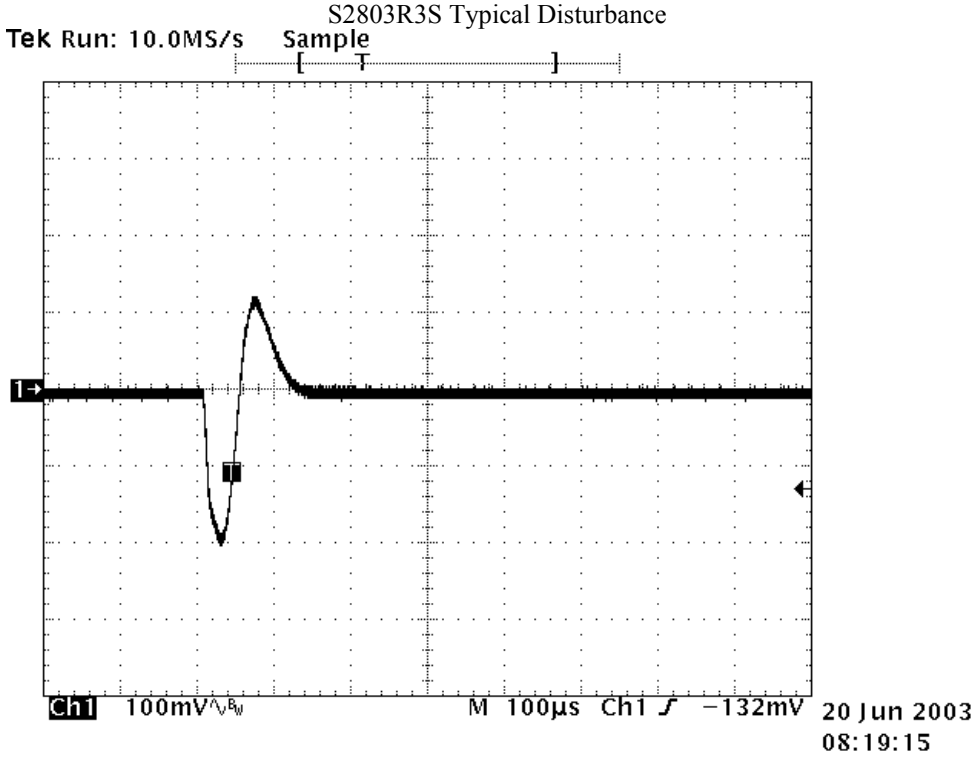
Model number	LET	Run Number	Trigger Level	Occurrences
S2803R3S	47.3	4	-165mV	431
S2803R3S	60	29	-165mV	7
S2803R3S	83	39	-165mV	1275
S2815S	47.3	11	-750mV	0
S2815S	60	31	-750mV	0
S2815S	83	42	-750mV	0
S2815D	47.3	17	-520mV	9
S2815D	60	33	-520mV	11
S2815D	83	49	-520mV	27

Run #	Ion	LET $MeV.cm^2/mg$	Energy Range MeV	μm	Flux $\#/cm^2/sec$	Fluence $\#/cm^2$	Device Type	S/N	Vin Volts
4	Xe	47.3	1934	157	1.0E+04	1.0E+06	S2803R3S	101	40
9	Xe	47.3	1934	157	1.0E+04	1.0E+06	S2815S	106	40
17	Xe	47.3	1934	157	1.0E+04	1.0E+06	S2815D	102	40
29	Xe	60	738	60	1.0E+04	1.0E+06	S2803R3S	101	40
31	Xe	60	738	60	1.0E+04	1.0E+06	S2815S	106	40
33	Xe	60	738	60	1.0E+04	1.0E+06	S2815D	102	40
39	Au	83	2574	135	1.0E+04	1. 0E+06	S2803R3S	101	40
42	Au	83	2574	135	1.0E+04	1.0E+06	S2815S	106	40
49	Au	83	2574	135	1.0E+04	1.0E+06	S2815D	102	40

For All data Angle = 0° Beam Diameter = 1.75 in X 1.75 in

Table. 5. S-Series Disturbances for given trigger level

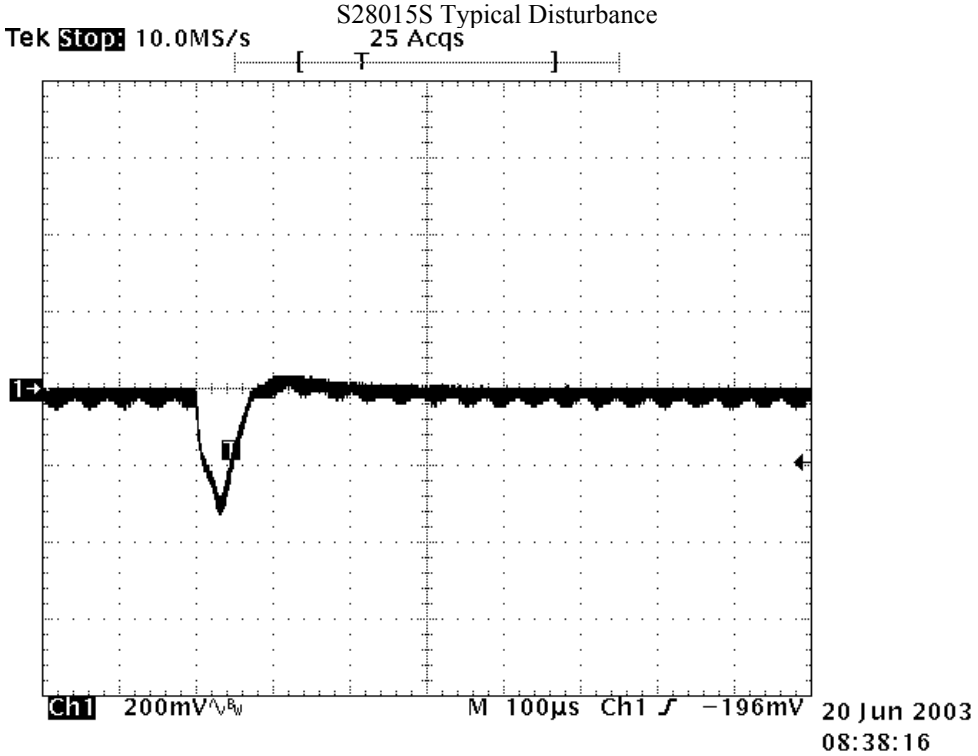
S2803R3S Typical Disturbance



Vin = 40V, Full Load

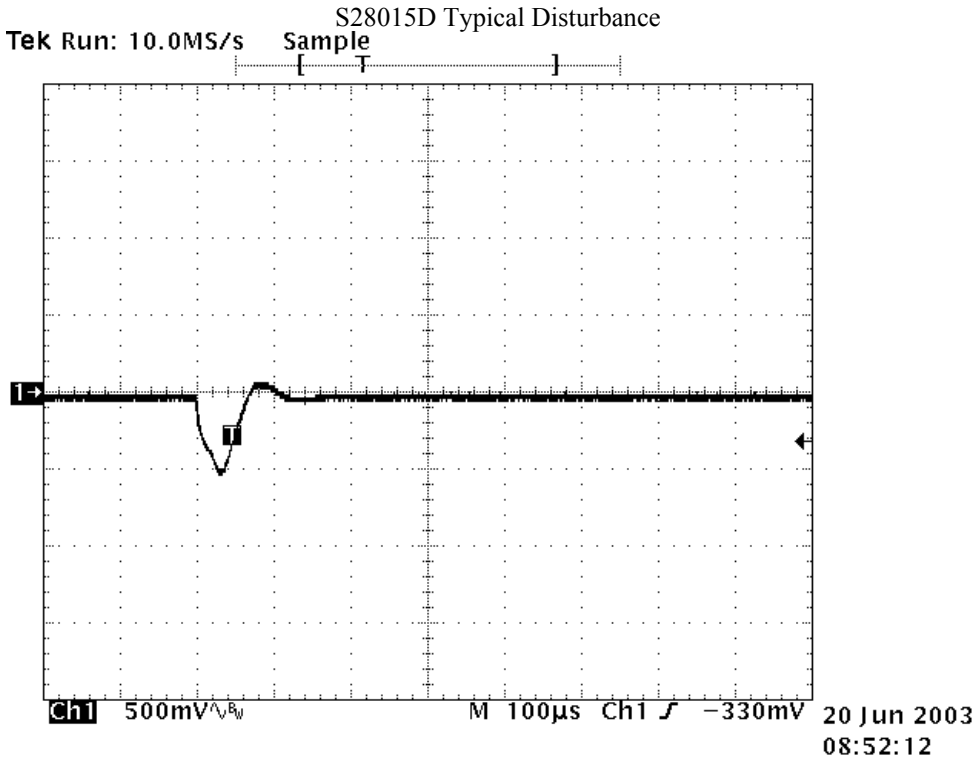
Figure 3. Typical Disturbance waveform for S2803R3S

S28015S Typical Disturbance



Vin = 40V, Full Load

Figure 4. Typical Disturbance waveform for S2815S



Vin = 40V, Full Load

Figure 5. Typical Disturbance waveform for S2815D

Appendix A

TEST CERTIFICATE
(SUPPLEMENTAL)

Defense Microelectronics Activity
Science and Engineering Gamma Irradiation Test Lab
DMEA/METI
4234 54th Street
McClellan, CA 95652

Accreditation Certificate Number: 1691-01

This laboratory is accredited by the American Association for Laboratory Accreditation (A2LA) and the dosimetry reported in this test certificate has been determined in accordance with the laboratory's terms of accreditation.
The results contained herein relate only to the items tested.
This certificate may not be reproduced, except in full, without the approval of this laboratory.

Date: 2003-06-10 **Test Certificate #:** 2003-NRC-011 **Total Pages (except cover):** 1

REQUEST FOR AND RESULTS OF TESTS

PAGE NO.	NO. OF PAGES
1	1

SECTION A - REQUEST FOR TEST

1. TO: *(Include ZIP Code)*	2. FROM: *(Include ZIP Code)*
Defense Microelectronics Activity DMEA/METI 4234 54th Street McClellan, CA 95652-2100	Arturo Arroyo Advanced Analog / International Rectifier 2270 Martin Ave Santa Clara, CA 95050 Phone: (408) 450-5807 FAX: (408) 988-2702 Email: arturo_arroyo@irf.com
3. PRIME CONTRACTOR AND ADDRESS *(Include ZIP Code)* EagleST 3778 Eagle St. San Diego, CA 92103 CONTRACT NUMBER CRADA 03-05	4. MANUFACTURING PLANT NAME AND ADDRESS *(Include ZIP Code)* P.O. NUMBER Task Request 001

5. END ITEM AND/OR PROJECT	6. SAMPLE NUMBER	7. LOT NO.	8. REASON FOR SUBMITTAL	9. DATE SUBMITTED
S-series DC/DC Converters MEE DC/DC Converter	5, 1	Engr. models	Characterization MIL-STD-883, test method 1019.5, Condition B	2003-06-03

10. MATERIAL TO BE TESTED	10a. QUANTITY SUBMITTED	11. QUANTITY REPRESENTED	12. SPEC. & AMEND AND/OR DRAWING NO. & REV. FOR SAMPLE & DATE
S-series DC/DC Converters MEE DC/DC Converter	5,1	N/A	s-series data sheet

13. PURCHASED FROM OR SOURCE	14. SHIPMENT METHOD	15. DATE SAMPLED AND SUBMITTED BY
Same as block 2.	N/A	N/A

16. REMARKS AND/OR SPECIAL INSTRUCTIONS AND/OR WAIVERS.

Dose Rate: <1 Mrad(SiO2)/hr Irradiation Steps: 10 Type of Test: Customer-Performed

Total Dose: 150 krad(SiO2) Requested Test Start Date: 2003-06-05 Dimensions: 30.5cm x 30.5cm (12" x 12")

TID irradiation shall be performed to accommodate eight externally biased DUTs mounted on an isoplanar test plate assuring uniform dose rates to each DUT. This test plate provides a thermal path to minimize dissipation induced heat rise of the 3 biased DUTs. Fixed loads for each biased DUT shall be coupled with a cable exiting the chamber, thereby keeping the heat load external to the test chamber. The nominal conditions during the irradiation shall be ambient temperature and pressure; no applied cooling or heating shall be introduced beyond what is already described. The test plate shall be contained within or behind a lead-aluminum shield to minimize dose enhancement effects, as required by TM1019.5. Group A electrical test shall be performed & recorded by the customer (onsite) at 0 rads, 10Krads, 50Krads, 100Krads, and 150Krads.

Experiment #: 2003-NRC-011 DMEA Approval:

17. SEND REPORT OF TEST TO
Individual identified in block 2

SECTION B - RESULTS OF TEST *(Continue on plain white paper if more space is required)*

1. DATE SAMPLE RECEIVED	2. DATE RESULTS REPORTED	3. LAB REPORT NUMBER
N/A	2003-06-10	N/A

4. TEST PERFORMED	RESULTS OF TEST	SAMPLE RESULT	REQUIREMENTS
2003-06-05 11:23 to 11:48:40.2	25.47 krad(SiO2)* at 992.4 rad(SiO2)/min		
2003-06-05 13:05 to 13:30:40.2	25.47 krad(SiO2)* at 992.3 rad(SiO2)/min		
2003-06-05 13:38 to 14:29:20.4	50.95 krad(SiO2)* at 992.3 rad(SiO2)/min		
2003-06-05 15:09 to 16:00:20.4	50.95 krad(SiO2)* at 992.3 rad(SiO2)/min		

* +/-7.78% at a 95% confidence

DATE	TYPED NAME AND TITLE OF PERSON CONDUCTING TEST	SIGNATURE
2003-06-10	Gary Waldsmith, Facility Supervisor	
2003-06-10	David Pentrack, Technical Manager	

DD FORM 1222, FEB 62 (EF) REPLACES DD FORM 1222, 1 JUL 58, WHICH IS OBSOLETE.

Appendix B

(TID)
Pre, and Final
Parametric Data

```
Filename:      RESULTS\0310S03S.CH
Date:          Wednesday  June 4, 2003
Time:          16:27:58
Test:           FINAL
Program:      FDP 172xxx  Engineering Evaluation Rev. A
Lot Number:    0310
Serial Number: 131
Operator:      ANT
Model:         S2803.3SF/CH
Test Temp:     +25  deg C
```

TEST	RESULT	LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	3.31 V	3.23	3.37	PASS
Line regulation 10% load	0.010 %	-5.000	5.000	PASS
Line regulation Half load	0.014 %	-5.000	5.000	PASS
Line regulation Full load	0.013 %	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.267 %	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.264 %	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.270 %	-1.000	1.000	PASS
Input current NO LOAD	18.63 mA	5.00	60.00	PASS
Input Current With Inhibit	2.66 mA	0.00	8.00	PASS
Output ripple Vin = 18 V	5.26 mV	0.00	35.00	PASS
Output ripple Vin = 28 V	5.17 mV	0.00	35.00	PASS
Output ripple Vin = 40 V	4.99 mV	0.00	35.00	PASS
Input ripple current	9.18 mA	0.00	50.00	PASS
Frequency	521 KHz	425	575	PASS
Efficiency	77.53 %	68.00	90.00	PASS
OvLd TP. Vin = 28 V	4.130 A	3.330	4.240	PASS
ShortCircuit PD.	6.550 W	0.000	9.000	PASS
HTF transient	-99 mV	-300	300	PASS
HTF recovery time	51 uS	0	200	PASS
FTH transient	94 mV	-300	300	PASS
FTH recovery time	22 uS	0	200	PASS
TO 10%Ld overshoot	235.3 mV	2.0	500.0	PASS
TO 10%Ld Delay time	5.6 mS	0.0	10.0	PASS
TOFL overshoot	235.3 mV	0.0	500.0	PASS
TOFL delay time	5.6 mS	0.0	10.0	PASS
Post Test voltage accuracy	3.31 V	3.23	3.37	PASS

PASSED

Filename: RESULTS\0310S03S.CH
Date: Friday June 13, 2003
Time: 15:25:07
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0310
Serial Number: 131
Operator: aa
Model: S2803.3SF/CH
Test Temp: +25 deg C

TEST	RESULT		LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	3.32	V	3.23	3.37	PASS
Line regulation 10% load	0.003	%	-5.000	5.000	PASS
Line regulation Half load	0.001	%	-5.000	5.000	PASS
Line regulation Full load	0.001	%	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.270	%	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.273	%	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.273	%	-1.000	1.000	PASS
Input current NO LOAD	18.29	mA	5.00	60.00	PASS
Input Current With Inhibit	2.67	mA	0.00	8.00	PASS
Output ripple Vin = 18 V	14.87	mV	0.00	35.00	PASS
Output ripple Vin = 28 V	4.57	mV	0.00	35.00	PASS
Output ripple Vin = 40 V	4.58	mV	0.00	35.00	PASS
Input ripple current	10.31	mA	0.00	50.00	PASS
Frequency	549	KHz	425	575	PASS
Efficiency	77.38	%	68.00	90.00	PASS
OvLd TP. Vin = 28 V	3.930	A	3.330	4.240	PASS
ShortCircuit PD.	6.242	W	0.000	9.000	PASS
HTF transient	-96	mV	-300	300	PASS
HTF recovery time	26	uS	0	200	PASS
FTH transient	92	mV	-300	300	PASS
FTH recovery time	20	uS	0	200	PASS
TO 10%Ld overshoot	235.3	mV	2.0	500.0	PASS
TO 10%Ld Delay time	4.5	mS	0.0	10.0	PASS
TOFL overshoot	235.3	mV	0.0	500.0	PASS
TOFL delay time	4.5	mS	0.0	10.0	PASS
Post Test voltage accuracy	3.32	V	3.23	3.37	PASS

PASSED

Filename: RESULTS\0310S05S.CH
Date: Wednesday June 4, 2003
Time: 16:35:56
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0310
Serial Number: 105
Operator: ANT
Model: S2805SF/CH
Test Temp: +25 deg C

TEST	RESULT		LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	5.00	V	4.90	5.10	PASS
Line regulation 10% load	0.005	%	-5.000	5.000	PASS
Line regulation Half load	0.002	%	-5.000	5.000	PASS
Line regulation Full load	0.004	%	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.115	%	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.119	%	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.116	%	-1.000	1.000	PASS
Input current NO LOAD	20.45	mA	5.00	50.00	PASS
Input Current With Inhibit	2.68	mA	0.00	8.00	PASS
Output ripple Vin = 18 V	9.17	mV	0.00	50.00	PASS
Output ripple Vin = 28 V	3.54	mV	0.00	50.00	PASS
Output ripple Vin = 40 V	3.69	mV	0.00	50.00	PASS
Input ripple current	8.85	mA	0.00	50.00	PASS
Frequency	523	KHz	425	575	PASS
Efficiency	79.10	%	75.00	90.00	PASS
OvLd TP. Vin = 28 V	2.680	A	2.200	2.800	PASS
ShortCircuit PD.	5.463	W	0.000	9.000	PASS
HTF transient	-87	mV	-300	300	PASS
HTF recovery time	26	uS	0	200	PASS
FTH transient	73	mV	-300	300	PASS
FTH recovery time	12	uS	0	200	PASS
TO 10%Ld overshoot	313.7	mV	2.0	500.0	PASS
TO 10%Ld Delay time	6.0	mS	0.0	10.0	PASS
TOFL overshoot	274.5	mV	0.0	500.0	PASS
TOFL delay time	6.0	mS	0.0	10.0	PASS
Post Test voltage accuracy	5.01	V	4.90	5.10	PASS

PASSED

Filename: RESULTS\0310S05S.CH
Date: Friday June 13, 2003
Time: 15:36:35
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0310
Serial Number: 105
Operator: aa
Model: S2805SF/CH
Test Temp: +25 deg C

TEST	RESULT		LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	5.00	V	4.90	5.10	PASS
Line regulation 10% load	0.005	%	-5.000	5.000	PASS
Line regulation Half load	0.004	%	-5.000	5.000	PASS
Line regulation Full load	0.003	%	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.118	%	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.118	%	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.121	%	-1.000	1.000	PASS
Input current NO LOAD	20.59	mA	5.00	50.00	PASS
Input Current With Inhibit	2.67	mA	0.00	8.00	PASS
Output ripple Vin = 18 V	3.35	mV	0.00	50.00	PASS
Output ripple Vin = 28 V	3.10	mV	0.00	50.00	PASS
Output ripple Vin = 40 V	3.30	mV	0.00	50.00	PASS
Input ripple current	9.88	mA	0.00	50.00	PASS
Frequency	550	KHz	425	575	PASS
Efficiency	78.87	%	75.00	90.00	PASS
OvLd TP. Vin = 28 V	2.560	A	2.200	2.800	PASS
ShortCircuit PD.	5.150	W	0.000	9.000	PASS
HTF transient	-78	mV	-300	300	PASS
HTF recovery time	22	uS	0	200	PASS
FTH transient	71	mV	-300	300	PASS
FTH recovery time	11	uS	0	200	PASS
TO 10%Ld overshoot	352.9	mV	2.0	500.0	PASS
TO 10%Ld Delay time	4.8	mS	0.0	10.0	PASS
TOFL overshoot	313.7	mV	0.0	500.0	PASS
TOFL delay time	4.8	mS	0.0	10.0	PASS
Post Test voltage accuracy	5.00	V	4.90	5.10	PASS

PASSED

Filename: RESULTS\0341S15S.CH
Date: Wednesday June 4, 2003
Time: 16:44:56
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0341
Serial Number: 109
Operator: ANT
Model: S2815SF/CH
Test Temp: +25 deg C

TEST	RESULT	LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	15.03 V	14.70	15.30	PASS
Line regulation 10% load	0.008 %	-5.000	5.000	PASS
Line regulation Half load	0.008 %	-5.000	5.000	PASS
Line regulation Full load	0.007 %	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.016 %	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.014 %	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.014 %	-1.000	1.000	PASS
Input current NO LOAD	36.95 mA	5.00	80.00	PASS
Input Current With Inhibit	2.70 mA	0.00	8.00	PASS
Output ripple Vin = 18 V	15.45 mV	0.00	80.00	PASS
Output ripple Vin = 28 V	3.00 mV	0.00	80.00	PASS
Output ripple Vin = 40 V	3.50 mV	0.00	80.00	PASS
Input ripple current	9.47 mA	0.00	50.00	PASS
Frequency	523 KHz	425	575	PASS
Efficiency	81.56 %	78.00	90.00	PASS
OvLd TP. Vin = 28 V	0.967 A	0.730	0.980	PASS
ShortCircuit PD.	4.898 W	0.000	9.000	PASS
HTF transient	-67 mV	-300	300	PASS
HTF recovery time	0 uS	0	200	PASS
FTH transient	61 mV	-300	300	PASS
FTH recovery time	0 uS	0	200	PASS
TO 10%Ld overshoot	1254.9 mV	2.0	1500.0	PASS
TO 10%Ld Delay time	6.5 mS	0.0	10.0	PASS
TOFL overshoot	1019.6 mV	0.0	1500.0	PASS
TOFL delay time	6.4 mS	0.0	10.0	PASS
Post Test voltage accuracy	15.03 V	14.70	15.30	PASS

PASSED

Filename: RESULTS\0341S15S.CH
Date: Friday June 13, 2003
Time: 15:57:08
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0341
Serial Number: 109
Operator: aa
Model: S2815SF/CH
Test Temp: +25 deg C

TEST	RESULT	LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	15.02 V	14.70	15.30	PASS
Line regulation 10% load	0.009 %	-5.000	5.000	PASS
Line regulation Half load	0.008 %	-5.000	5.000	PASS
Line regulation Full load	0.008 %	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.016 %	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.015 %	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.015 %	-1.000	1.000	PASS
Input current NO LOAD	37.54 mA	5.00	80.00	PASS
Input Current With Inhibit	2.67 mA	0.00	8.00	PASS
Output ripple Vin = 18 V	2.32 mV	0.00	80.00	PASS
Output ripple Vin = 28 V	2.73 mV	0.00	80.00	PASS
Output ripple Vin = 40 V	3.33 mV	0.00	80.00	PASS
Input ripple current	10.61 mA	0.00	50.00	PASS
Frequency	546 KHz	425	575	PASS
Efficiency	81.37 %	78.00	90.00	PASS
OvLd TP. Vin = 28 V	0.907 A	0.730	0.980	PASS
ShortCircuit PD.	4.686 W	0.000	9.000	PASS
HTF transient	-64 mV	-300	300	PASS
HTF recovery time	0 uS	0	200	PASS
FTH transient	60 mV	-300	300	PASS
FTH recovery time	0 uS	0	200	PASS
TO 10%Ld overshoot	1333.3 mV	2.0	1500.0	PASS
TO 10%Ld Delay time	5.4 mS	0.0	10.0	PASS
TOFL overshoot	1098.0 mV	0.0	1500.0	PASS
TOFL delay time	5.7 mS	0.0	10.0	PASS
Post Test voltage accuracy	15.01 V	14.70	15.30	PASS

PASSED

Filename: RESULTS\0310S05D.CH
Date: Tuesday June 3, 2003
Time: 18:34:23
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0310
Serial Number: 101
Operator: atu
Model: S2805DF/CH
Test Temp: +25 deg C

TEST	RESULT		LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	4.99	V	4.90	5.10	PASS
Neg Output voltage accuracy	4.99	V	4.90	5.10	PASS
Line regulation 10% load	0.007	%	-5.000	5.000	PASS
Line regulation Half load	0.006	%	-5.000	5.000	PASS
Line regulation Full load	0.006	%	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.041	%	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.041	%	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.041	%	-1.000	1.000	PASS
Pos Cross regulation Vin = 18 V	1.96	%	-5.00	5.00	PASS
Pos Cross regulation Vin = 28 V	1.84	%	-5.00	5.00	PASS
Pos Cross regulation Vin = 40 V	1.88	%	-5.00	5.00	PASS
Neg Cross regulation Vin = 18 V	-1.94	%	-5.00	5.00	PASS
Neg Cross regulation Vin = 28 V	-1.85	%	-5.00	5.00	PASS
Neg Cross regulation Vin = 40 V	-1.88	%	-5.00	5.00	PASS
Input current NO LOAD	20.32	mA	5.00	80.00	PASS
Input Current With Inhibit	2.70	mA	0.00	8.00	PASS
Output ripple Vin = 18 V	16.69	mV	0.00	80.00	PASS
Output ripple Vin = 28 V	20.86	mV	0.00	80.00	PASS
Output ripple Vin = 40 V	22.93	mV	0.00	80.00	PASS
Neg Output ripple Vin = 18 V	12.23	mV	0.00	80.00	PASS
Neg Output ripple Vin = 28 V	15.48	mV	0.00	80.00	PASS
Neg Output ripple Vin = 40 V	17.26	mV	0.00	80.00	PASS
Input ripple current	9.43	mA	0.00	50.00	PASS
Frequency	521	KHz	425	575	PASS
Efficiency	79.91	%	77.00	90.00	PASS
OvLd TP. Vin = 28 V	1.430	A	1.100	1.500	PASS
ShortCircuit PD.	6.839	W	0.000	9.000	PASS
Neg ShortCircuit PD.	7.197	W	0.000	9.000	PASS
HTF transient	-82	mV	-300	300	PASS
HTF recovery time	23	uS	0	200	PASS
Neg HTF transient	0	mV	-300	300	PASS
Neg HTF recovery time	0	uS	0	200	PASS
FTH transient	64	mV	-300	300	PASS
FTH recovery time	14	uS	0	200	PASS
Neg FTH transient	-61	mV	-300	300	PASS
Neg FTH recovery time	13	uS	0	200	PASS
TO 10%Ld overshoot	274.5	mV	2.0	500.0	PASS
TO 10%Ld Delay time	6.3	mS	0.0	10.0	PASS
Neg TO 10%Ld overshoot	313.7	mV	2.0	500.0	PASS
Neg TO 10%Ld Delay time	6.3	mS	0.0	10.0	PASS
TOFL overshoot	274.5	mV	0.0	500.0	PASS
TOFL delay time	6.3	mS	0.0	10.0	PASS
Neg TOFL overshoot	274.5	mV	0.0	500.0	PASS
Neg TOFL delay time	6.3	mS	0.0	10.0	PASS
Post Test voltage accuracy	4.99	V	4.90	5.10	PASS
Neg Post Test voltage accuracy	4.98	V	4.90	5.10	PASS

PASSED

Filename: RESULTS\0310S05D.CH
Date: Friday June 13, 2003
Time: 18:15:31
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0310
Serial Number: 101
Operator: aa
Model: S2805DF/CH
Test Temp: +25 deg C

TEST	RESULT		LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	4.99	V	4.90	5.10	PASS
Neg Output voltage accuracy	4.98	V	4.90	5.10	PASS
Line regulation 10% load	0.006	%	-5.000	5.000	PASS
Line regulation Half load	0.007	%	-5.000	5.000	PASS
Line regulation Full load	0.007	%	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.041	%	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.041	%	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.042	%	-1.000	1.000	PASS
Pos Cross regulation Vin = 18 V	1.98	%	-5.00	5.00	PASS
Pos Cross regulation Vin = 28 V	1.84	%	-5.00	5.00	PASS
Pos Cross regulation Vin = 40 V	1.86	%	-5.00	5.00	PASS
Neg Cross regulation Vin = 18 V	-1.92	%	-5.00	5.00	PASS
Neg Cross regulation Vin = 28 V	-1.83	%	-5.00	5.00	PASS
Neg Cross regulation Vin = 40 V	-1.86	%	-5.00	5.00	PASS
Input current NO LOAD	18.41	mA	5.00	80.00	PASS
Input Current With Inhibit	2.73	mA	0.00	8.00	PASS
Output ripple Vin = 18 V	21.02	mV	0.00	80.00	PASS
Output ripple Vin = 28 V	20.19	mV	0.00	80.00	PASS
Output ripple Vin = 40 V	22.00	mV	0.00	80.00	PASS
Neg Output ripple Vin = 18 V	19.05	mV	0.00	80.00	PASS
Neg Output ripple Vin = 28 V	15.57	mV	0.00	80.00	PASS
Neg Output ripple Vin = 40 V	17.37	mV	0.00	80.00	PASS
Input ripple current	10.73	mA	0.00	50.00	PASS
Frequency	546	KHz	425	575	PASS
Efficiency	79.67	%	77.00	90.00	PASS
OvLd TP. Vin = 28 V	1.390	A	1.100	1.500	PASS
ShortCircuit PD.	5.830	W	0.000	9.000	PASS
Neg ShortCircuit PD.	6.077	W	0.000	9.000	PASS
HTF transient	-78	mV	-300	300	PASS
HTF recovery time	20	uS	0	200	PASS
Neg HTF transient	0	mV	-300	300	PASS
Neg HTF recovery time	0	uS	0	200	PASS
FTH transient	59	mV	-300	300	PASS
FTH recovery time	12	uS	0	200	PASS
Neg FTH transient	-63	mV	-300	300	PASS
Neg FTH recovery time	13	uS	0	200	PASS
TO 10%Ld overshoot	274.5	mV	2.0	500.0	PASS
TO 10%Ld Delay time	5.3	mS	0.0	10.0	PASS
Neg TO 10%Ld overshoot	274.5	mV	2.0	500.0	PASS
Neg TO 10%Ld Delay time	5.3	mS	0.0	10.0	PASS
TOFL overshoot	235.3	mV	0.0	500.0	PASS
TOFL delay time	5.2	mS	0.0	10.0	PASS
Neg TOFL overshoot	196.1	mV	0.0	500.0	PASS
Neg TOFL delay time	5.2	mS	0.0	10.0	PASS
Post Test voltage accuracy	4.99	V	4.90	5.10	PASS
Neg Post Test voltage accuracy	4.98	V	4.90	5.10	PASS

PASSED

Filename: RESULTS\0310S15D.CH
Date: Tuesday June 3, 2003
Time: 18:56:11
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0310
Serial Number: 105
Operator: atu
Model: S2815DF/CH
Test Temp: +25 deg C

TEST	RESULT		LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	15.00	V	14.70	15.30	PASS
Neg Output voltage accuracy	15.00	V	14.70	15.30	PASS
Line regulation 10% load	0.015	%	-5.000	5.000	PASS
Line regulation Half load	0.016	%	-5.000	5.000	PASS
Line regulation Full load	0.016	%	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.007	%	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.007	%	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.008	%	-1.000	1.000	PASS
Pos Cross regulation Vin = 18 V	0.81	%	-3.00	3.00	PASS
Pos Cross regulation Vin = 28 V	0.66	%	-3.00	3.00	PASS
Pos Cross regulation Vin = 40 V	0.63	%	-3.00	3.00	PASS
Neg Cross regulation Vin = 18 V	-0.89	%	-3.00	3.00	PASS
Neg Cross regulation Vin = 28 V	-0.73	%	-3.00	3.00	PASS
Neg Cross regulation Vin = 40 V	-0.68	%	-3.00	3.00	PASS
Input current NO LOAD	40.49	mA	5.00	80.00	PASS
Input Current With Inhibit	2.70	mA	0.00	8.00	PASS
Output ripple Vin = 18 V	44.03	mV	0.00	80.00	PASS
Output ripple Vin = 28 V	16.06	mV	0.00	80.00	PASS
Output ripple Vin = 40 V	17.07	mV	0.00	80.00	PASS
Neg Output ripple Vin = 18 V	16.97	mV	0.00	80.00	PASS
Neg Output ripple Vin = 28 V	19.17	mV	0.00	80.00	PASS
Neg Output ripple Vin = 40 V	20.40	mV	0.00	80.00	PASS
Input ripple current	9.48	mA	0.00	50.00	PASS
Frequency	526	KHz	425	575	PASS
Efficiency	77.96	%	76.00	90.00	PASS
OvLd TP. Vin = 28 V	0.533	A	0.370	0.550	PASS
ShortCircuit PD.	5.771	W	0.000	9.000	PASS
Neg ShortCircuit PD.	5.742	W	0.000	9.000	PASS
HTF transient	-68	mV	-300	300	PASS
HTF recovery time	0	uS	0	200	PASS
Neg HTF transient	0	mV	-300	300	PASS
Neg HTF recovery time	0	uS	0	200	PASS
FTH transient	60	mV	-300	300	PASS
FTH recovery time	0	uS	0	200	PASS
Neg FTH transient	-69	mV	-300	300	PASS
Neg FTH recovery time	0	uS	0	200	PASS
TO 10%Ld overshoot	705.9	mV	2.0	1500.0	PASS
TO 10%Ld Delay time	6.1	mS	0.0	10.0	PASS
Neg TO 10%Ld overshoot	784.3	mV	2.0	1500.0	PASS
Neg TO 10%Ld Delay time	6.2	mS	0.0	10.0	PASS
TOFL overshoot	784.3	mV	0.0	1500.0	PASS
TOFL delay time	6.2	mS	0.0	10.0	PASS
Neg TOFL overshoot	784.3	mV	0.0	1500.0	PASS
Neg TOFL delay time	6.2	mS	0.0	10.0	PASS
Post Test voltage accuracy	14.99	V	14.70	15.30	PASS
Neg Post Test voltage accuracy	14.98	V	14.70	15.30	PASS

PASSED

Filename: RESULTS\0310S15D.CH
Date: Friday June 13, 2003
Time: 18:28:26
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0310
Serial Number: 105
Operator: aa
Model: S2815DF/CH
Test Temp: +25 deg C

TEST	RESULT		LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	14.97	V	14.70	15.30	PASS
Neg Output voltage accuracy	14.97	V	14.70	15.30	PASS
Line regulation 10% load	0.017	%	-5.000	5.000	PASS
Line regulation Half load	0.016	%	-5.000	5.000	PASS
Line regulation Full load	0.015	%	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.008	%	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.008	%	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.006	%	-1.000	1.000	PASS
Pos Cross regulation Vin = 18 V	0.79	%	-3.00	3.00	PASS
Pos Cross regulation Vin = 28 V	0.66	%	-3.00	3.00	PASS
Pos Cross regulation Vin = 40 V	0.63	%	-3.00	3.00	PASS
Neg Cross regulation Vin = 18 V	-0.86	%	-3.00	3.00	PASS
Neg Cross regulation Vin = 28 V	-0.73	%	-3.00	3.00	PASS
Neg Cross regulation Vin = 40 V	-0.68	%	-3.00	3.00	PASS
Input current NO LOAD	37.33	mA	5.00	80.00	PASS
Input Current With Inhibit	2.78	mA	0.00	8.00	PASS
Output ripple Vin = 18 V	17.46	mV	0.00	80.00	PASS
Output ripple Vin = 28 V	17.89	mV	0.00	80.00	PASS
Output ripple Vin = 40 V	18.57	mV	0.00	80.00	PASS
Neg Output ripple Vin = 18 V	19.65	mV	0.00	80.00	PASS
Neg Output ripple Vin = 28 V	19.24	mV	0.00	80.00	PASS
Neg Output ripple Vin = 40 V	20.30	mV	0.00	80.00	PASS
Input ripple current	10.36	mA	0.00	50.00	PASS
Frequency	552	KHz	425	575	PASS
Efficiency	77.99	%	76.00	90.00	PASS
OvLd TP. Vin = 28 V	0.513	A	0.370	0.550	PASS
ShortCircuit PD.	5.545	W	0.000	9.000	PASS
Neg ShortCircuit PD.	5.541	W	0.000	9.000	PASS
HTF transient	-61	mV	-300	300	PASS
HTF recovery time	0	uS	0	200	PASS
Neg HTF transient	0	mV	-300	300	PASS
Neg HTF recovery time	0	uS	0	200	PASS
FTH transient	56	mV	-300	300	PASS
FTH recovery time	0	uS	0	200	PASS
Neg FTH transient	-62	mV	-300	300	PASS
Neg FTH recovery time	0	uS	0	200	PASS
TO 10%Ld overshoot	784.3	mV	2.0	1500.0	PASS
TO 10%Ld Delay time	4.9	mS	0.0	10.0	PASS
Neg TO 10%Ld overshoot	862.7	mV	2.0	1500.0	PASS
Neg TO 10%Ld Delay time	4.9	mS	0.0	10.0	PASS
TOFL overshoot	862.7	mV	0.0	1500.0	PASS
TOFL delay time	4.8	mS	0.0	10.0	PASS
Neg TOFL overshoot	784.3	mV	0.0	1500.0	PASS
Neg TOFL delay time	4.9	mS	0.0	10.0	PASS
Post Test voltage accuracy	14.96	V	14.70	15.30	PASS
Neg Post Test voltage accuracy	14.96	V	14.70	15.30	PASS

PASSED

Appendix C

(SEE)
Pre, and Final
Parametric Data

```
Filename:      RESULTS\0310S03S.CH
Date:          Wednesday  June 4, 2003
Time:          16:22:05
Test:           FINAL
Program:      FDP 172xxx  Engineering Evaluation Rev. A
Lot Number:    0310
Serial Number: 101
Operator:      ANT
Model:         S2803.3SF/CH
Test Temp:     +25  deg C
```

TEST	RESULT	LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	3.31 V	3.23	3.37	PASS
Line regulation 10% load	0.002 %	-5.000	5.000	PASS
Line regulation Half load	0.003 %	-5.000	5.000	PASS
Line regulation Full load	0.001 %	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.296 %	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.297 %	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.295 %	-1.000	1.000	PASS
Input current NO LOAD	17.98 mA	5.00	60.00	PASS
Input Current With Inhibit	2.65 mA	0.00	8.00	PASS
Output ripple Vin = 18 V	5.16 mV	0.00	35.00	PASS
Output ripple Vin = 28 V	5.03 mV	0.00	35.00	PASS
Output ripple Vin = 40 V	4.85 mV	0.00	35.00	PASS
Input ripple current	9.33 mA	0.00	50.00	PASS
Frequency	523 KHz	425	575	PASS
Efficiency	77.58 %	68.00	90.00	PASS
OvLd TP. Vin = 28 V	4.130 A	3.330	4.240	PASS
ShortCircuit PD.	6.586 W	0.000	9.000	PASS
HTF transient	-108 mV	-300	300	PASS
HTF recovery time	25 uS	0	200	PASS
FTH transient	102 mV	-300	300	PASS
FTH recovery time	18 uS	0	200	PASS
TO 10%Ld overshoot	235.3 mV	2.0	500.0	PASS
TO 10%Ld Delay time	5.9 mS	0.0	10.0	PASS
TOFL overshoot	235.3 mV	0.0	500.0	PASS
TOFL delay time	5.9 mS	0.0	10.0	PASS
Post Test voltage accuracy	3.31 V	3.23	3.37	PASS

```
PASSED
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Date: Monday July 7, 2003
Time: 15:57:08
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0310
Serial Number: 101
Operator: du
Model: S2803.3SF/CH
Test Temp: +25 deg C

TEST	RESULT		LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	3.31	V	3.23	3.37	PASS
Line regulation 10% load	0.003	%	-5.000	5.000	PASS
Line regulation Half load	0.004	%	-5.000	5.000	PASS
Line regulation Full load	0.002	%	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.294	%	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.298	%	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.295	%	-1.000	1.000	PASS
Input current NO LOAD	18.02	mA	5.00	60.00	PASS
Input Current With Inhibit	2.60	mA	0.00	8.00	PASS
Output ripple Vin = 18 V	6.14	mV	0.00	35.00	PASS
Output ripple Vin = 28 V	5.83	mV	0.00	35.00	PASS
Output ripple Vin = 40 V	5.77	mV	0.00	35.00	PASS
Input ripple current	9.56	mA	0.00	50.00	PASS
Frequency	523	KHz	425	575	PASS
Efficiency	77.68	%	68.00	90.00	PASS
OvLd TP. Vin = 28 V	4.110	A	3.330	4.240	PASS
ShortCircuit PD.	6.701	W	0.000	9.000	PASS
HTF transient	-108	mV	-300	300	PASS
HTF recovery time	26	uS	0	200	PASS
FTH transient	102	mV	-300	300	PASS
FTH recovery time	16	uS	0	200	PASS
TO 10%Ld overshoot	235.3	mV	2.0	500.0	PASS
TO 10%Ld Delay time	5.9	mS	0.0	10.0	PASS
TOFL overshoot	196.1	mV	0.0	500.0	PASS
TOFL delay time	5.9	mS	0.0	10.0	PASS
Post Test voltage accuracy	3.31	V	3.23	3.37	PASS

PASSED

Filename: RESULTS\0341S15S.CH
Date: Wednesday June 4, 2003
Time: 16:38:44
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0341
Serial Number: 106
Operator: ANT
Model: S2815SF/CH
Test Temp: +25 deg C

TEST	RESULT		LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	15.02	V	14.70	15.30	PASS
Line regulation 10% load	0.008	%	-5.000	5.000	PASS
Line regulation Half load	0.008	%	-5.000	5.000	PASS
Line regulation Full load	0.006	%	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.015	%	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.015	%	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.014	%	-1.000	1.000	PASS
Input current NO LOAD	36.46	mA	5.00	80.00	PASS
Input Current With Inhibit	2.61	mA	0.00	8.00	PASS
Output ripple Vin = 18 V	3.83	mV	0.00	80.00	PASS
Output ripple Vin = 28 V	3.42	mV	0.00	80.00	PASS
Output ripple Vin = 40 V	3.91	mV	0.00	80.00	PASS
Input ripple current	9.83	mA	0.00	50.00	PASS
Frequency	520	KHz	425	575	PASS
Efficiency	81.31	%	78.00	90.00	PASS
OvLd TP. Vin = 28 V	0.947	A	0.730	0.980	PASS
ShortCircuit PD.	4.845	W	0.000	9.000	PASS
HTF transient	-69	mV	-300	300	PASS
HTF recovery time	0	uS	0	200	PASS
FTH transient	62	mV	-300	300	PASS
FTH recovery time	0	uS	0	200	PASS
TO 10%Ld overshoot	1254.9	mV	2.0	1500.0	PASS
TO 10%Ld Delay time	6.4	mS	0.0	10.0	PASS
TOFL overshoot	1019.6	mV	0.0	1500.0	PASS
TOFL delay time	6.4	mS	0.0	10.0	PASS
Post Test voltage accuracy	15.01	V	14.70	15.30	PASS

PASSED

Filename: RESULTS\0341S15S.CH
Date: Monday July 7, 2003
Time: 15:50:12
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0341
Serial Number: 106
Operator: du
Model: S2815SF/CH
Test Temp: +25 deg C

TEST	RESULT	LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	15.02 V	14.70	15.30	PASS
Line regulation 10% load	0.008 %	-5.000	5.000	PASS
Line regulation Half load	0.007 %	-5.000	5.000	PASS
Line regulation Full load	0.007 %	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.016 %	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.014 %	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.015 %	-1.000	1.000	PASS
Input current NO LOAD	36.53 mA	5.00	80.00	PASS
Input Current With Inhibit	2.64 mA	0.00	8.00	PASS
Output ripple Vin = 18 V	2.77 mV	0.00	80.00	PASS
Output ripple Vin = 28 V	3.60 mV	0.00	80.00	PASS
Output ripple Vin = 40 V	4.21 mV	0.00	80.00	PASS
Input ripple current	10.24 mA	0.00	50.00	PASS
Frequency	520 KHz	425	575	PASS
Efficiency	81.36 %	78.00	90.00	PASS
OvLd TP. Vin = 28 V	0.927 A	0.730	0.980	PASS
ShortCircuit PD.	4.758 W	0.000	9.000	PASS
HTF transient	-68 mV	-300	300	PASS
HTF recovery time	0 uS	0	200	PASS
FTH transient	63 mV	-300	300	PASS
FTH recovery time	0 uS	0	200	PASS
TO 10%Ld overshoot	1254.9 mV	2.0	1500.0	PASS
TO 10%Ld Delay time	6.2 mS	0.0	10.0	PASS
TOFL overshoot	862.7 mV	0.0	1500.0	PASS
TOFL delay time	6.3 mS	0.0	10.0	PASS
Post Test voltage accuracy	15.01 V	14.70	15.30	PASS

PASSED

Filename: RESULTS\0310S15D.CH
Date: Tuesday June 3, 2003
Time: 18:53:39
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0310
Serial Number: 102
Operator: atu
Model: S2815DF/CH
Test Temp: +25 deg C

TEST	RESULT		LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	14.98	V	14.70	15.30	PASS
Neg Output voltage accuracy	14.96	V	14.70	15.30	PASS
Line regulation 10% load	0.015	%	-5.000	5.000	PASS
Line regulation Half load	0.016	%	-5.000	5.000	PASS
Line regulation Full load	0.016	%	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.006	%	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.007	%	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.008	%	-1.000	1.000	PASS
Pos Cross regulation Vin = 18 V	0.86	%	-3.00	3.00	PASS
Pos Cross regulation Vin = 28 V	0.76	%	-3.00	3.00	PASS
Pos Cross regulation Vin = 40 V	0.71	%	-3.00	3.00	PASS
Neg Cross regulation Vin = 18 V	-0.85	%	-3.00	3.00	PASS
Neg Cross regulation Vin = 28 V	-0.70	%	-3.00	3.00	PASS
Neg Cross regulation Vin = 40 V	-0.66	%	-3.00	3.00	PASS
Input current NO LOAD	38.29	mA	5.00	80.00	PASS
Input Current With Inhibit	2.68	mA	0.00	8.00	PASS
Output ripple Vin = 18 V	11.59	mV	0.00	80.00	PASS
Output ripple Vin = 28 V	13.01	mV	0.00	80.00	PASS
Output ripple Vin = 40 V	14.74	mV	0.00	80.00	PASS
Neg Output ripple Vin = 18 V	15.39	mV	0.00	80.00	PASS
Neg Output ripple Vin = 28 V	16.09	mV	0.00	80.00	PASS
Neg Output ripple Vin = 40 V	17.37	mV	0.00	80.00	PASS
Input ripple current	9.54	mA	0.00	50.00	PASS
Frequency	524	KHz	425	575	PASS
Efficiency	78.62	%	76.00	90.00	PASS
OvLd TP. Vin = 28 V	0.523	A	0.370	0.55	PASS
ShortCircuit PD.	5.604	W	0.000	9.000	PASS
Neg ShortCircuit PD.	5.604	W	0.000	9.000	PASS
HTF transient	-71	mV	-300	300	PASS
HTF recovery time	0	uS	0	200	PASS
Neg HTF transient	0	mV	-300	300	PASS
Neg HTF recovery time	0	uS	0	200	PASS
FTH transient	64	mV	-300	300	PASS
FTH recovery time	0	uS	0	200	PASS
Neg FTH transient	-66	mV	-300	300	PASS
Neg FTH recovery time	0	uS	0	200	PASS
TO 10%Ld overshoot	705.9	mV	2.0	1500.0	PASS
TO 10%Ld Delay time	6.3	mS	0.0	10.0	PASS
Neg TO 10%Ld overshoot	705.9	mV	2.0	1500.0	PASS
Neg TO 10%Ld Delay time	6.3	mS	0.0	10.0	PASS
TOFL overshoot	784.3	mV	0.0	1500.0	PASS
TOFL delay time	6.3	mS	0.0	10.0	PASS
Neg TOFL overshoot	784.3	mV	0.0	1500.0	PASS
Neg TOFL delay time	6.3	mS	0.0	10.0	PASS
Post Test voltage accuracy	14.96	V	14.70	15.30	PASS
Neg Post Test voltage accuracy	14.95	V	14.70	15.30	PASS

PASSED

Filename: RESULTS\0310S15D.CH
Date: Thursday July 10, 2003
Time: 10:33:39
Test: FINAL
Program: FDP 172xxx Engineering Evaluation Rev. A
Lot Number: 0310
Serial Number: 102
Operator: aa
Model: S2815DF/CH
Test Temp: +25 deg C

TEST	RESULT		LOW LIM	HIGH LIM	STATUS
Output voltage accuracy	14.95	V	14.70	15.30	PASS
Neg Output voltage accuracy	14.94	V	14.70	15.30	PASS
Line regulation 10% load	0.009	%	-5.000	5.000	PASS
Line regulation Half load	0.008	%	-5.000	5.000	PASS
Line regulation Full load	0.008	%	-5.000	5.000	PASS
Load regulation Vin = 18 V	0.007	%	-1.000	1.000	PASS
Load regulation Vin = 28 V	0.006	%	-1.000	1.000	PASS
Load regulation Vin = 40 V	0.006	%	-1.000	1.000	PASS
Pos Cross regulation Vin = 18 V	0.91	%	-3.00	3.00	PASS
Pos Cross regulation Vin = 28 V	0.78	%	-3.00	3.00	PASS
Pos Cross regulation Vin = 40 V	0.72	%	-3.00	3.00	PASS
Neg Cross regulation Vin = 18 V	-0.91	%	-3.00	3.00	PASS
Neg Cross regulation Vin = 28 V	-0.72	%	-3.00	3.00	PASS
Neg Cross regulation Vin = 40 V	-0.68	%	-3.00	3.00	PASS
Input current NO LOAD	34.64	mA	5.00	80.00	PASS
Input Current With Inhibit	2.63	mA	0.00	8.00	PASS
Output ripple Vin = 18 V	15.61	mV	0.00	80.00	PASS
Output ripple Vin = 28 V	14.58	mV	0.00	80.00	PASS
Output ripple Vin = 40 V	15.05	mV	0.00	80.00	PASS
Neg Output ripple Vin = 18 V	16.00	mV	0.00	80.00	PASS
Neg Output ripple Vin = 28 V	16.08	mV	0.00	80.00	PASS
Neg Output ripple Vin = 40 V	17.74	mV	0.00	80.00	PASS
Input ripple current	9.83	mA	0.00	50.00	PASS
Frequency	524	KHz	425	575	PASS
Efficiency	78.51	%	76.00	90.00	PASS
OvLd TP. Vin = 28 V	0.523	A	0.370	0.55	PASS
ShortCircuit PD.	5.545	W	0.000	9.000	PASS
Neg ShortCircuit PD.	5.599	W	0.000	9.000	PASS
HTF transient	-69	mV	-300	300	PASS
HTF recovery time	0	uS	0	200	PASS
Neg HTF transient	0	mV	-300	300	PASS
Neg HTF recovery time	0	uS	0	200	PASS
FTH transient	64	mV	-300	300	PASS
FTH recovery time	0	uS	0	200	PASS
Neg FTH transient	-64	mV	-300	300	PASS
Neg FTH recovery time	0	uS	0	200	PASS
TO 10%Ld overshoot	705.9	mV	2.0	1500.0	PASS
TO 10%Ld Delay time	6.4	mS	0.0	10.0	PASS
Neg TO 10%Ld overshoot	705.9	mV	2.0	1500.0	PASS
Neg TO 10%Ld Delay time	6.5	mS	0.0	10.0	PASS
TOFL overshoot	784.3	mV	0.0	1500.0	PASS
TOFL delay time	6.4	mS	0.0	10.0	PASS
Neg TOFL overshoot	784.3	mV	0.0	1500.0	PASS
Neg TOFL delay time	6.4	mS	0.0	10.0	PASS
Post Test voltage accuracy	14.94	V	14.70	15.30	PASS
Neg Post Test voltage accuracy	14.94	V	14.70	15.30	PASS

PASSED