

# RIC7113L4

## RADIATION HARDENED HIGH AND LOW SIDE GATE DRIVER

### Features

- Total dose capability to 100 kRads(Si)
- Floating channel designed for bootstrap operation
- Fully operational to +400V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V  
Logic and power ground  $\pm 5V$  offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Hermetically Sealed
- Lightweight
- ESD Rating: Class 1C per MIL-STD-883, Method 3015

### Product Summary

<b>V<sub>OFFSET</sub></b>	<b>400V max.</b>
<b>I<sub>O+/-</sub></b>	<b>2A / 2A</b>
<b>V<sub>OUT</sub></b>	<b>10 - 20V</b>
<b>t<sub>on/off</sub> (typ.)</b>	<b>120 &amp; 100 ns</b>
<b>Delay Matching(typ.)</b>	<b>5 ns</b>

### Description

The RIC7113L4 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 400 volts.

### Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min.	Max.	Units	
V <sub>B</sub>	High Side Floating Supply Voltage	-0.5	V <sub>S</sub> + 20	V	
V <sub>S</sub>	High Side Floating Supply Offset Voltage	—	400		
V <sub>HO</sub>	High Side Floating Output Voltage	V <sub>S</sub> - 0.5	V <sub>B</sub> + 0.5		
V <sub>CC</sub>	Low Side Fixed Supply Voltage	-0.5	20		
V <sub>LO</sub>	Low Side Output Voltage	-0.5	V <sub>CC</sub> + 0.5		
V <sub>DD</sub>	Logic Supply Voltage	-0.5	V <sub>SS</sub> + 20		
V <sub>SS</sub>	Logic Supply Offset Voltage	V <sub>CC</sub> - 20	V <sub>CC</sub> + 0.5		
V <sub>IN</sub>	Logic Input Voltage (HIN, LIN & SD)	V <sub>SS</sub> - 0.5	V <sub>DD</sub> + 0.5		
dV <sub>S</sub> /dt	Allowable Offset Supply Voltage Transient (Figure 2)	—	50		V/ns
P <sub>D</sub>	Package Power Dissipation @ T <sub>LEAD</sub> ≤ +25°C	—	1.0		W
R <sub>thJC</sub>	Thermal Resistance, Junction to Case	13 (Typ)	16.4	°C/W	
R <sub>thJ-LEAD</sub>	Thermal Resistance, Junction to Lead *	120 (Typ)	—		
R <sub>thJ-LID</sub>	Thermal Resistance, Junction to Lid *	24 (Typ)	—		
T <sub>J</sub>	Junction Temperature	-55	125	°C	
T <sub>S</sub>	Storage Temperature	-55	150		
T <sub>L</sub>	Lead Temperature (Soldering, 10 seconds)	—	300		
	Weight	1.3(typical)		g	

\* Guaranteed by design, not tested

### Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. The  $V_S$  and  $V_{SS}$  offset ratings are tested with all supplies biased at 15V differential.

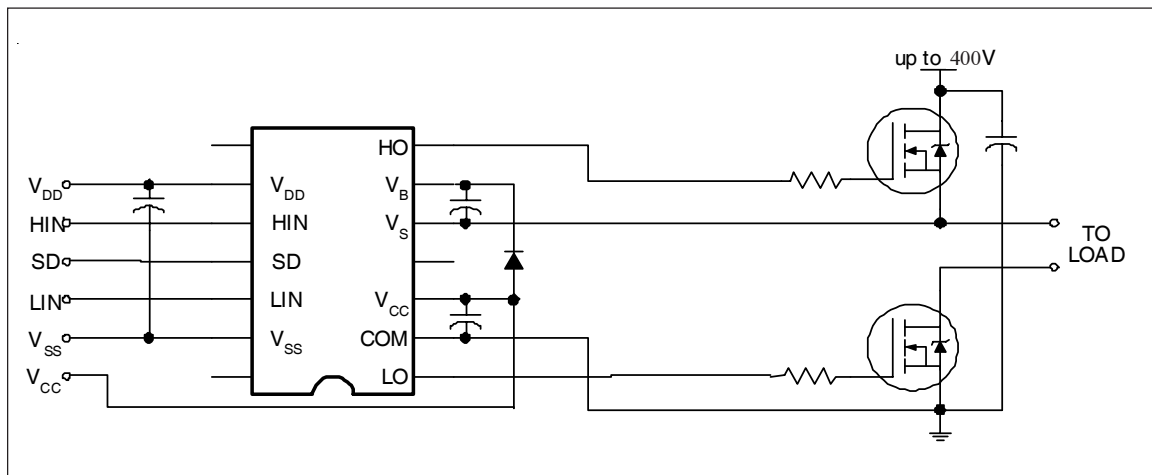
Symbol	Parameter	Min.	Max.	Units
$V_B$	High Side Floating Supply Absolute Voltage	$V_S + 10$	$V_S + 20$	V
$V_S$	High Side Floating Supply Offset Voltage	-4	400	
$V_{HO}$	High Side Floating Output Voltage	$V_S$	$V_B$	
$V_{CC}$	Low Side Fixed Supply Voltage	10	20	
$V_{LO}$	Low Side Output Voltage	0	$V_{CC}$	
$V_{DD}$	Logic Supply Voltage	$V_{SS} + 5$	$V_{SS} + 20$	
$V_{SS}$	Logic Supply Offset Voltage	-5	5	
$V_{IN}$	Logic Input Voltage (HIN, LIN & SD)	$V_{SS}$	$V_{DD}$	

### Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15V, and  $V_{SS}$  = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

Symbol	Parameter	$T_j = 25^\circ\text{C}$			$T_j = -55 \text{ to } 125^\circ\text{C}$		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.		
$t_{on}$	Turn-On Propagation Delay	—	120	150	—	260	ns	$V_S = 0\text{V}$
$t_{off}$	Turn-Off Propagation Delay	—	100	125	—	220		$V_S = 400\text{V}$
$t_{sd}$	Shutdown Propagation Delay	—	110	140	—	235		$V_S = 400\text{V}$
$t_r$	Turn-On Rise Time	—	25	35	—	50		$C_L = 1000\text{pf}$
$t_f$	Turn-Off Fall Time	—	17	25	—	40		$C_L = 1000\text{pf}$
MT	Delay Matching, HS & LS Turn-On/Off	—	5	20	—	—		$ t_{on} - t_{on}  \text{ or }  t_{off} - t_{off} $

### Typical Connection



### Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ,  $V_{DD}$ ) = 15V, unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all three logic input pins: HIN, LIN and SD. The  $V_O$  and  $I_O$  parameters are referenced to COM or  $V_S$  and are applicable to the respective output pins: HO or LO.

Symbol	Parameter	$T_j = 25^\circ\text{C}$		$T_j = -55 \text{ to } 125^\circ\text{C}$		Units	Test Conditions
		Min.	Max.	Min.	Max.		
$V_{IH}$	Logic "1" Input Voltage	3.1	—	3.3	—	V	$V_{DD} = 5\text{V}$
		6.4	—	6.8	—		$V_{DD} = 10\text{V}$
		9.5	—	10	—		$V_{DD} = 15\text{V}$
		12.5	—	13.3	—		$V_{DD} = 20\text{V}$
$V_{IL}$	Logic "0" Input Voltage	—	1.6	—	1.6	V	$V_{DD} = 5\text{V}$
		—	3.8	—	3.6		$V_{DD} = 10\text{V}$
		—	6.0	—	5.7		$V_{DD} = 15\text{V}$
		—	8.3	—	7.9		$V_{DD} = 20\text{V}$
$V_{OH}$	High Level Output Voltage, $V_{BIAS} - V_O$	—	1.2	—	1.5	V	$V_{IN} = V_{IH}$ , $I_O = 0\text{A}$
$V_{OL}$	Low Level Output Voltage, $V_O$	—	0.1	—	0.1		$V_{IN} = V_{IH}$ , $I_O = 0\text{A}$
$I_{LK}$	Offset Supply Leakage Current	—	50	—	250	$\mu\text{A}$	$V_B = V_S = 400\text{V}$
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	—	230	—	500		$V_{IN} = 0\text{V}$ or $V_{DD}$
$I_{QCC}$	Quiescent $V_{CC}$ Supply Current	—	340	—	600		$V_{IN} = 0\text{V}$ , or $V_{DD}$
$I_{QDD}$	Quiescent $V_{DD}$ Supply Current	—	30	—	60		$V_{IN} = 0\text{V}$ , or $V_{DD}$
$I_{IN+}$	Logic "1" Input Bias Current	—	40	—	70		$V_{IN} = V_{DD}$
$I_{IN-}$	Logic "0" Input Bias Current	—	1.0	—	10		$V_{IN} = 0\text{V}$
$V_{BSUV+}$	$V_{BS}$ Supply Undervoltage Positive Going Threshold	7.5	9.7	—	—	V	
$V_{BSUV-}$	$V_{BS}$ Supply Undervoltage Negative Going Threshold	7.0	9.4	—	—		
$V_{CCUV+}$	$V_{CC}$ Supply Undervoltage Positive Going Threshold	7.4	9.6	—	—		
$V_{CCUV-}$	$V_{CC}$ Supply Undervoltage Negative Going Threshold	7.0	9.4	—	—		
$I_{O+}$	Output High Short Circuit Pulsed Current *	2.0	—	—	—	A	$V_O = 0\text{V}$ , $V_{IN} = V_{DD}$ $PW \leq 10 \mu\text{s}$
$I_{O-}$	Output Low Short Circuit Pulsed Current *	2.0	—	—	—		$V_O = 15\text{V}$ , $V_{IN} = 0\text{V}$ $PW \leq 10 \mu\text{s}$

\* Guaranteed by design, not tested

### Radiation Performance

International Rectifier Radiation Hardened gate drivers are tested to verify their hardness capability. The hardness assurance program at International Rectifier uses a Cobalt-60 (<sup>60</sup>Co) source and heavy ion irradiation.

Every wafer shall be tested per MIL-STD-883, Method 1019, test condition A “Ionizing Radiation (Total Dose) Test Procedure”.

Both pre- and post- irradiation performances are tested and specified using the same drive circuitry and test conditions to provide a direct comparison.

For Static Irradiation Test Conditions refer to figure 7.

Static Electrical Characteristics		Tj = 25°C		Units	Test Conditions
		100K Rads (Si)			
		Min	Max		
V <sub>IH</sub>	Logic “1” Input Voltage	3.1	—	V	VDD = 5V
		6.4	—		VDD = 10V
		9.5	—		VDD = 15V
		12.5	—		VDD = 20V
V <sub>IL</sub>	Logic “0” Input Voltage	—	1.6	V	VDD = 5V
		—	3.8		VDD = 10V
		—	6.0		VDD = 15V
		—	8.3		VDD = 20V
V <sub>OH</sub>	High Level Output Voltage, V <sub>BIAS</sub> - V <sub>O</sub>	—	1.2		V <sub>IN</sub> = V <sub>IH</sub> , I <sub>O</sub> = 0A
V <sub>OL</sub>	Low Level Output Voltage, V <sub>O</sub>	—	0.1		V <sub>IN</sub> = V <sub>IH</sub> , I <sub>O</sub> = 0A
I <sub>LK</sub>	Offset Supply Leakage Current	—	50	µA	V <sub>B</sub> = V <sub>S</sub> = 400V
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> Supply Current	—	230		V <sub>IN</sub> = 0V or VDD
I <sub>QCC</sub>	Quiescent V <sub>CC</sub> Supply Current	—	340		V <sub>IN</sub> = 0V or VDD
I <sub>QDD</sub>	Quiescent V <sub>DD</sub> Supply Current	—	30		V <sub>IN</sub> = 0V or VDD
I <sub>IN+</sub>	Logic “1” Input Bias Current	—	40		V <sub>IN</sub> = VDD
I <sub>IN-</sub>	Logic “0” Input Bias Current	—	1.0		V <sub>IN</sub> = 0V
V <sub>BSUV+</sub>	V <sub>BS</sub> Supply Undervoltage Positive Going Threshold	7.5	9.7		V
V <sub>BSUV-</sub>	V <sub>BS</sub> Supply Undervoltage Negative Going Threshold	7.0	9.4		
V <sub>CCUV+</sub>	V <sub>CC</sub> Supply Undervoltage Positive Going Threshold	7.4	9.9		
V <sub>CCUV-</sub>	V <sub>CC</sub> Supply Undervoltage Negative Going Threshold	7.0	9.6		
I <sub>O+</sub>	Output High Short Circuit Pulsed Current *	2.0	—	A	V <sub>O</sub> = 0V, V <sub>IN</sub> = VDD PW ≤ 10 µs
I <sub>O-</sub>	Output Low Short Circuit Pulsed Current *	2.0	—		V <sub>O</sub> = 15V, V <sub>IN</sub> = 0V PW ≤ 10 µs

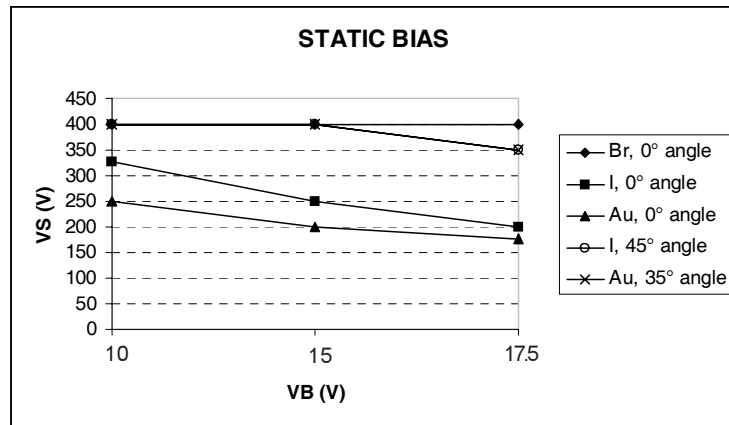
\* Guaranteed by design, not tested

International Rectifier radiation hardened Gate Drivers have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization data is illustrated below. For Static Bias Test Conditions refer to figure 8.

**Single Event Effect Safe Operating Area**

Ion	LET MeV/(mg/cm <sup>2</sup> )	Energy (MeV)	Angle (degrees)	V <sub>s</sub> (V)		
				@V <sub>BS</sub> = 10V	@V <sub>BS</sub> = 15V	@V <sub>BS</sub> = 17.5V
Br	37	284	0	400	400	400
I	60	344	0	325	250	200
Au	82	346	0	250	200	175
I	85	344	45	400	400	350
Au	100	346	35	400	400	350

Note: VCC/VDD = 20V, except for LET=100, then VCC/VDD = 17.5V



Single Event Effect, Safe Operating Area

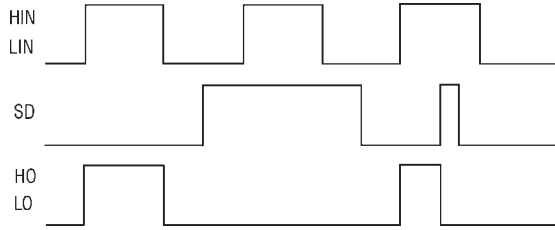


Figure 1. Input/Output Logic Timing Diagram

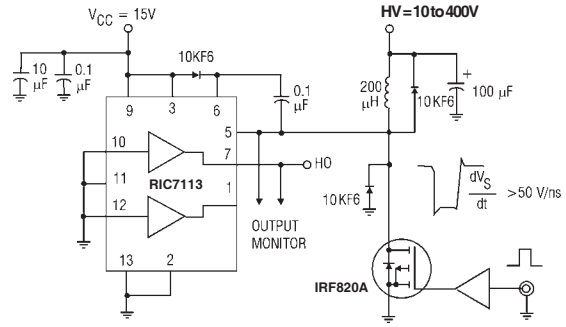


Figure 2. Floating Supply Voltage Transient Test Circuit

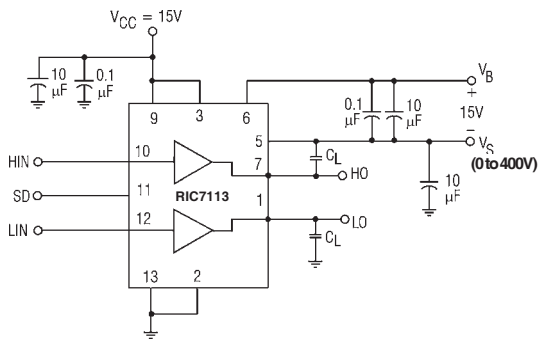


Figure 3. Switching Time Test Circuit

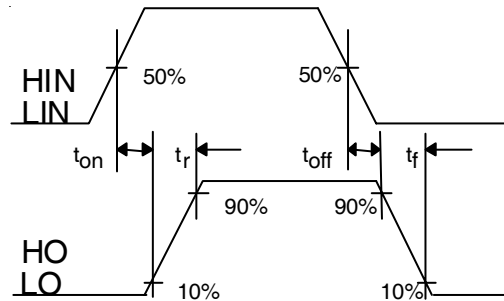


Figure 4. Switching Time Waveform Definition

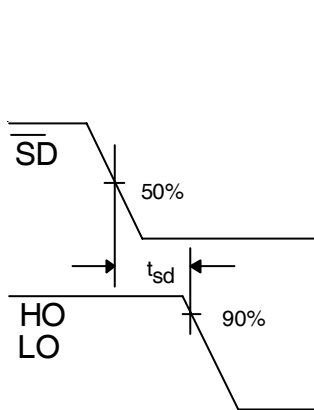


Figure 5. Shutdown Waveform Definitions

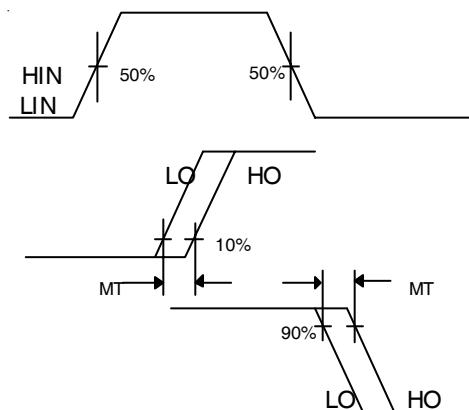


Figure 6. Delay Matching Waveform Definitions

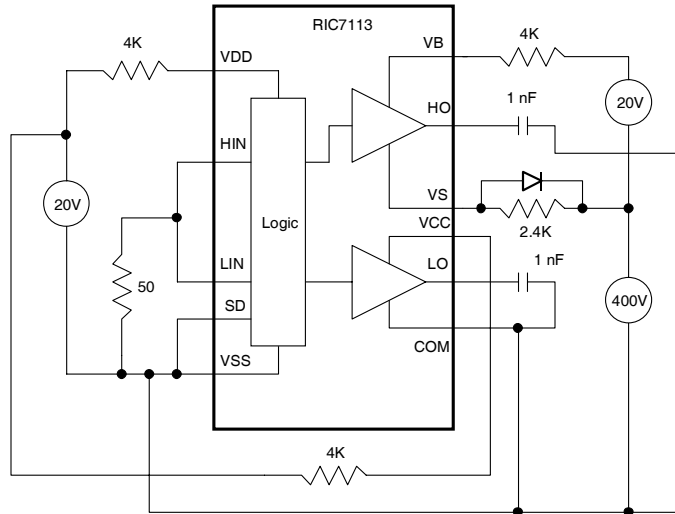


Figure 7. Static Bias Conditions for Total Ionizing Dose Test

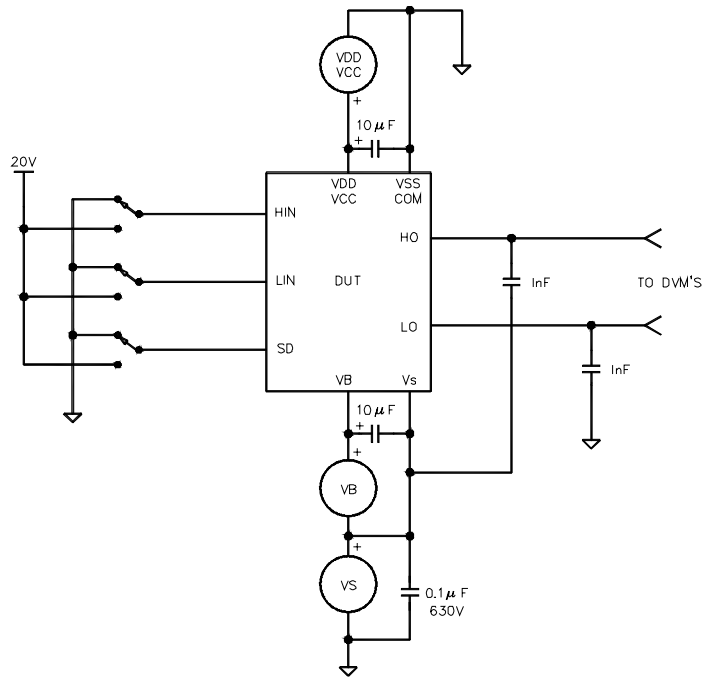
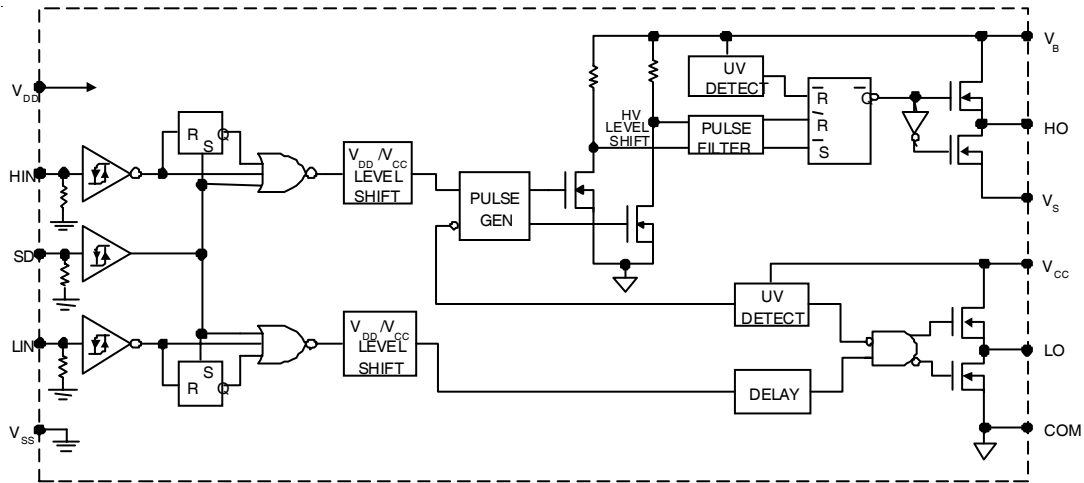


Figure 8. Static Bias Conditions for Single Event Effect Test

**Functional Block Diagram**

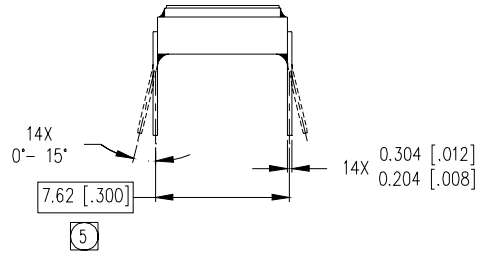
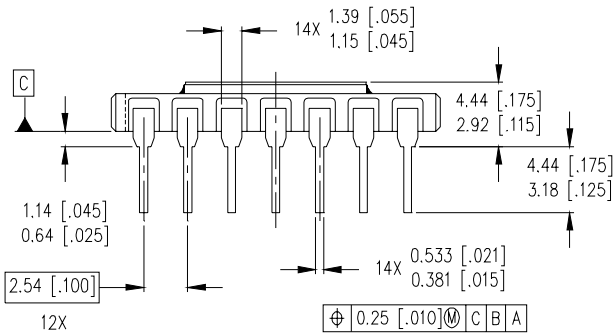
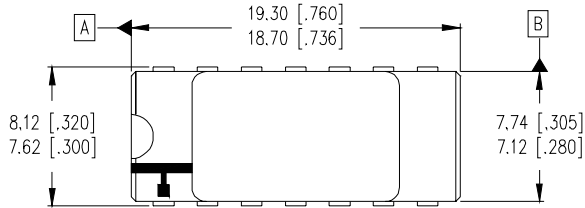


**Lead Definitions**

Symbol	Description
VDD	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
VSS	Logic ground
VB	High side floating supply
HO	High side gate drive output
VS	High side floating supply return
VCC	Low side supply
LO	Low side gate drive output
COM	Low side return



**Case Outline and Dimensions — MO-036AB Package**



**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MO-036AB.
- ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

**LEAD ASSIGNMENTS**

