

**RADIATION HARDENED  
 LOGIC LEVEL POWER MOSFET  
 THRU-HOLE (MO-036AB)**

**2N7614M1  
 IRHLG77214  
 250V, Quad N-CHANNEL  
 TECHNOLOGY**



**Product Summary**

Part Number	Radiation Level	RDS(on)	ID
IRHLG77214	100K Rads (Si)	1.1Ω	0.8A
IRHLG73214	300K Rads (Si)	1.1Ω	0.8A



International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

**Features:**

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight

**Absolute Maximum Ratings**

**Pre-Irradiation**

	Parameter		Units
ID @ VGS = 4.5V, TC= 25°C	Continuous Drain Current	0.8	A
ID @ VGS = 4.5V, TC= 100°C	Continuous Drain Current	0.5	
IDM	Pulsed Drain Current ①	3.2	
PD @ TC = 25°C	Max. Power Dissipation	1.4	W
	Linear Derating Factor	0.01	W/°C
VGS	Gate-to-Source Voltage	±10	V
EAS	Single Pulse Avalanche Energy ②	50.4	mJ
IAR	Avalanche Current ①	0.8	A
EAR	Repetitive Avalanche Energy ①	0.14	mJ
dv/dt	Peak Diode Recovery dv/dt ③	12.3	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063in/1.6mm from case for 10s)	
	Weight	1.3 (Typical)	g

For footnotes refer to the last page

**Electrical Characteristics For Each N-Channel Device @ T<sub>J</sub> = 25°C (Unless Otherwise specified)**

	Parameter	Min	Typ	Max	Units	Test Conditions
B <sub>V</sub> D <sub>SS</sub>	Drain-to-Source Breakdown Voltage	250	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔB <sub>V</sub> D <sub>SS</sub> /ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	0.34	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	1.1	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 0.5A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	—	-6.0	—	mV/°C	
g <sub>fs</sub>	Forward Transconductance	1.0	—	—	S	V <sub>DS</sub> = 15V, I <sub>DS</sub> = 0.5A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	1.0	μA	V <sub>DS</sub> = 200V, V <sub>GS</sub> = 0V
		—	—	10		V <sub>DS</sub> = 200V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 10V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -10V
Q <sub>g</sub>	Total Gate Charge	—	—	15	nC	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 0.8A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	3.5		V <sub>DS</sub> = 125V
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	—	8.3		
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	18	ns	V <sub>DD</sub> = 125V, I <sub>D</sub> = 0.8A, V <sub>GS</sub> = 4.5V, R <sub>G</sub> = 7.5Ω
t <sub>r</sub>	Rise Time	—	—	85		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	35		
t <sub>f</sub>	Fall Time	—	—	30		
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	10	—	nH	Measured from Drain lead (6mm /0.25in from pack.) to Source lead (6mm/0.25in from pack.) with Source wire internally bonded from Source pin to Drain pad
C <sub>iss</sub>	Input Capacitance	—	552	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	69	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	1.43	—		
R <sub>g</sub>	Gate Resistance	—	6.77	—	Ω	f = 1.0MHz, open drain

**Source-Drain Diode Ratings and Characteristics (Per Die)**

	Parameter	Min	Typ	Max	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	0.8	A	T <sub>J</sub> = 25°C, I <sub>S</sub> = 0.8A, V <sub>GS</sub> = 0V ④
I <sub>SM</sub>	Pulse Source Current (Body Diode) ①	—	—	3.2		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>F</sub> = 0.8A, di/dt ≤ 100A/μs
t <sub>rr</sub>	Reverse Recovery Time	—	—	290	ns	V <sub>DD</sub> ≤ 25V ④
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	388	nC	
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				

**Thermal Resistance (Per Die)**

	Parameter	Min	Typ	Max	Units	Test Conditions
R <sub>thJA</sub>	Junction-to-Ambient	—	—	90	°C/W	Typical socket mount

Note: Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

## Radiation Characteristics

IRHLG77214, 2N7614M1

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥ (Per Die)**

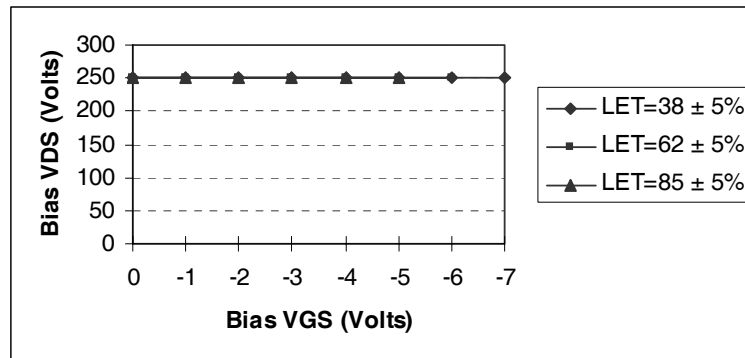
	Parameter	Up to 300K Rads (Si) <sup>1</sup>		Units	Test Conditions
		Min	Max		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	250	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	2.0		V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250μA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	100	nA	V <sub>GS</sub> = 10V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	-100		V <sub>GS</sub> = -10V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	10	μA	V <sub>DS</sub> = 200V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance (TO-39) ④	—	??	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 0.5A
R <sub>DS(on)</sub>	Static Drain-to-Source On-state Resistance (MO-036AB) ④	—	1.1	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 0.5A
V <sub>SD</sub>	Diode Forward Voltage ④	—	1.2	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 0.8A

1. Part numbers IRHLG77214, IRHLG73214

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

**Table 2. Typical Single Event Effect Safe Operating Area**

LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)					
			@VGS=0V	@VGS=-2V	@VGS=-4V	@VGS=-5V	@VGS=-6V	@VGS=-7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	250	250	250	250	250	250
62 ± 5%	355 ± 7.5%	33 ± 7.5%	250	250	250	250	250	-
85 ± 5%	380 ± 7.5%	29 ± 7.5%	250	250	250	250	-	-



**Fig a. Typical Single Event Effect, Safe Operating Area**

For footnotes refer to the last page

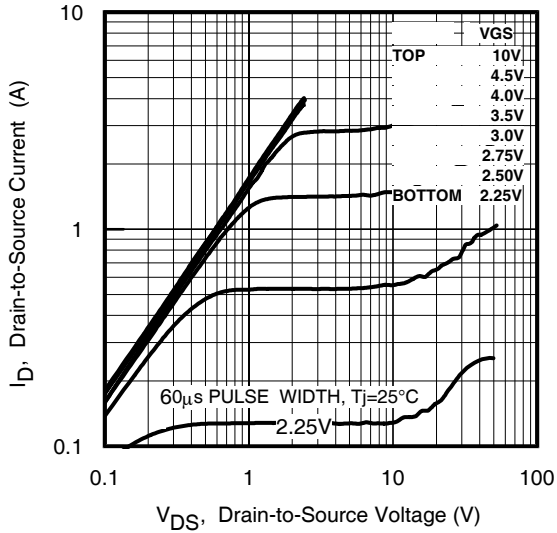


Fig 1. Typical Output Characteristics

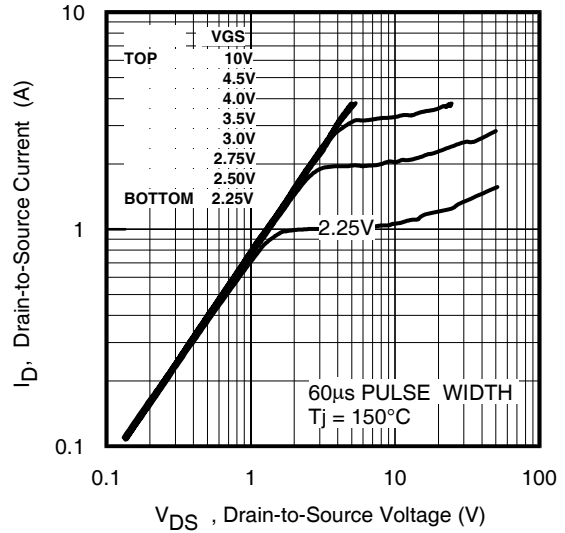


Fig 2. Typical Output Characteristics

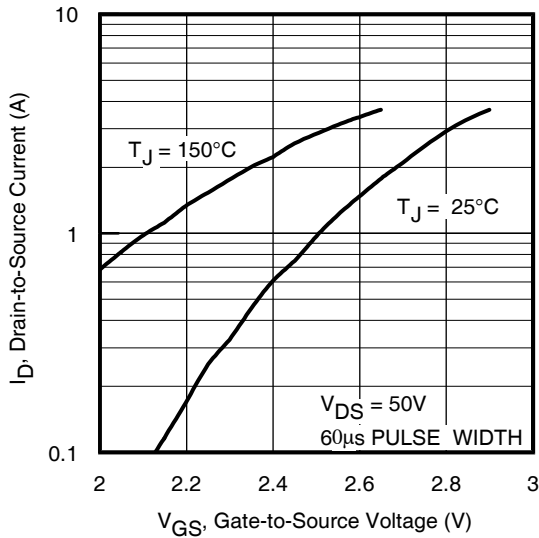


Fig 3. Typical Transfer Characteristics

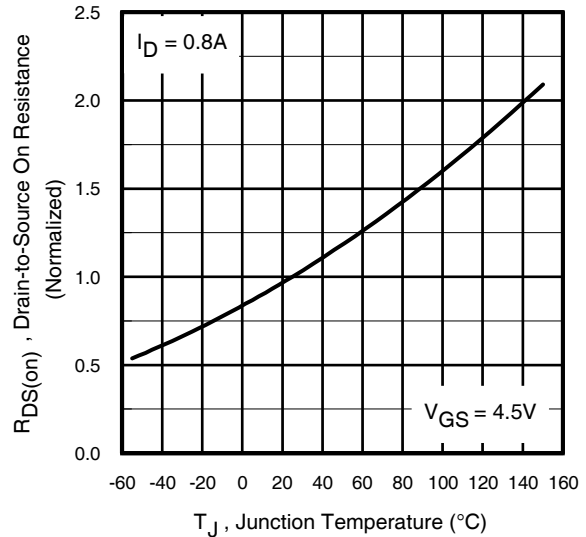
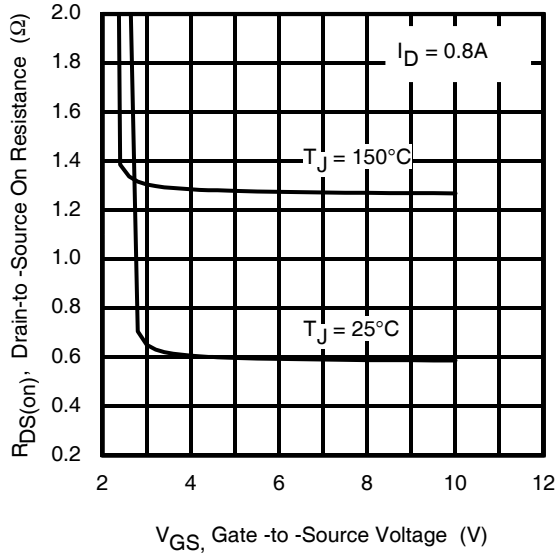
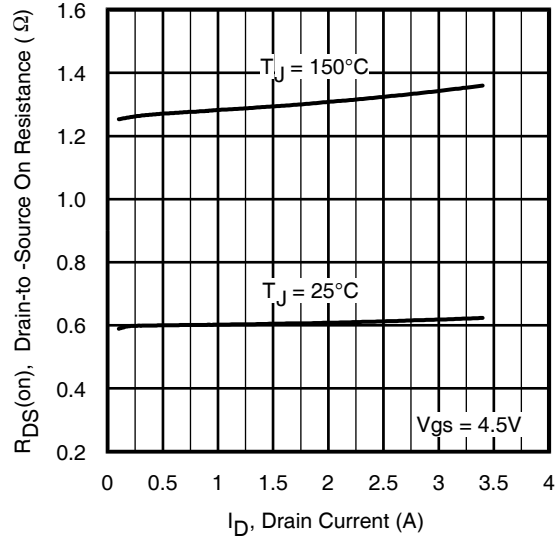


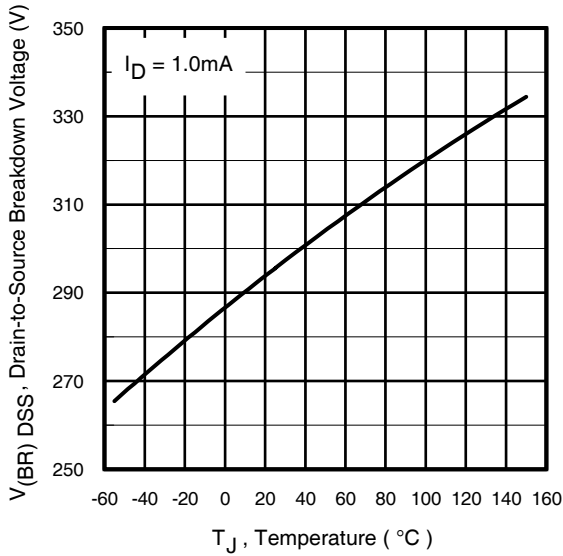
Fig 4. Normalized On-Resistance Vs. Temperature



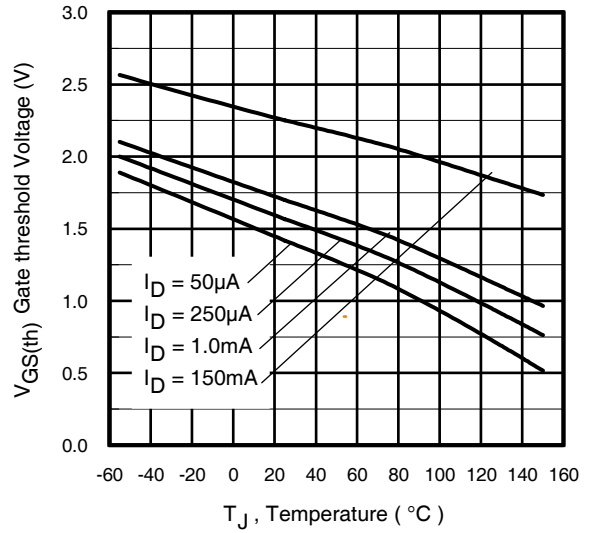
**Fig 5.** Typical On-Resistance Vs Gate Voltage



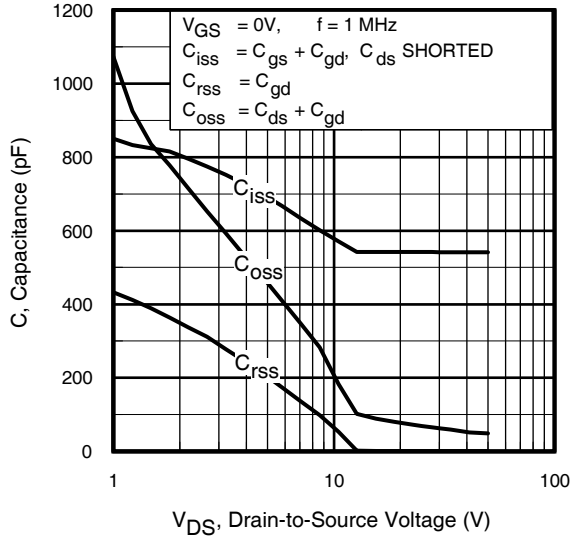
**Fig 6.** Typical On-Resistance Vs Drain Current



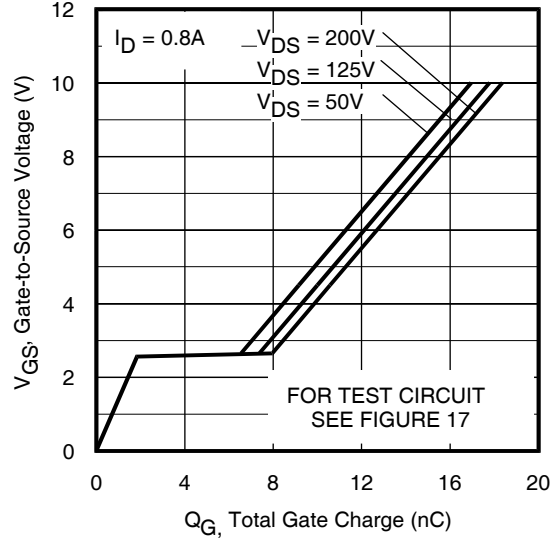
**Fig 7.** Typical Drain-to-Source Breakdown Voltage Vs Temperature



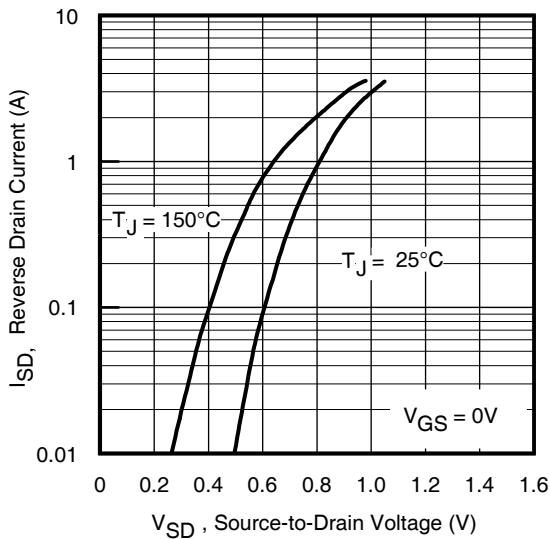
**Fig 8.** Typical Threshold Voltage Vs Temperature



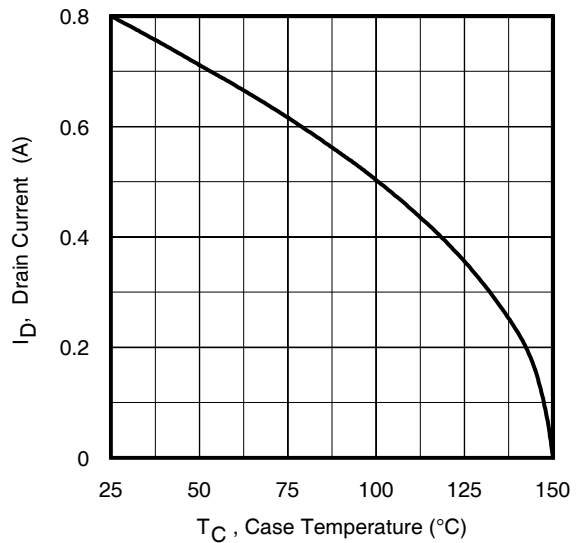
**Fig 9.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 10.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 11.** Typical Source-to-Drain Diode Forward Voltage



**Fig 12.** Maximum Drain Current Vs. Case Temperature

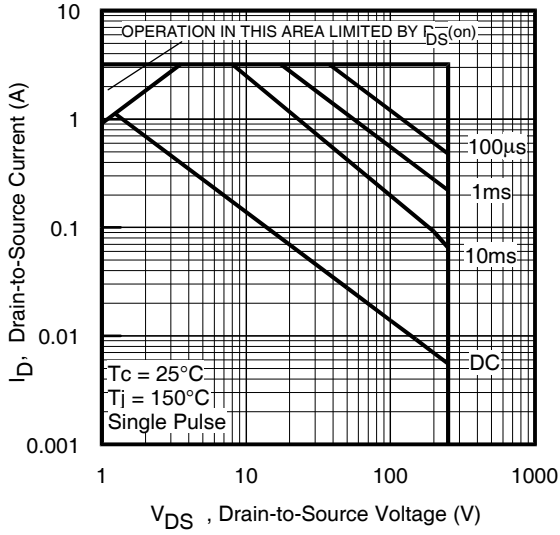


Fig 13. Maximum Safe Operating Area

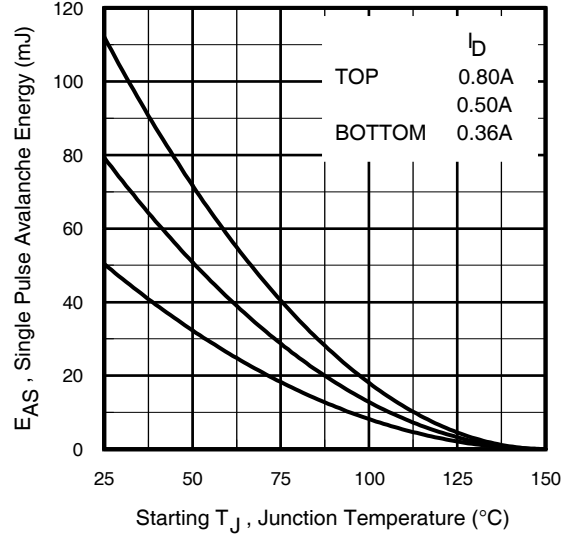


Fig 14. Maximum Avalanche Energy Vs. Drain Current

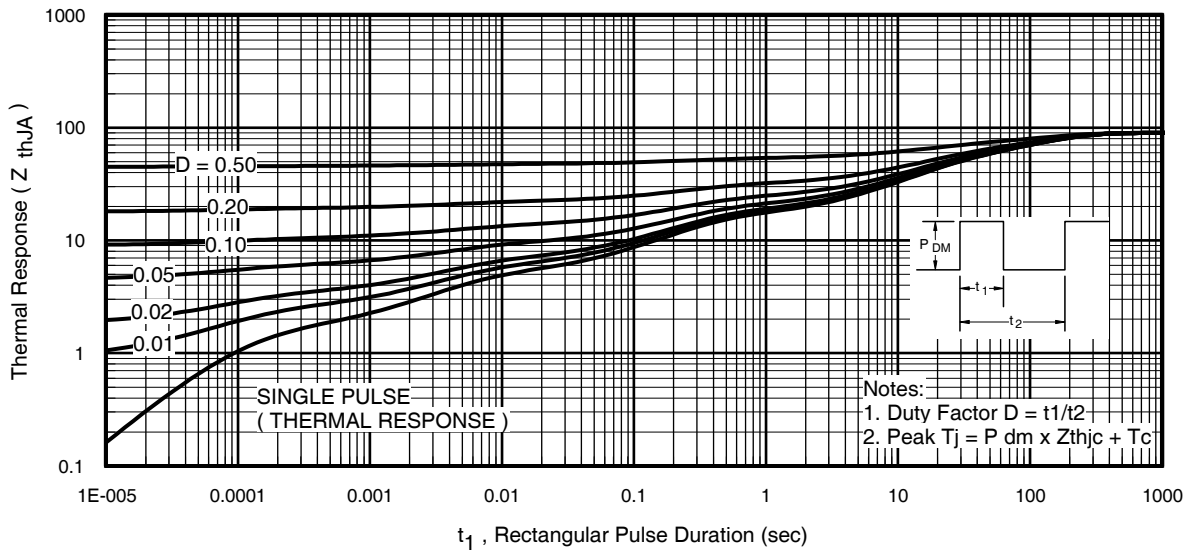


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

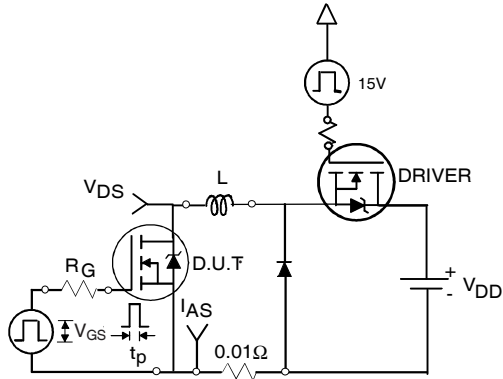


Fig 16a. Unclamped Inductive Test Circuit

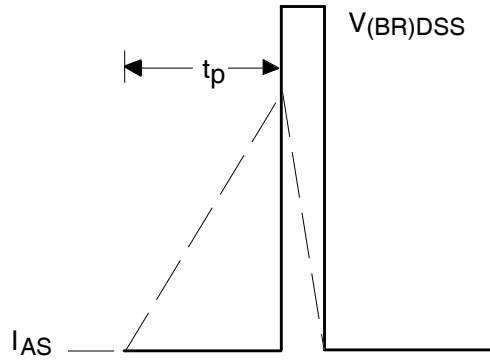


Fig 16b. Unclamped Inductive Waveforms

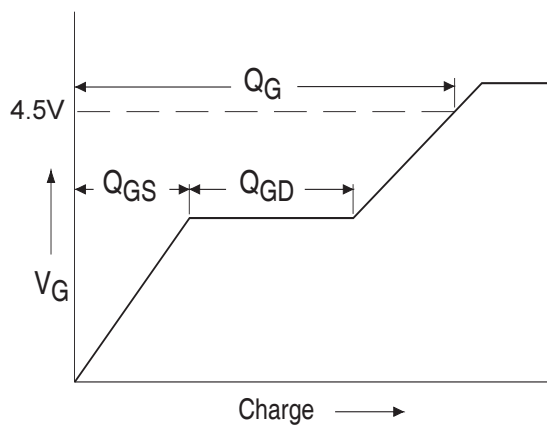


Fig 17a. Basic Gate Charge Waveform

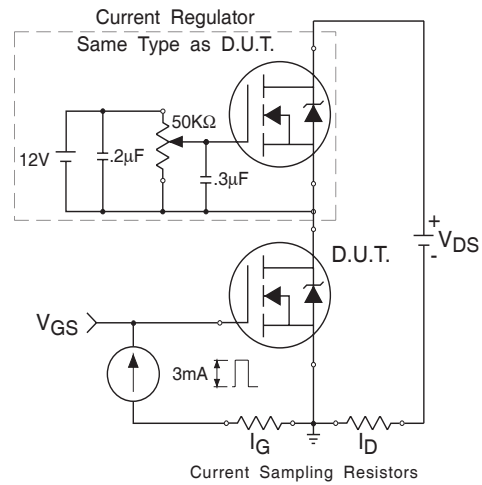


Fig 17b. Gate Charge Test Circuit

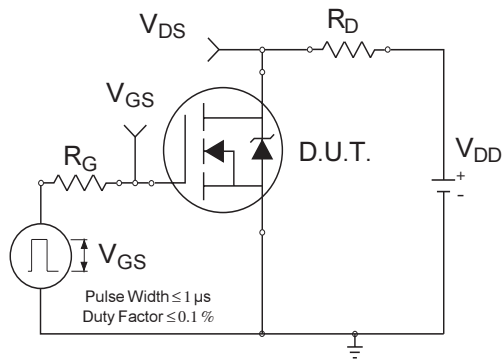


Fig 18a. Switching Time Test Circuit

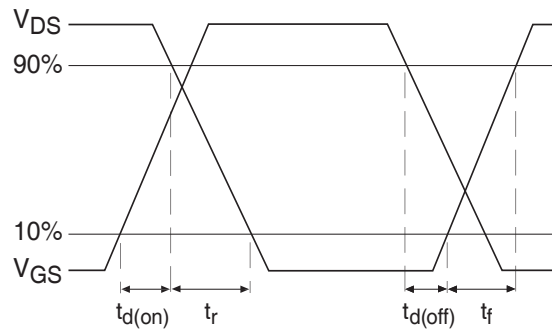


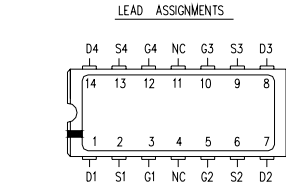
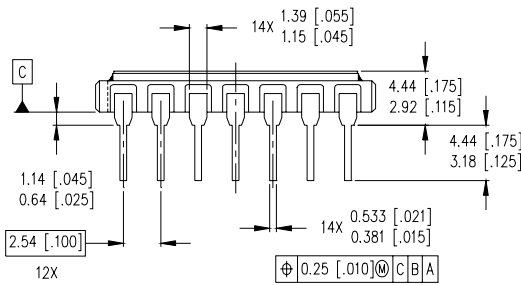
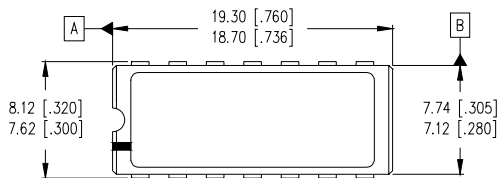
Fig 18b. Switching Time Waveforms



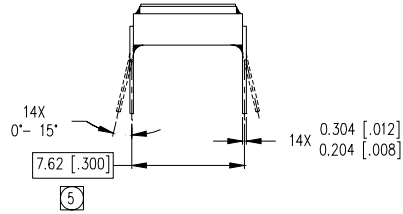
**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ②  $V_{DD} = 50V$ , starting  $T_J = 25^\circ C$ ,  $L = 157mH$   
Peak  $I_L = 0.8A$ ,  $V_{GS} = 10V$
- ③  $I_{SD} \leq 0.8A$ ,  $di/dt \leq 340A/\mu s$ ,  
 $V_{DD} \leq 250V$ ,  $T_J \leq 150^\circ C$
- ④ Pulse width  $\leq 300 \mu s$ ; Duty Cycle  $\leq 2\%$
- ⑤ **Total Dose Irradiation with  $V_{GS}$  Bias.**  
10 volt  $V_{GS}$  applied and  $V_{DS} = 0$  during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with  $V_{DS}$  Bias.**  
200 volt  $V_{DS}$  applied and  $V_{GS} = 0$  during irradiation per MIL-STD-750, method 1019, condition A.

**Case Outline and Dimensions — MO-036AB**



**LEGEND**  
 G = GATE      S = SOURCE  
 D = DRAIN    NC = NO CONNECTION



**NOTES:**

- 1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 4. OUTLINE CONFORMS TO JEDEC OUTLINE MO-036AB.
- ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

International  
**IR** Rectifier

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