Customer Training Workshop
Traveo™ II Fault Subsystem

Q4 2020

Target Products

› Target product families for this training material

Family Category	Series	Code Flash Memory Size
Traveo™ II Automotive Body Controller Entry	CYT2B6	Up to 576KB
Traveo II Automotive Body Controller Entry	CYT2B7	Up to 1088KB
Traveo II Automotive Body Controller Entry	CYT2B9	Up to 2112KB
Traveo II Automotive Body Controller Entry	CYT2BL	Up to 4160KB
Traveo II Automotive Body Controller High	CYT3BB/4BB	Up to 4160KB
Traveo II Automotive Body Controller High	CYT4BF	Up to 8384KB
Traveo II Automotive Cluster	CYT3DL	Up to 4160KB
Traveo II Automotive Cluster	CYT4DN	Up to 6336KB

Fault Subsystem Overview

- Stores fault information
- Supports signaling interface; reset, interrupt, trigger, or output
- Fault sources:
  - MPU/SMPU/PPU violations
  - Peripheral-specific errors
    - For example: WDT, CSV, and BOD on VDDA, OVD on VDDA and LVD
  - Memory-controller-specific errors
    - For example: SRAM ECC errors and Flash ECC errors
- Communicated as either a bus error or a fault in the fault report structure
- Functionality is available only in Active/Sleep power modes

Hint Bar

Review TRM chapter 15 for additional details

See each device datasheet for Fault Sources

Memory protection unit (MPU)

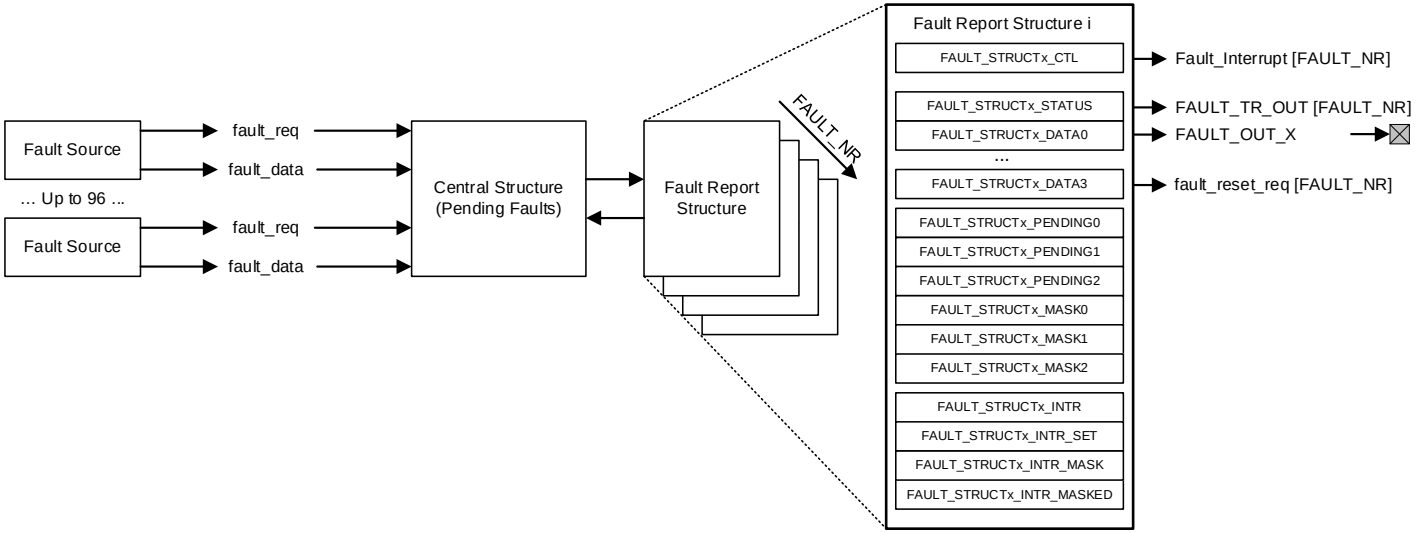
Shared memory protection unit (SMPU)

Peripheral protection unit (PPU)

Error-correction code (ECC)

Fault Subsystem Block Diagram

- Fault subsystem components



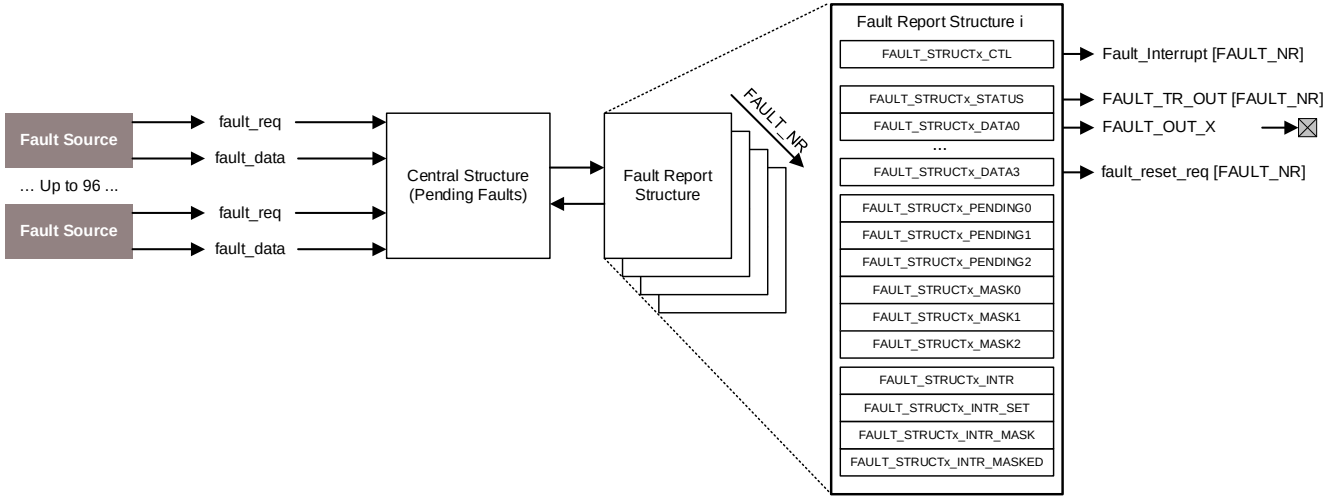
Hint Bar

Review TRM section 15.1 for additional details

See each device datasheet for Fault Sources

Fault Sources

- MPU/SMPU/PPU violations
- Peripheral-specific errors
  - Example: WDT, CSV, and BOD on VDDA, OVD on VDDA, LVD
- Memory-controller-specific errors
  - Examples: SRAM ECC errors, Flash and Flash ECC errors



Hint Bar

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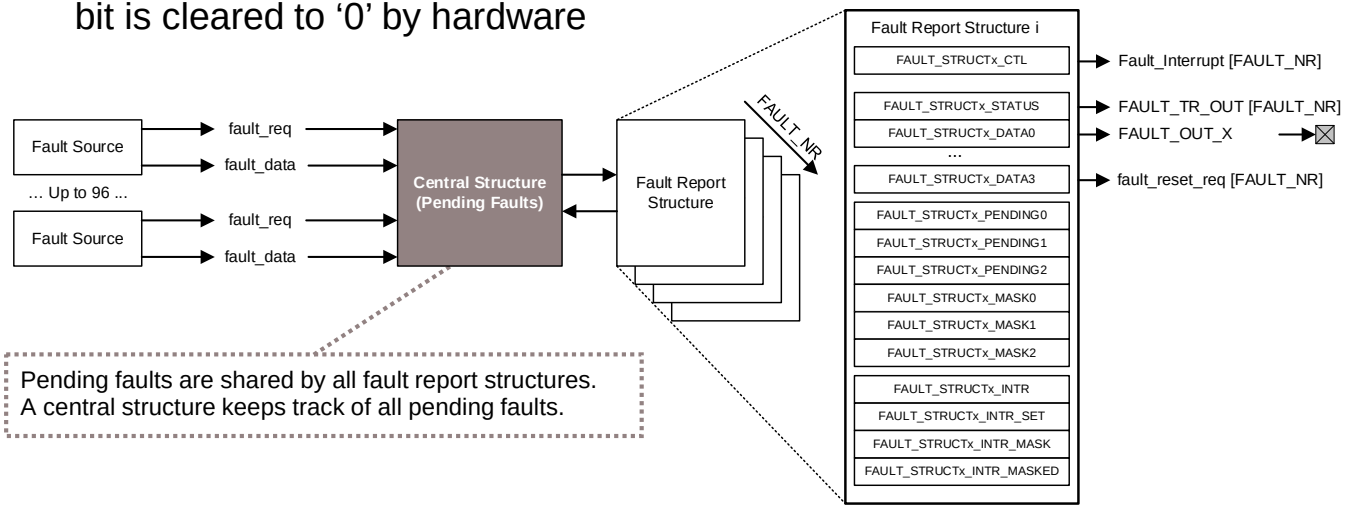
See each device datasheet for Fault Sources

Central Structure

- Pending faults are shared by all fault report structures
- Central structure keeps track of all the pending faults
  - FAULT_STRUCTx_PENDINGy[1] registers reflect which of the fault sources are pending
  - When a pending fault is captured by a fault structure, the associated pending bit is cleared to ‘0’ by hardware



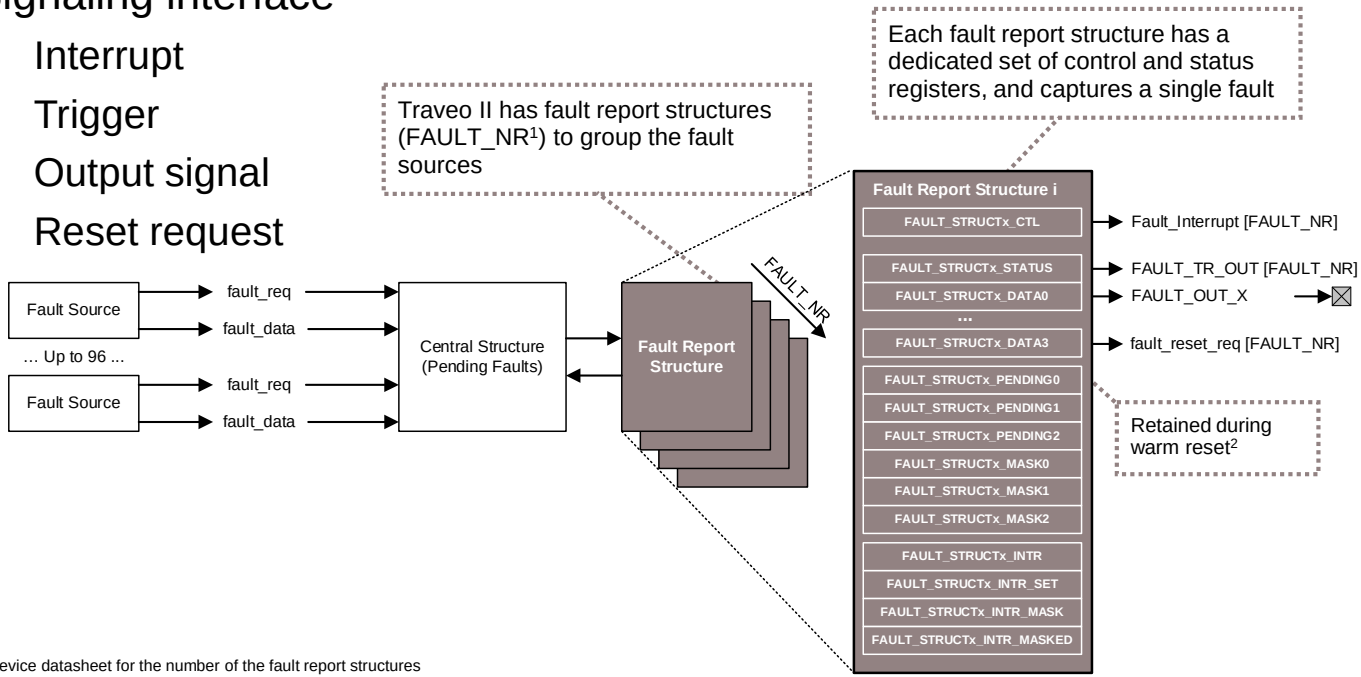
Hint Bar

Review TRM section 15.1 and Register TRM for additional details

[1] FAULT_STRUCTx, 'x' signifies the fault structure instance and 'y' in FAULT_STRUCTx_PENDINGy varies from 0 through 2

Fault Report Structure

- Captures fault information
- Signaling interface
  - Interrupt
  - Trigger
  - Output signal
  - Reset request



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[1] See each device datasheet for the number of the fault report structures
[2] Fault, Software, MCWDT, Debug, CSV

Captured Fault Information

- Each fault report structure has a dedicated set of control and status registers and captures a single fault
- The captured fault information includes:
  - A validity bit field that indicates that a fault is captured
  - A fault index that identifies the fault source
  - Additional fault information
    - Changes depending on the fault source

Fault Sources	Additional Fault Information				
	Fault Block	Syndrome	Violating Address	Master ID	Access Information
MPU/SMPU/PPU/CAN ECC			✔	✔	✔
SRAM/Flash ECC		✔	✔		
Flash Bus Error			✔	✔	
WDT/CSV/BOD/OVD/LVD	✔				

Hint Bar

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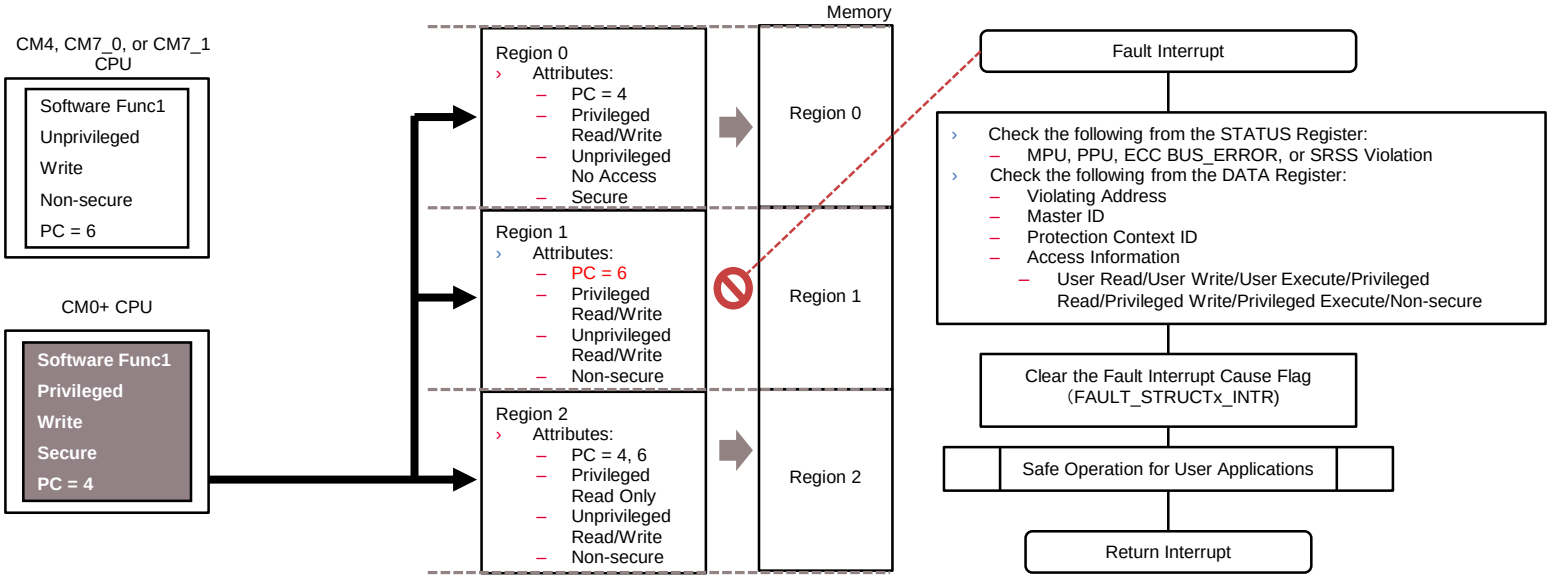
Fault and Protection

- Use a Fault Interrupt when an SMPU violation is detected
  - Enable Fault Source 0 (CM0+ MPU/SMPU violation) of MASK register and INTR_MASK to generate the interrupt
- When CM0+ accesses three memory regions (Region 0, 1, 2), as shown below, a fault interrupt occurs
  - Privileged, Write, Secure, Protection Context (PC) = 4, Access to Region 0, 1, 2



Signaling Interface

- The fault subsystem supports a signaling interface that notifies the CPU or the external system that there is a fault
- The following signals are enabled by software:
  - A fault interrupt (“Fault_Interrupt”)
  - A trigger (“FAULT_TR_OUT”)
  - A chip output pin (“FAULT_OUT_X”)
  - A fault reset request (“fault_reset_req”)
- Use Case:

Fault	Signaling Interface	Purpose
MPU/SMPU/PPU Violation	Interrupt	Check the master and address
ECC Correctable Error (SEC)	Trigger connects to TCPWM	Log the error counts
LVD/CSV Violation	Output pin	Send alarm to system and stop the MCU
MCWDT Timeout	Reset request	Recover from abnormal operation

- Advantage
  - Centralizes fault information management and handles each fault according to system requirements

Hint Bar

Review TRM section 15.1 and Register TRM for additional details

Review the Trigger Multiplexer training section for additional trigger details

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Revision History

Revision	ECN	Submission Date	Description of Change
**	6129736	04/10/2018	Initial release
*A	6321436	09/26/2018	Added page 2, 6, and the note descriptions of all pages. Updated page 3, 4, 7, 9. Removed the Appendix.
*B	6595227	06/14/2019	Updated page 2, 4 to 7, 9, 10.
*C	7013756	10/29/2020	Updated page 2, 6.