

# MOSFET Failure Modes in the Zero-Voltage-Switched Full-Bridge Switching Mode Power Supply Applications

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*Abstract*-As the demand for the telecom/server power is growing exponentially, the need for higher power density increases each year. Increasing power density relies on less component counts, smaller reactive component size, and/or better system efficiency. Higher switching frequency leads to the smaller reactive and filter component size. Better efficiency, which reduces the heat sink or paralleled devices, requires the reduction either in conduction losses or switching losses, or both. Therefore, phase-shifted zero-voltage-switching (ZVS) full bridge topologies are gaining popularity due to their extremely low switching losses in the power devices even at higher switching frequency.

However the intrinsic body diode is required to conduct in order to create the ZVS turn-on condition for the power MOSFET. Due to the extremely low reverse voltage, the reverse recovery charges might not be swept out before turning off the MOSFET. Therefore, the body diode might be subjected to the  $dv/dt$  stress when it is not yet capable of blocking reverse voltage.

Also not able to maintain the ZVS operation at low load will force the on-state MOSFET to turn off at hard-switching condition. Like in the hard-switched full bridge topology, the  $cdv/dt$  shoot-through current might produce a voltage spike at the gate of the off-state MOSFET on the same leg and cause devices failure.

Several silicon technologies will be presented to resolve the above-mentioned failure modes in the ZVS topology. Fast reverse recovery time and better  $dv/dt$  ruggedness make this new MOSFET technology suitable for higher frequency ZVS full-bridge applications. Inherent with extremely high silicon density and low gate charge, these new MOSFETs can reduce the component count with the same or better performance and will enable much higher power density for the next generation telecom/server SMPS designs.

## I. INTRODUCTION

Demand for higher power density, especially in the telecom/server power applications, has driven the power electronics industry to the innovation of better topologies and power devices. The design trends are higher power density and more reliable power devices. Increasing power density from 5-7 W/in<sup>3</sup> now to 10 W/in<sup>3</sup> in the same form factor is an incredible challenge for power supply designers.

Phase-shifted zero-voltage-switching (ZVS) topology [1] seems to be the remedy for achieving higher power density and increased device reliability. The advantages of ZVS operation are minimized switching losses, higher operation frequency, less  $dv/dt$  and  $di/dt$  dynamic stresses.

Reduction of switching losses enables higher switching frequency and requires less heat sink. Higher switching frequency will also lead to smaller reactive and filter components, and result in higher power density. Less dynamic stresses increase the reliability on power devices.

However, power MOSFET failures have been reported recently in the ZVS full bridge topology [2, 3]. Slow reverse recovery of the intrinsic body diode under low reverse voltage is believed to be the root cause for the MOSFET failures. Screening the reverse recovered time of power MOSFETs is one of the solutions, but customers need to pay the price penalty. Another solution is a complicated network of paralleled fast-recovery diodes to divert current from the body diode of the MOSFET [3, 4]. The best solution is to expedite the reverse recovery process on the body diode [2].

The other field failure is also reported at no or low load conditions in the ZVS circuitry. Unable to achieve ZVS condition at no or low load has forced the power MOSFET to experience hard-switched turn-on and turn-off. The possible failure mode for this operation is the  $Cdv/dt$  shoot-through [5]. Detailed failure analysis on the  $Cdv/dt$  shoot-through problem, together with the silicon and system solutions, will be described in this article.

The in-depth understanding of the failure modes in the ZVS operation has led to the development of a new generation fast-body-diode MOSFET technology that reduces reverse-recovery time, increases  $dv/dt$  stress capability, minimizes the  $Cdv/dt$  shoot-through, and therefore is suitable for the high frequency, high power phase-shifted ZVS applications.

## II. MOSFET FAILURE MODES IN ZVS OPERATION

A full-bridge ZVS topology is displayed in Figure 1 where diodes D1-D4 are the intrinsic body diodes of power MOSFETs Q1-Q4. Capacitors C1- C4 represent either the output capacitances of power...

MOSFETs or external capacitors if more capacitance is required. The stray inductor  $L$  or  $L_r$  represents the leakage inductor of the transformer, or the external inductance. Detailed operation and analysis of a full-bridge ZVS circuit can be found in [1]. Typical waveforms of a one kilowatts ZVS full bridge circuit are shown in Figure 2 with 110 KHz switching frequency. Notice that the drain voltage waveform does not show any overshoot voltage spikes that are often seen in the hard-switched bridge topology.

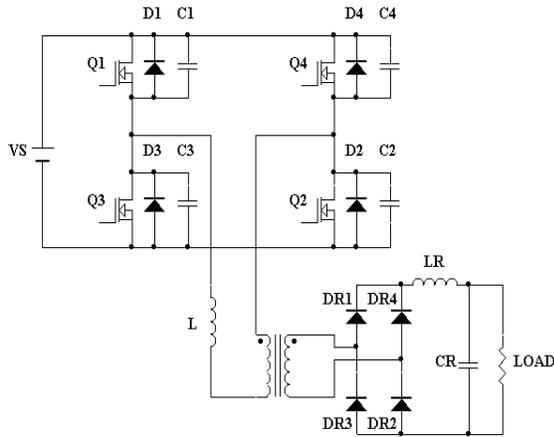


Fig. 1. Phase-Shifted Full Bridge ZVS converter.

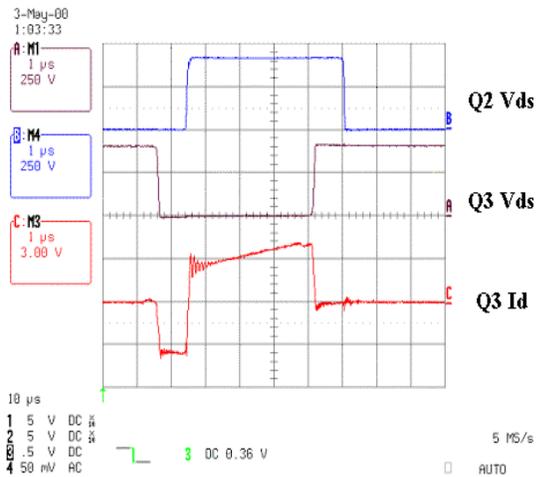


Fig. 2. Phase-shifted ZVS circuit waveforms.

Figure 3 shows a simplified device waveform of Q3. Q1 is turned off at  $t_0$  to start ZVS turn-on of Q3. The resonant network C1, C2, and L or  $L_r$  force to discharge C3 to zero voltage. At  $t_1$ , the body

diode D3 will conduct current and Q3 can be turned on any time during  $t_1$  and  $t_2$ . Q2 will be turned off and Q4 are turned on at  $t_2$  to force current to change direction. Body diode D3 will be in reverse recovery after  $t_3$ . If the reverse recovery process is not completed by  $t_5$ , the time when Q3 is turned off, D3 will not be able to block the reverse voltage and cause failure of the MOSFET.

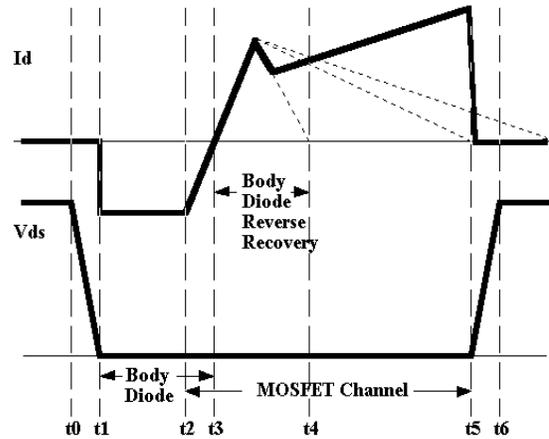


Figure 3. Simplified waveform of Q3

### A. Full Load Failure Mode

Some MOSFET failure modes are inherent to the full-bridge ZVS converter. The power MOSFET is turned on at zero voltage because its body diode needs to conduct first and clamps the drain-source to 0.7V in the phase-shifted ZVS full-bridge topology. No dynamic voltage stress is imposed on the drain of the power MOSFET when the body diode is in reverse recovery. But it will take longer for the body diode to sweep the charges out from the drift region and for the depletion region to be built up under light load and low voltage conditions. The reverse recovery time ( $t_{rr}$ ) of the body diode increases as the applied voltage becomes lower.

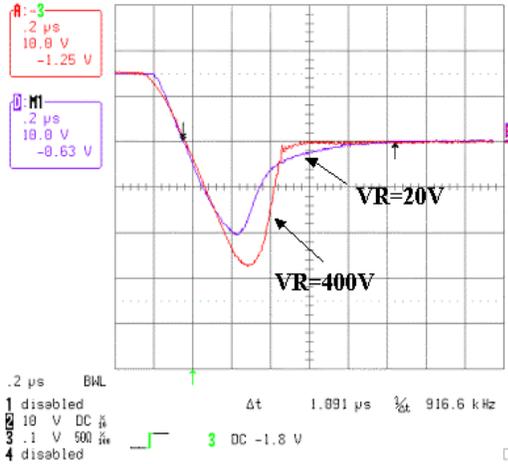


Fig. 4. Reverse voltage effect on reverse recovery

The reverse voltage effect on the body diode during the reverse-recovery process for a standard 500V power MOSFET is shown in Figure 4. Notice that for a conventional power MOSFET, the reverse recovery time increases as the applied reverse voltage decreases. In Table 1 the estimated  $t_{rr}$  at 1V of reverse voltage is 3.73  $\mu\text{s}$ , compared to the 3.6  $\mu\text{s}$  on time for the MOSFET channel in Figure 3. The assumption here is the body diode conducts all the current. Of course, the reverse recovery time is dependent of forward current,  $di/dt$ , and junction temperature. Since the MOSFET can be gated on any time before  $t_2$  in Figure 3, it is likely the body diode will conduct less than the full current.

Reverse Voltage (V)	$T_{rr}$ ( $\mu\text{s}$ )	Comment
1	3.73	Estimated
20	1.09	Measured
100	0.57	Measured
400	0.32	Measured

Table 1. Reverse recovery time versus voltage at 100A/ $\mu\text{s}$  on a standard 500V MOSFET

However, it is clearly shown in Figure 3 the body diode of Q3 needs to complete the reverse recovery before  $t = t_5$ . Otherwise, the body diode D3 is not yet fully recovered and may not be able to block reverse voltage. If the remaining charges are still in the junction and turning on the MOSFET Q1, the resulting  $dv/dt$  may trigger on the parasitic bipolar junction transistor (BJT) and might destroy the power MOSFET.

Once the body diode is in reverse recovery, two conditions could trigger the failure mode [5, 6]. The first is due to the peak reverse recovery current ( $I_{RRM}$ ). Reverse recovery currents flow from drift region into P+ implant. The horizontal component of  $I_{RRM}$  will produce voltage drop on the P+ implant resistance ( $R_b$ ) and might turn on the parasitic BJT. Secondly, turn-off  $dv/dt$  might induce a current through the drain-to-base capacitance  $C_{db}$  and  $R_b$ , and subsequently turn on the parasitic BJT. These reverse recovery current flows are shown in Figure 5.

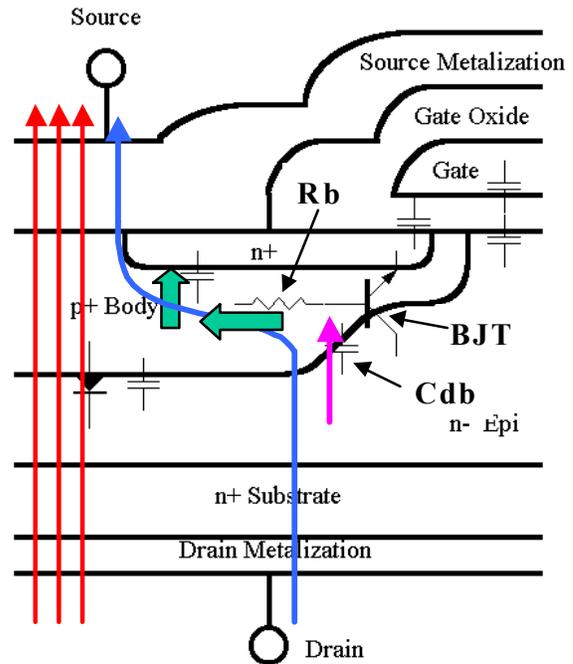


Fig. 5. Cross-section of a standard MOSFET showing current flow during reverse recovery.

All the above-mentioned problems can be resolved by developing the new generation power MOSFETs with the following characteristics:

- Fast reverse recovery of body diode especially at lower reverse voltage;
- Low reverse recovery charge of body diode;
- More ruggedness to reduce tendency for second breakdown.

#### B. Low and No Load Failure Mode

There is another failure mode of the ZVS full-bridge topology which occurs at no or low load condition. The necessary condition for the ZVS

operation is the stored inductive energy in L or Lr is sufficient to swing the capacitor voltage on C1 and C3 when Q1 is turned off at t<sub>0</sub>.

$$\frac{1}{2}L \times i^2 \geq \frac{1}{2}(C_1 + C_3) \times V_S^2.$$

At no or low load current, the capacitor C3 will not be fully discharged to zero voltage at t<sub>1</sub>. The body diode D3 will never conduct current before turn-on of Q3. Figure 6 shows the measured waveform of Q3 at low load conditions in the ZVS full bridge topology. Notice that a little voltage spike shows at the gate corresponding to the sharp change on the drain voltage. The current waveform in Figure 6 indicates the device Q3 is turned on again when it is supposed to be off. This is known as the Cdv/dt shoot-through problem with both the Q1 and Q3 on at the same time causing the leg to short.

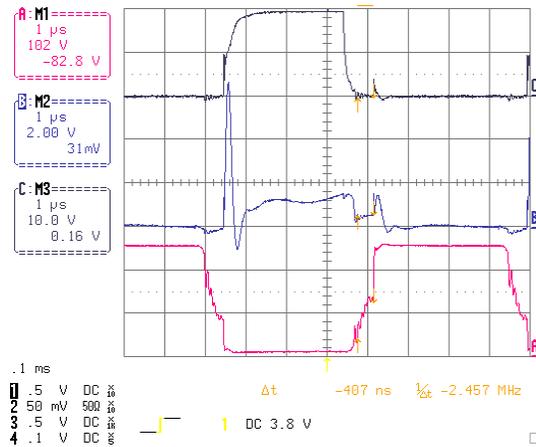


Figure 6. Measured low load waveform in ZVS topology.

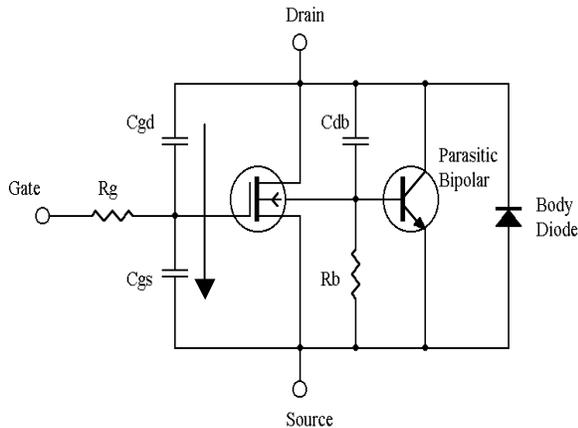


Figure 7. Equivalent circuit showing Cdv/dt shoot-through.

Developing a new generation power MOSFET with the following characteristics will increase Cdv/dt immunity and decrease the likelihood of shoot-through while the phase-shifted ZVS is operating at no or low load condition:

- Lower Qgd/Qgs ratio
- Lower internal Rg
- Increased threshold voltage

### III. NEW ZVS POWER MOSFETS

The potential problems on the power MOSFET for the full-bridge ZVS operation have been well addressed and studied by the authors. The power MOSFET in a ZVS converter needs a fast intrinsic body-diode and low reverse recovery charges. The reverse recovery of the body diode should be fast especially at lower reverse voltage. Figure 8 shows the comparison of the body diode reverse recovery characteristics with the data of reverse recovery time (Trr), charge (Qrr) and peak reverse current (I<sub>RRM</sub>) listed in Table 2.

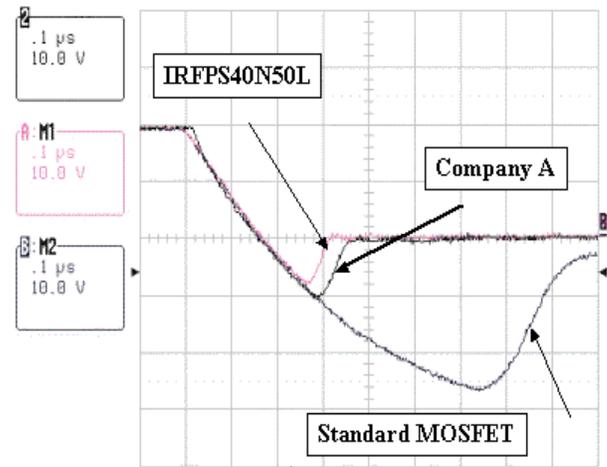


Fig. 8. Body diode reverse recovery comparison.

Devices	Trr (ns)	Qrr (μC)	I <sub>RRM</sub> (A)
Standard	1050	11.91	26
Company A	205	1.26	10
IRFPS40N50L	147	0.69	8

Table 2. Comparison of body-diode reverse recovery characteristics (I<sub>F</sub> = 20A, di/dt = 82 A/μs, V<sub>R</sub> = 25V, T = 25 °C).

Table 3 shows the comparison of total gate charge (Qg), gate-to-source charge (Qgs) and gate-to-drain “Miller” charge (Qgd). The total charge and “Miller” charge on IRFPS40N50L, in Super247™ package are the lowest in the same class. The extremely low gate charge on the “L” series makes driver design much easier and simpler.

Device	Qg (nC)	Qgs (nC)	Qgd (nC)
Company A	420	55	215
IRFPS40N50L	290	66	110

Table 3. Comparison of gate charge (I<sub>D</sub>= 25A, V<sub>DS</sub>=400V, V<sub>GS</sub>=10V, T=25 °C).

Device	Body diode dv/dt (V/ns)
Company A	5
IRFPS40N50L	22

Table 4. Body diode dv/dt comparison.

As discussed above, the charges within the body diode of the MOSFET in a ZVS converter must be removed before the device being turned off. Otherwise the turn-off dv/dt could trigger the BJT and cause device second breakdown while body diode is still in reverse recovery. The problem will get worse when the converter works at high frequency in which less time is available for the body diode to remove and recombine the charges. Therefore, the body diode should be able to sustain the dv/dt stress without turning on the parasitic BJT. The IRFPS40N50L has been structured successfully in this way and has no any negative impacts on the other superior performance of the device. The body diode dv/dt number is listed in Table 4. Thus the “L” series device would be significantly less prone to the second breakdown in ZVS applications.

Devices	Company A	IRFPS40N50L
Relative Die Size	1.6	1
Typical R <sub>don</sub> @25°C	77 mΩ	82 mΩ
Qg loss	0.502 W	0.441 W
Body diode loss	0.114 W	0.121 W
Total Conduction Loss @ 80°C	5.264 W	5.604 W
Total Device Loss @ 80°C	5.765 W	6.046 W

Table 5. In-circuit comparison breakdown of power losses.

The in-circuit testing results of 3 KW ZVS unit at 100 KHz switching frequency are shown in Table 5. The die size of Company A’s is 60% bigger than IRFPS40N50L. However, Company A shows just 5% better in total device power dissipation compared to IRFPS40N50L.

On the other hand, the Cdv/dt shoot-through failure mode can be resolved by reducing the Qgd/Qgs ratio [7] and by decreasing the internal gate resistance. The new silicon technology and process, associated with the “L” series power MOSFETs, have minimized the gate voltage spike dramatically and also increased ruggedness. The in-circuit waveform from three different technologies is shown in Figure 9.

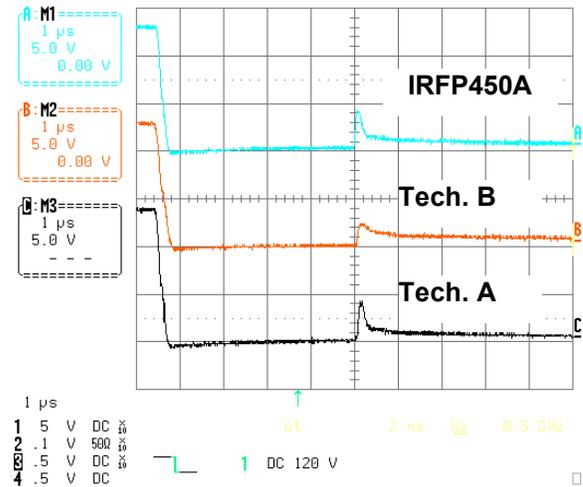


Figure 9. Cdv/dt improvement by silicon technology.

With the combination of the lower Qgd/Qgs ratio and the reduction of the internal R<sub>g</sub>, the voltage spike associated with the Cdv/dt shoot-through has been reduced by 50% with Technology B, as shown in Table 6. The decrease in the Cdv/dt spike reduces the possibility of turn-on of the MOSFET and occurrence of shoot-through. The new “L” series power MOSFET family employed similar silicon technology as those of Technology B. Therefore the “L” series MOSFET devices can effectively reduce the Cdv/dt shoot through problem at no or low load conditions in the phase-shifted ZVS topology.

Device	Cdv/dt Spike (V)	Qgd/Qgs	R <sub>g</sub> (Ohm)
IRFP450A	4	1.7	1.04
Tech. A	3.8	1.95	1.03
Tech. B	1.9	1.47	0.62

Table 6 Cdv/dt improvement with different technologies.

#### IV. CONCLUSION

A new “L” series MOSFET family with low on-resistance, fast recovery body diode and more ruggedness has been studied with the phase-shifted full-bridge ZVS converter. The low on-resistance reduces the conduction loss so that the device will work at a lower junction temperature or reduce the number of paralleled devices. The fast body diode reverse recovery time ( $< 250$  ns maximum) ensures its reverse recovery charges are cleared completely before the MOSFET device can be turned off, especially at a low drain voltage and high switching frequency. The 22V per nanoseconds  $dv/dt$  ruggedness of the IRFPS40N50L ensures the device can sustain higher turn-off stress. With the lower  $Q_{gd}$  to  $Q_{gs}$  ratio along with the reduction of the internal  $R_g$ , it has been shown that the  $Cdv/dt$  immunity of the “L” series MOSFETs has been increased to eliminate the potential shoot-through effect at no load or low load conditions in the phase-shifted ZVS full bridge topology. Measurement results show that the “L” series power MOSFETs are more suitable for the high-voltage, high-power ZVS converter and makes the circuit capable of operating at higher switching frequencies.

#### V. REFERENCES

- [1]. Milan M. Jovanovic, et al., “Zero-Voltage-Switching Technique In High-Frequency Off-Line Converters,” IEEE Proceedings of Applied Power Electronics Conference, pp. 23-32, 1988.
- [2]. Leo Saro, Richard Redl, Kenneth Dierberger, “High-Voltage MOSFET Behavior in Soft-Switching Converter: Analysis and Reliability Improvements,” International Tel-communication Conference, San Francisco, 1998.
- [3]. Hubert Aigner, et al., “Improving the Full-Bridge Phase-shift ZVT Converter for Failure-Free Operation Under Extreme Conditions in Welding and Similar Applications,” IEEE proceedings of Industrial Applications Society Annual Meeting, St. Louis, 1998.
- [4]. D. Grant, “HEXFET III: A New Generation of Power MOSFETs,” International Rectifier Application Note 966A.
- [5]. D.L. Blackburn, “Turn-Off Failure on Power MOSFETs,” Power Electronics Specialists Conference Records, pp. 429-435, 1985.

[6] Thomas Wu, et al, “Dynamic Stresses Might Cause Power MOSFET Failure,” PCIM Magazine, April, 2000.

[7] International Rectifier IRF7809/IRF7811 data sheet.