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# Efficient 200W Low Voltage DC/DC for Redundant On-Board Processing Systems


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***Abstract* — A 200W rad-hard, high current, low output voltage DC/DC converter has been developed and qualified for use in a two for one cold redundant configuration supplying multiple parallel processor channels on-board a communication satellite. Best in class efficiency in excess of 93.5% is achieved and includes all housekeeping consumption as well as the loss in the active diode OR-ing circuit placed in series with the output.**



***Keywords — Power Conversion, Components, Redundancy***


## I. Introduction

Today's communication satellites achieve ultra-high throughput with multiple RF channels and advanced on-board processing. Increased use of baseband processing drives a change in the requirements for DC/DC power supplies specifically there is an increased demand for low voltage, high current DC/DC converters that supply multiple processor channels instead of the typical one-to-one type configuration. To ensure reliability for this system architecture, redundancy is done at DC/DC level. This means the output must be single point failure free for over voltage and output short circuit failures. At the same time the power density and conversion efficiency, continue to be key performance parameters.

In this article, we present customized design solutions selected to meet specific requirements for a 200 W low output voltage and high output current power supply designed for redundant systems. This includes a new transformer configuration optimized for high current outputs that allows operation of multiple transformers in parallel with inherent current sharing but without additional control circuits. The individual transformers are custom designed for the applications but based on off the shelf core sizes.

A new rad-hard MOSFET optimized for low conduction loss is developed. When used for synchronous rectification and protection switch in series with the output it enables best in class power efficiency while ensuring the output is single point failure free for short circuit. The new die is packaged in the SupIR-SMD package which has very low thermal resistance from die to pads and can be soldered to a standard printed circuit board (PCB) using a normal reflow process.

## II. Motivation

A customer request for a specialized 200 W DC/DC converter initiated the development of a new product platform. Specifically the building height and power efficiency requirement for this product is critical and limits the number of suitable power transformers for the application. This lead to the development of a converter topology where a single primary side power stage drives two smaller power transformers with the primary side windings connected in series and the secondary sides including rectifiers are configured in parallel to facilitate a high output current. The key specifications for the converter are given in TABLE I.

TABLE I. Key Specification for DC/DC

| Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|
| Input Voltage | Steady state | 98.0 | 100.5 | V |
| Output Voltage | Steady state | 3.65 ±1.5% | | V |
| Output Current | Steady state | 0 | 55 | A |
| Power Efficiency | Load: 75% to 100%<br>I/F Temp: 25ºC to 58 ºC | 91 | | % |
| Outline<br>- height<br>- width<br>- length | Aluminum housing | | <br>20.6<br>140.1<br>162.1 | <br>mm<br>mm<br>mm |

## III. Converter Topology

The main criteria for the topology are: galvanic isolation, high power density and high power efficiency. The selected topology consists of a primary side full-bridge and a secondary side Hybridge rectifier, which is also known as the current doubler. The Hybridge rectifier can be implemented with diodes or as in this case synchronous rectifiers. As described in [1] the Hybridge rectifier can be implemented with an integrated magnetics (IM) where the two output chokes are wound on the same core as the transformer. This improves the power density compared to a solution with three separate magnetic components. With two output inductors operating in parallel and 180° phase shifted the output ripple frequency is twice the switching frequency which means the output ripple voltage is reduced. With individual synchronous rectifiers for the output inductors, each carrying half the output current, the topology is well suited for low voltage, high current outputs which is discussed further in [2].

### *A. Transformer and Power Stage Configuration*

The PCB holds all components needed and is populated on both sides to minimize the overall outline area needed. The outline height requirement limits the number of suitable magnetic cores that can transfer the required power. A solution with two modified E32/6/20 core-sets operating together to supply the full output power is selected. The core height needs to be reduced to fit within the required outline. This is done by milling the three legs so the effective core size is E32/4.5/20. Since the output has low voltage and high

current, the secondary side of the transformers are connected in parallel such each transformer and output rectifier set carry half the output current in order to reduce the conduction loss in the copper windings and output rectifiers. A simplified block diagram of the converter topology is given in Fig. 1 and the detailed schematic for the power stage and transformer configuration is given in Fig. 2

The selected PWM controller has generic part number UC1825. This controller is used in peak current mode with slope compensation and limits the duty-cycle for each PWM

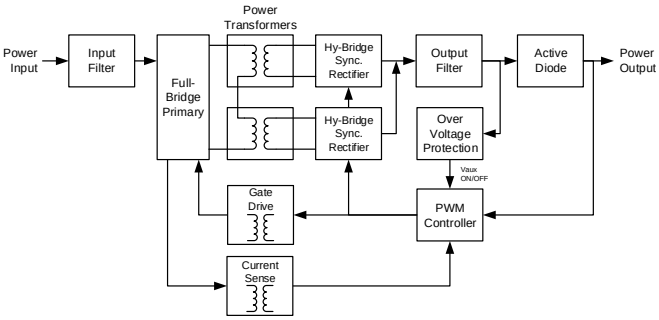


Fig. 1. Topology Block Schematic

output to $D_{max}$ = 43%. The duty-cycle limitation in combination with slope compensation prevents sub-harmonic oscillation. With limited duty-cycle and disregarding conduction losses the required transformer turns ratio can be expressed as a function of input and output voltage ($V_{in}$ and $V_{out}$) and the maximum duty-cycle:

$$n \leq \frac{V_{in,min}}{V_{out,max}} D_{max} \quad (1)$$

For the given input and output voltage the turns ratio becomes 11.37:1. Since the operational minimum input voltage is lower than the steady state minimum input voltage, the selected turns ratio is 10:1. This also leaves margin for the voltage drop caused by conduction loss. With a relatively high turns ratio and two transformers that need to share the load it is beneficial to place the primary winding of the two transformers in series and the secondary side including rectifiers in parallel. This gives inherent current sharing between the two transformers as long the primary turns are split evenly between the transformers. Furthermore, it is possible to reduce parts count and complexity of the regulation and PWM control circuits when the two IM primary windings are driven with a single primary power stage and PWM controller.

### *B. Control Scheme and Internal Supply Voltage*

Peak current mode control is used for controlling the output voltage. The PWM controller is located on the secondary side to allow direct sensing of the output voltage. The primary side switch current is measured and transferred to the secondary side with two current sense transformers, one transformer for each side of the full-bridge. Likewise, the

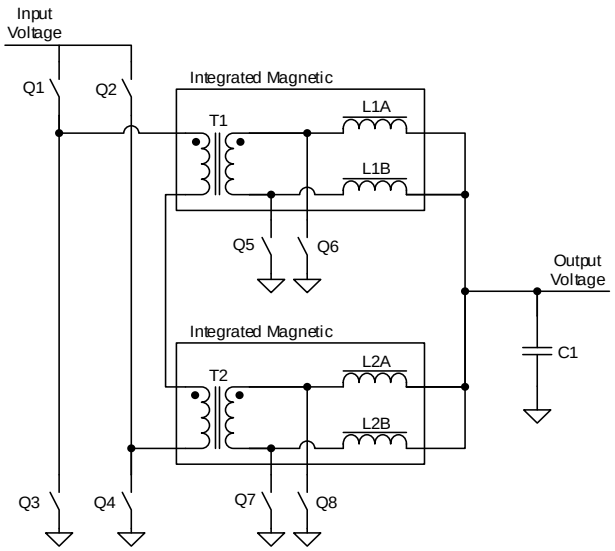


Fig. 2. Power Stage and Transformer Schematic

PWM signals are transferred to the primary side with a gate drive transformer. As the PWM controller is located on the secondary side a separate startup circuit is needed to establish a supply voltage for the PWM controller on the secondary side. For this purpose, a fly-back converter is used with the PWM controller located on the primary side. This also gives clear separation between the PWM supply voltage and the operational state of the main converter which makes operation during fault conditions such as short circuit of the output possible.

### *C. Protection Circuits and Redundancy*

Redundancy is established at system level using two identical converters with their outputs connected together to the same supply rail. In this configuration the DC/DC converter itself does not need any redundant circuit blocks and the requirements are therefore limited to ensure that no single point failure can propagate to the common supply rail. Only one of the two converters are turned on at a time and in the event of a fault in the primary converter the spare can be commanded on instead. This is referred to as a two for one cold redundant configuration. With a hardwired connection from both converters to the supply rail it is required that each converter is single point failure free for faults that can damage downstream equipment or cause permanent loss of the supply rail. This means that the converter shall not produce excessive over voltages or permanently short the supply rail to return.

An output over voltage monitoring circuit is included which removes the supply voltage for the PWM controller if an over voltage is detected. Likewise the onboard fly-back converter is equipped with an over voltage protection circuit to eliminate failure propagation from the internal supply voltages to the output.

An active diode circuit is placed between the output filter capacitors and the output terminals. The circuit consists of a MOSFET and a control circuit that regulates the voltage across source and drain. A simplified schematic of the active diode circuit is given in Fig. 3. If the source-drain voltage becomes negative, the PI regulator will turn off the MOSFET in order to break the connection.

The active diode circuit serves two purposes that both results in a negative source-drain voltage: The primary purpose is to protect the downstream supply rail against short circuit internally to the converter. The second purpose is to protect the converter against reverse current in the power stage. With synchronous rectifiers, the power stage is bi-directional which means current can flow from the output to the input. The peak current mode control scheme normally only supports current flow from input to output since the sensed current is diode rectified causing the PWM pulse to be

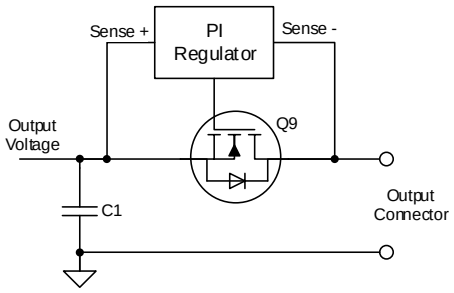


Fig. 3. Active Diode Schematic

terminated incorrectly if the current reverses. With a current sense transformer in each side of the primary side full-bridge it is possible to block the negative part of the current sense signal with a simple rectifier diode. This is not the case if a single current sense transformer is used to sense both sides of the primary side full-bridge because the sensed signal then has to be rectified with a diode full wave bridge rectifier.

When the negative part of the current sense signal is blocked it enables reverse current flow of half the ripple current in the output inductors. Ability to handle negative output current is required for this application in the event that both the primary and spare converters are on. If both converters are on current may flow from the output of one converter into the output of the other during the time it takes for the active diode regulator circuit to turn off the MOSFET.

A simple on/off active diode circuit without regulation can be used only if it can be guaranteed that only one converter connected to the common supply rail is on at the same time.

## IV. Main Transformer

The two identical main transformers are based on an E32/6/20 core set modified to reduce the building height. This core geometry is typically used for planar transformers with the windings integrated in the PCB. In this application, the windings are copper foils wound around the core legs as shown in Fig. 4. This construction is referred to as VerWin IM which is short for Vertical Winding Integrated Magnetic.

Since the windings are wound as a spiral and thereby layered on top of each other the proximity effect must be carefully considered. For the transformer section of the IM the proximity effect can be managed by interleaving primary and secondary turns. This is not the case for the inductor parts of the IM so instead the number of turns should be kept as low as possible. A low number of turns also reduces the DC resistance, which is desirable for low voltage and high current applications such as this one.

The IM only consists of the foil windings, the magnetic core and two mounting clamps. No coil former or pins are used and instead the core is clamped directly onto the PCB and the copper foils are soldered directly into the PCB. This helps reduce both electrical and thermal resistance from the core and windings.

## V. MOSFET for Rectifiers and Active Diode

In a high current low voltage application, the power conversion efficiency is highly dependent on the conduction losses in the devices on the secondary side. This is relevant for the IM windings as previously discussed as well as the

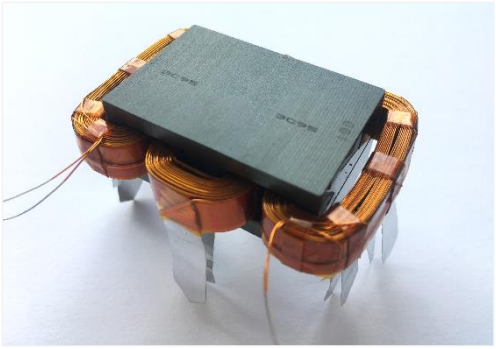

Fig. 4. VerWin Integrated Magnetic, Center leg holds the transformer windings, Side legs hold the output inductor windings.


Fig. 5. SupIR-SMD package selected for rectifiers and active diode MOSFETs.

synchronous rectifiers and active diode circuit. For a given technology, the MOSFET on-resistance (Rdson) is reduced by increasing the die size. Consequently, the gate charge and output capacitance of the device will increase as well which affect the switching loss. The switch timing of the synchronous rectifiers can be tuned to achieve soft switching and thereby reduce the power loss. The power loss due to gate charge, $P_{QG}$ is estimated by:

$$P_{QG} = Q_G \cdot V_{DRV} \cdot f_{sw} \quad (2)$$

Where $f_{sw}$ is the switching frequency, $V_{DRV}$ is the gate drive voltage and $Q_G$ is the total gate charge at $V_{DRV}$. For a given $Q_G$ the power loss can be reduced by lowering the switching frequency and the gate drive voltage. The switching frequency is closely linked to the magnetics design and a change will affect other circuit blocks such as control loop, input filter, and output filters. The gate drive voltage is determined by the gate-source voltage required to fully saturate the MOSFET. Selecting a MOSFET with logic level gate-source threshold is therefore desirable. Rad-hard MOSFETs with logic level gate-source threshold are available from IR HiRel's R8 technology series. The drain-source voltage rating is 20 V, which allows for a voltage derating of 55 % in this application. The R8 MOSFETs released at the time are designed for smaller applications such as point-of- load converters in the 10 A range and the die size as it is will not be able to handle the currents in this application.

Instead of paralleling five or more MOSFETs for each rectifier position, it was decided to scale the die size by a factor of 5 and package it in the SupIR-SMD package shown in Fig. 5. The packaged parts have an Rdson of 1.9 mΩ at room temperature and a gate charge of 118 nC at 5.5 V on the gate-source. The thermal resistance is 0.5 K/W from junction to the drain terminal, which is located under the package and soldered directly to the PCB in a normal reflow process. With the multiple layer base construction of the SupIR-SMD package it outperforms other hermetic SMD packages when subjected to thermal cycling. Detailed description and test results for the SupIR-SMD package are given in [3].

A single MOSFET is used for each of the four rectifier positions. Due to the transformer configuration, the rectifiers are effectively driven two and two in parallel. The RMS current in each of the four rectifiers is 17 A at full load which means the combined conduction losses for all four rectifier MOSFETs is 2.2 W at room temperature. For the active diode position, four MOSFETs are placed in parallel to reduce the power loss to 1.25 W at room temperature.

## VI. Measurements and Performance

In the following sections key measurements related to the selected topology and key performance parameters will be presented.

### *A. Transformer Configuration*

The selected topology with a single full-bridge driving two identical transformers coupled in series on the primary side and parallel on the secondary side, inherently have a resonance tank consisting of the synchronous rectifier output capacitances and the IM output inductors. When the rectifiers are off, the node impedance is high and a resonance is seen on the rectifier drain terminal as shown in Fig. 6.

The resonance is not affected by the load conditions of the converter and it can be dampened by placing resistors between the drain terminals of the synchronous rectifiers that are driven in phase i.e. between Q5 and Q7 and similarly between Q6 and Q8 (referring to Fig. 2). Fig. 7 shows the effect of adding dampening resistors between the drain terminals. The power loss in the dampening resistors is in the 20 mW to 30 mW range.

### *B. Active Diode Performance*

The active diode circuit regulates the drain-source voltage of the MOSFETs to approximately –3.5mV until the gate-source voltage is clamped and the MOSFET saturates with minimum Rdson. If the voltage across the active diode circuit becomes greater than –3.5 mV the gate-source voltage is pulled down to 0V to block reverse current.

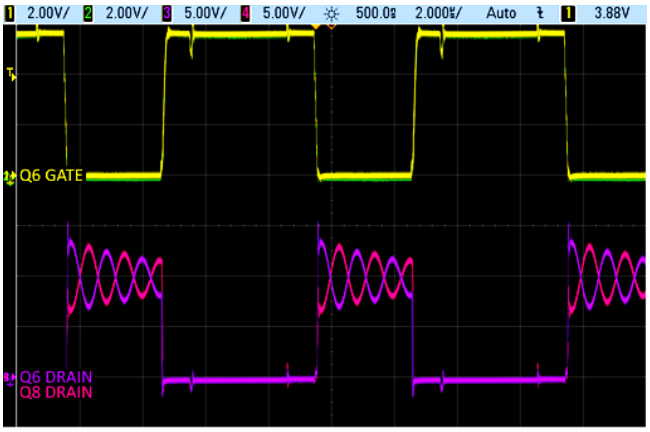


Fig. 6. Un-dampened resonance between synchronous rectifiers and IM inductors.

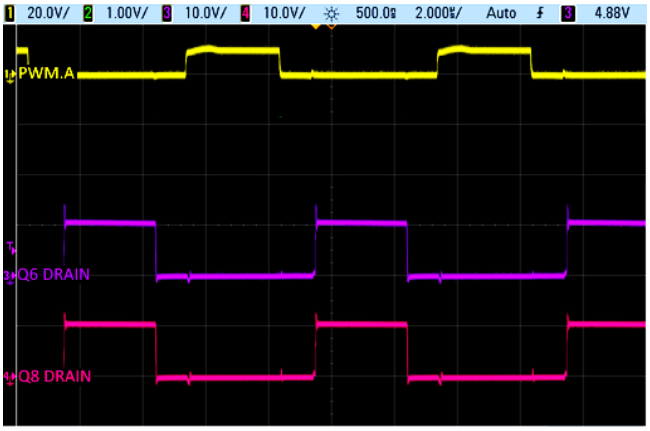


Fig. 7. Dampening resistors added between drain of synchronous rectifiers.

Fig. 8 shows the measured voltage across the active diode circuit as a function of output current. For reference the gate-source voltage is also shown. The gate-source voltage is clamped at 5.1V at which point the output current is just below 10A. As the output current is increased the drop across the active diode circuit becomes a linear function of the current since the MOSFETs are saturated with minimum Rdson .

The active diode circuit primary purpose is to protect the common supply rail against a single point failure such as shorted output capacitor internally to the converter. The performance is tested by shorting the output filter capacitors with a MOSFET while monitoring the output current and output voltage at the terminals of the converter. The result is given in Fig. 9. External capacitance is added to the output terminals, which is why the output voltage does not collapse completely after the active diode circuit has switched off to break the connection. The output current is 8 A prior to the short circuit test and during the 5 us transient response of the active diode regulator, the output current reverses and flows into the converter. In this case the reverse current reach 2 A.

### *C. Power Conversion Efficiency*

The converter efficiency is characterized across temperature and output current. Fig. 10 gives the measured efficiency which is greater than 92 % from 15 A to 55 A corresponding to approximately 30 % to 100 % of full load. The efficiency peaks with >93.5 % at around 55 % of full load. The requirement of greater than 91 % efficiency from 75 % to 100 % load is met at all temperatures.

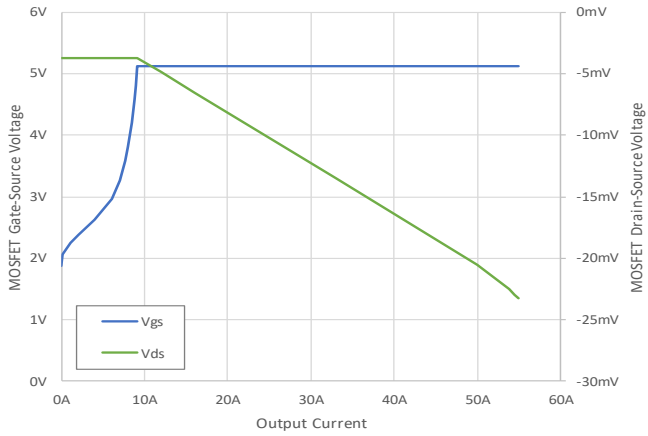


Fig. 8. Active diode circuit, measured drain-source and gate-source voltage vs. output current.

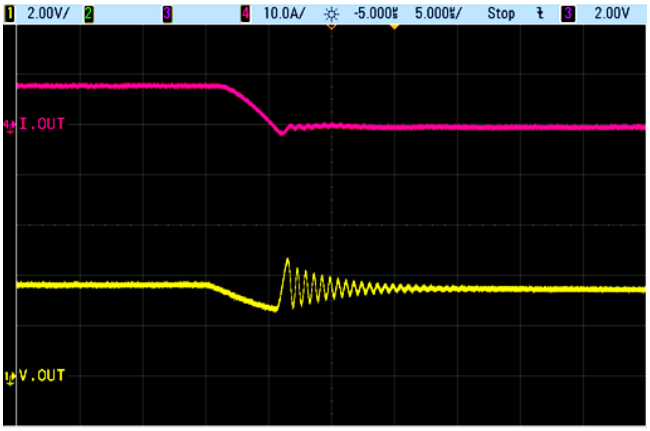


Fig. 9. Output voltage and current at terminal, during short circuit of output capacitor.

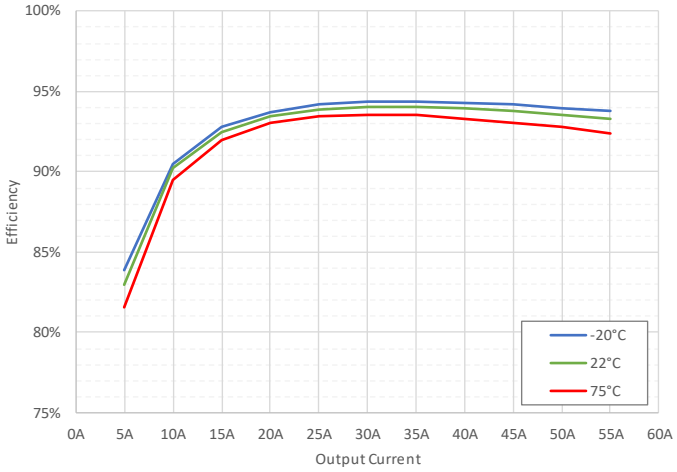


Fig. 10. Power Conversion Efficiency vs. Output Current, parametric with temperature.

All internal losses, including the active diode circuit in series with the power output, is included in the efficiency measurements. Best efficiency is seen in cold temperatures reaching >94% and the efficiency drops with up to 1 %-point for high temperatures compared to room temperature due to increased conduction loss in the transformers and MOSFETs.

## VII. Conclusion

A rad-hard low output voltage 200W DC/DC power supply suitable for redundant power systems has been developed and qualified for space flight. System reliability is ensured by using two identical converters that each include output over voltage protection circuits and an active diode circuit between the output filter capacitors and the terminals. The active diode circuit is based on a controlled MOSFET that blocks reverse current and ensures the downstream supply rail is single point failure free for a short to return internally to the converter.

A converter topology consisting of two smaller transformers with the primary side windings connected in series and the secondary sides windings connected in parallel reduce the building height and minimize conduction losses by having half the primary turns each. The topology inherently ensures current sharing between the parallel connected secondary sides because the primary side is driven by a single full-bridge, which is controlled by one PWM controller. Conduction losses are further reduced by using a tailored logic-level MOSFETs with an Rdson of 1.9 mΩ for the synchronous rectifiers as well as the active diode circuit.

The combination of selected converter topology, a customized integrated magnetics with foil windings and a new power MOSFET for synchronous rectification enables best in class power conversion efficiency of 93.5 % across temperature.

## VIII. References

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