International
IOR Rectifier

A Design Platform Optimized for Inner Loop Motor Control

Jay Goetz, International Rectifier, Minnetonka, Minnesota
Toshio Takahashi, International Rectifier, El Segundo, California

As presented at PCIM Europe 2003

Abstract

Motion control manufacturers today are under immense pressure due to global competition and regulatory constraints. Many, however, cannot retain the skilled people in house required to develop a complex motor drive product. This fact has actually created a thriving market for motion control consultants, but even though these consultants are usually skilled in the art, manufacturers cannot risk their reputation without some assurance of success.
A new approach is thus needed which reduces the schedule and technical risks in developing these complex power systems.
This paper introduces a new Motion Control Mixed Signal Chipset, which addresses the shortcomings of conventional development approaches, giving designers a powerful toolset for rapid prototyping of digital motor drives. Key technologies and merits are discussed based on the features it provides.

Accelerator™

The first product to utilize the Motion Control Mixed Signal Chipset, Accelerator™, follows the *Design Platform* model [1], proven to be so effective in the telecommunications and computer industries. In fact, it is expected that many manufacturers will adopt this approach to owning their own drive design because it is a "low pain" approach, even if they'll use it only infrequently, or if motor drive design is not their core competency.
Figure 1. shows the Accelerator™ AC Servo Design Platform, the first system product to use the new Motion Control Mixed Signal Chipset. This chipset uses a configurable hardware processor for inner loop motor control coupled with International Rectifier's advanced High Voltage IC (HVIC) gate driver and current sense interface chips. The flexible algorithm is implemented in FPGA, so that it can be structurally modified and tuned to quickly build high performance servo drive systems without any programming effort

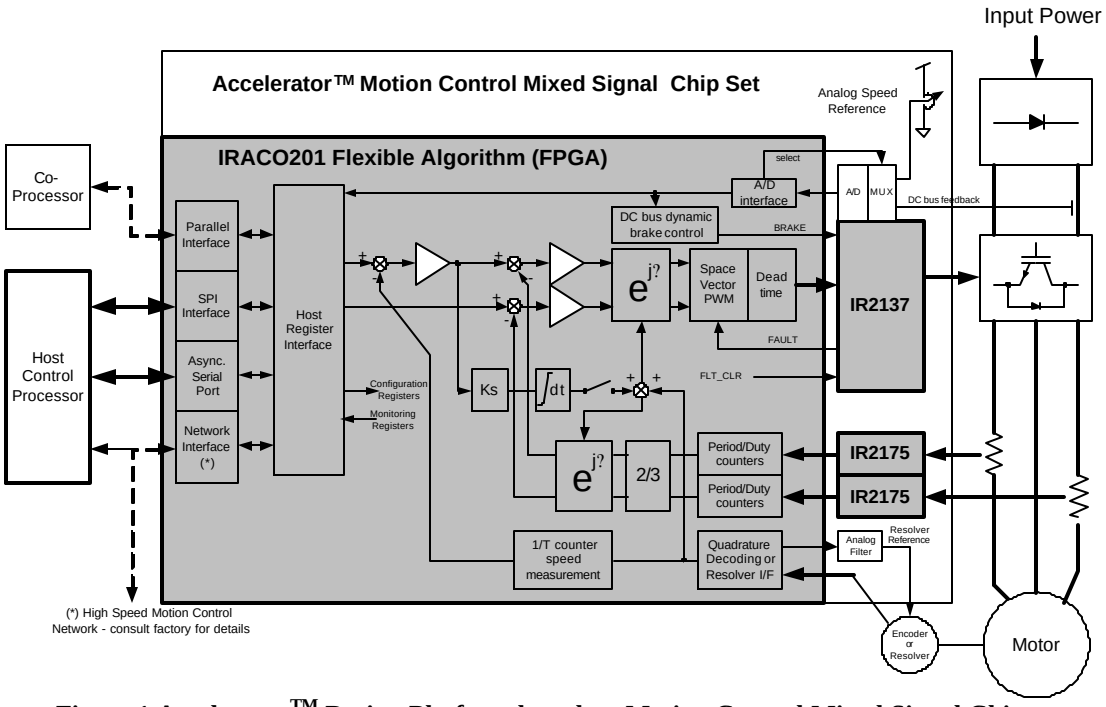

Figure 1 Accelerator™ Design Platform based on Motion Control Mixed Signal Chipset

Platform Technology

An effective Design Platform requires these key technologies:

?? Advanced Motion Control Mixed Signal Chipset - to increase functional integration and reduce cost.
?? High speed control processing for higher performance and to migrate more analog functions into digital control.
?? Configurable hardware processing to meet the need for greater flexibility and customization
?? Diagnostic tools which are non-intrusive and provide good visibility into the control loop.
?? Reliable hardware architecture to increase dependability of the eventual product

Advanced Motion Control Mixed Signal Chipset

A new Motion Control Mixed Signal Chipset is being introduced to implement inner loop motor control functions in hardware rather than in software, thus reducing latency and speeding up control loop execution. The current control loop, for example, executes less than 5 microseconds enabling high PWM carrier frequency update rates. The torque control loop bandwidth is 5kHz at –3dB point. This high bandwidth torque control is useful for high performance applications requiring high carrier frequencies (>10Khz) or applications, which cannot tolerate latency in the sensor-to-computed output process.

A major advantage of the Accelerator chip set is to help reduce design cycle time. Unlike a traditional DSP or microcontroller, the user does not need to design software programs to develop control algorithms. Rather, a flexible algorithm design is provided which is structurally modified and tuned using a powerful GUI called ServoDesigner. The entire process is reduced to a matter of hours instead of months or even years.

HVIC, Processor, and Power Stage

The Accelerator Design Platform employs HVIC technology, invented by International Rectifier in the late 1980's as a cost effective solution to high performance digital control of power systems. The latest HVIC product set consists of the IR2137 and IR2175. The IR2137 is a monolithic 600V high voltage gate driver IC with built-in over-current protection. A well-matched delay between phases, and between high/low sides allows the use of small deadtime, thus improving low speed performance.

The IR2175 is a monolithic 600V current sensing IC in a small SO8 package which doesn't require an A/D converter interface to the processor.

Critical pulse width generation and feedback timing cannot be handled adequately by software controllers, requiring dedicated hardware. These high voltage ICs are tightly coupled to a high speed configurable hardware processor (FPGA) to simplify the complicated design task of creating high voltage analog and power electronics circuits requiring gate drive, protection, and current sensing functions.

The power stage utilizes the IGBT module, rated at 600V/30A, which is an industry standard ECONO-style module and uses the latest short circuit protected IGBTs and fast recovery diode technology on a thermally advanced package design with DBC substrate and integral thermister temperature sensor, low inductance shunt resistors, an input 3phase bridge rectifier, and a motor brake circuit.

High Speed Control Processing

As more analog control loop designs have migrated to digital, the demand for fast digital processors has increased [2]. Digital Signal Processors (DSP) and microcontrollers, originally designed for communications and fast audio signal processing, were modified for real-time control duty to handle applications such as motor control. In fact, some control algorithm constructs, such as PID can be implemented efficiently as digital filters [3]. The peripheral-handling portions of these processors, control high-speed PWM generation with deadtime insertion, or high-resolution encoders, and require the raw speed that only dedicated hardware can provide. This deficiency has been handled by either adding a hardware section for control of the peripheral inside the processor, or by implementing this function external to the processor. Exclusive of the peripheral issue, the control loop software must be partitioned into several functions which are time-multiplexed tasks running at different rates depending on their required bandwidth and processing priority. Real-time Field Oriented Control (FOC) calculations are thus running along side background tasks, low priority scanned tasks along side fast feedback sensor processing tasks. A multitasking operating system or executive is

often used to manage all this context switching complexity, coupled with the DSP or microcontroller interrupt structure which all adds unwanted delay (latency) to important tasks required for motor control.

Figure 2 shows this dilemma from a system perspective. This is the structure of a typical cascaded servo drive control. Inner loop machine control functions, located toward the right side of the diagram require responsive processing, high update rates, and coordination with other real-time process. These torque control tasks are the ones that require a specific motion peripheral hardware element, and frequently use interrupts if a DSP or microcontroller is used.

Tasks that are closer to the host communication or man-machine interface side require less frequent update and can tolerate slow processing. However, they are usually more memory intensive and contain more sophisticated floating-point calculation such as for reference command generation. In addition, they tend to be very application dependent.

Software based DSPs or microcontrollers thus are not optimized to face the difficult and fundamental challenges in dealing with the variety of tasks required for high performance motion control. In order to achieve 5kHz torque bandwidth, for example, the torque control loop computation should execute in 20 microseconds. Figure 3, for example, shows the torque control performance for Accelerator™.

More advanced deadtime compensation, device protection response, accurate motor phase voltage feedback sensing, and current sensing are also increasingly important functions which require fast computation, tightly coupled with mixed signal digital hardware logic and analog circuitry. The high-speed logic for good PWM timing requires nanosecond resolution and needs dedicated logic such as CPLDs or FPGAs. The range and diversity of processing requirements shown in Figure 2 indicates that a new approach is required to address these types of control systems. This approach should address the timing-critical portion of the control by using dedicated hardware resources.

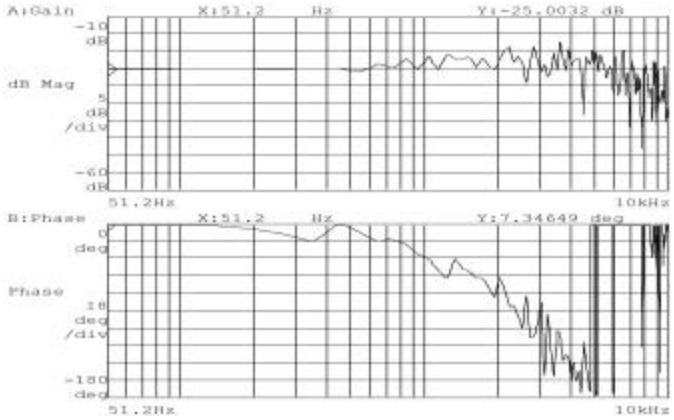

Figure 3 Torque Control Bandwidth of Accelerator
(extra 22° phase shift due to measurement setup)

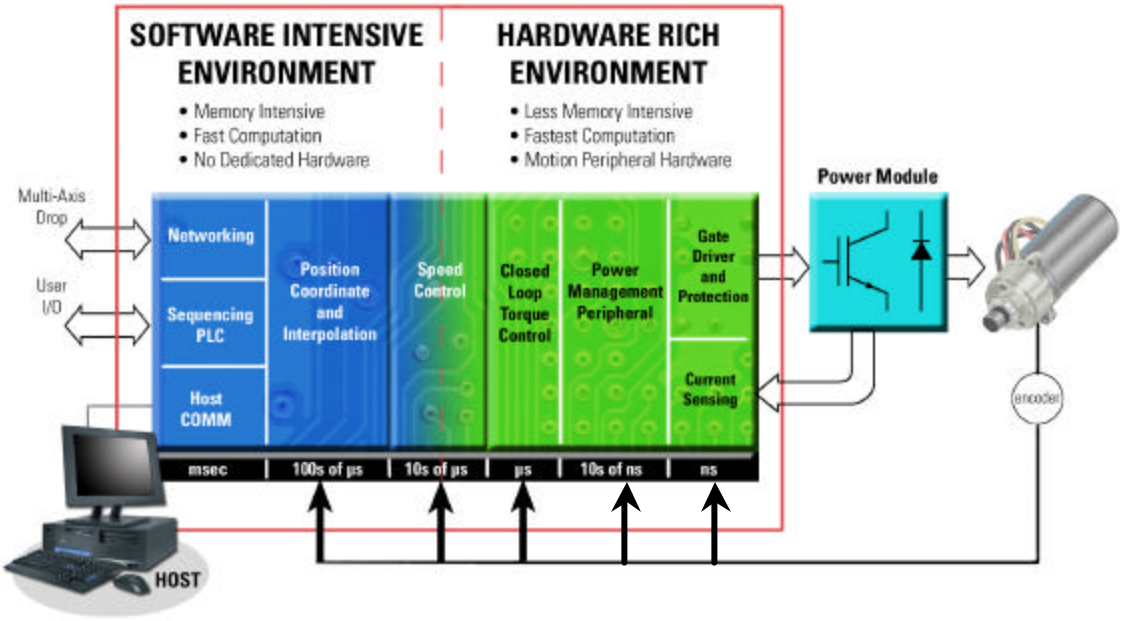

Figure 2 Servo Motor drive functions

Configurable Hardware Processing

Flexibility of the drive design is obtained by these three means:

- ?? An adjustable FOC algorithm with host computer access to all important drive parameters, monitor points. Included should be the ability make some of the more common changes to the algorithm structure without changing the code.
- ?? Allowing customization of the fundamental algorithm structure by building it from a library of motion IP core modules
- ?? Expressing the algorithm design in a clear block diagram format for understandability, preferably one which shows control action*
- ?? Use of a configurable hardware processor, an FPGA

*Web and PC based tools are being developed to show dynamically how the controller behaves and controls the motor.

The pre-configured adjustable algorithm is described by a system block diagram, which clearly shows how the control acts on the various data paths, giving the user better understanding of system behavior. This enhanced system perspective is important in creating robust controls, with fewer soft failures. These subtle types of failures typically occur in digital systems designed from scratch (using conventional design tools) due to inadequate software engineering, particularly in failure to properly test the design, both as it is being built and then at integration with hardware platform, motor and load conditions.

Figure 4. shows the flexible digital FOC architecture used in Accelerator™

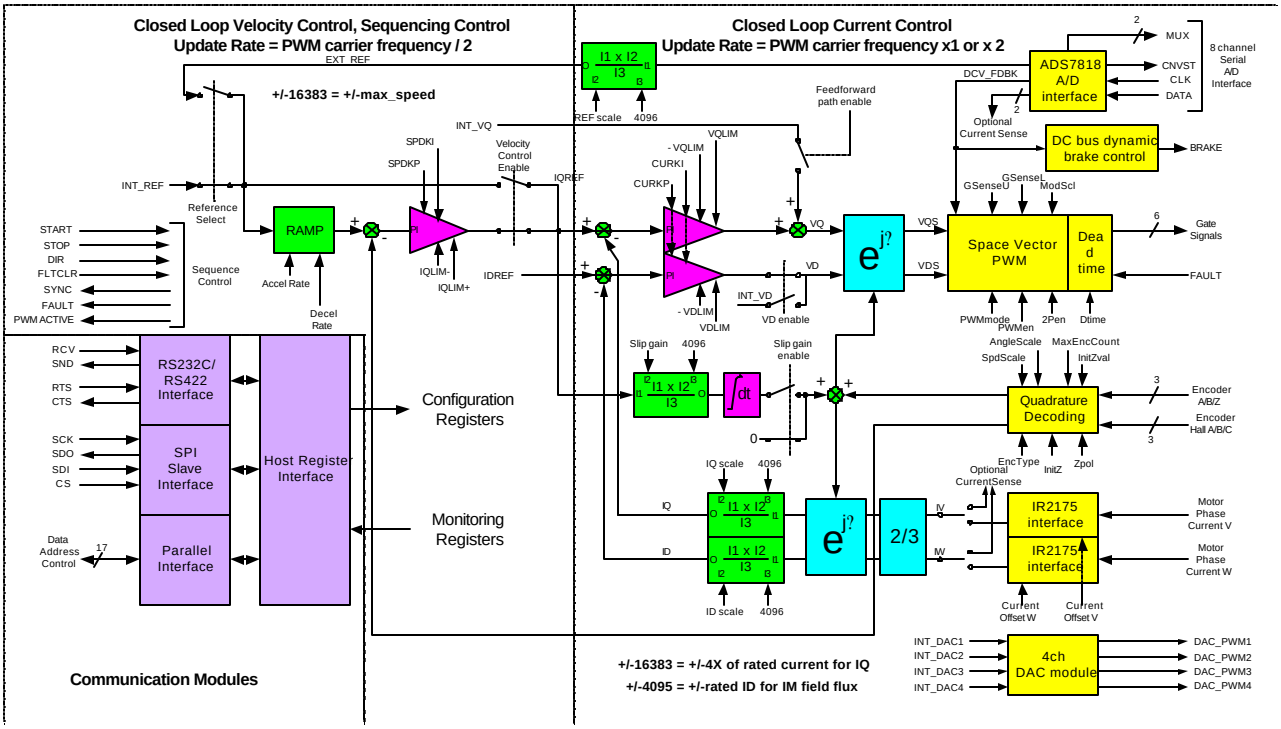

Figure 4. FlexibleFOC Algorithm

Re-configurability and Customization

As discussed, traditional software based computers have a processing engine at their core which is designed to perform a diverse range of functions combined with a set of I/O peripherals. These resources are "fixed" in hardware and cannot be changed. Since the "one size fits all" axiom doesn't apply to motor drive control, this results in suboptimal processing for specialized tasks which motor controls require involving high speed timing, and low latency, intensive computation. The processing tasks required for inner loop motor control thus fall into the area of being hard to implement, hence creating the need for an optimal motor drive Accelerator™.
Another drawback of the fixed core and peripherals is that this architecture is unable to support changes, as newly created peripheral functions are required to be processed by the dedicated hardware. An example in servo motor control is in changing from a 6 line incremental encoder to a 14 bit parallel absolute encoder or a resolver, which requires an A/D interface function. Manufacturers using software-based controllers typically have to go through the painful and costly process of re-hosting on a new DSP or Microcontroller to gain the specialized processing capability they need.
Change is in the wind. Fueled by a new technology called re-configurable computing technology, application of this powerful technology has just begun in the power system world though it has been commercialized extensively in other applications such as communications and multimedia signal processing. Processor re-configurability or (configurability) brings with it the concept of flexible hardware, which is now available to power system designers thanks to use of FPGAs. Designers and users are now able to shape the hardware according to the application at hand. This means that a new hardware design (hardware object) can be downloaded into the reconfigurable processing unit, which processes that application more effectively and efficiently. It is truly a powerful technology enabling major improvements in real time control systems.
Using the flexible approach that Accelerator provides, users can focus on their application rather than on rigorous software design methods requiring expertise with complex tools.
Detailed module testing of the design by the user is not required because this has been done while the FOC design was being built. Tests were carried out on a module level using digital simulation tools followed by system level testing as a whole using real motors and load conditions. The result is that implementation of the design is much easier because the algorithm is flexible, and it's structure and control behavior is better visualized. Use of the ServoDesigner configuration tool described later in this paper streamlines the process even further.

FPGAs as Control Processors

Field Programmable Gate Arrays (FPGA) provide the processing hardware infrastructure for implementation of customized designs. These are raw silicon logic engines, which can be programmed by designers or users to suit a broad range of applications for unlimited number of times. FPGA configuration code can be downloaded either from an external program or local stored memory. In Accelerator™, hardware object libraries are kept on a host computer for creating and downloading into the target execution hardware, which is a full function motor drive. The processor can be configured for specific functions (especially computing intensive tasks) without changing the physical component hardware. Up until recently, reconfigurable computing hardware was used only for coprocessors for the main CPU to optimize performance and off-load the main CPU. Accelerator™'s Motion Control Mixed Signal Chipset takes this a step further and pulls the inner loop control functionality and peripherals out of the main CPU, placing them into dedicated silicon in the FPGA hardware. FPGAs, used for this purpose, provide several advantages:

- FPGA's allow hardware designs to be re-configurable, including peripheral functions.
- FPGA's can process information faster than a general purpose DSP of the same vintage, especially when parallelism is used.
- Controller architecture can be optimized for space or speed or a mixture of both
- Bit widths for data registers can be selected based on application needs, and are easily upgraded
- HDL files are portable across different FPGA's

There are a few disadvantages:

- Priced Higher than some of the low end DSP's and microcontrollers
- Not commonly available in small pinout packages.
- Maturity of tools is behind software based DSP's

Improvements are being made in FPGAs to erase these disadvantages. Increased sales of configurable processors have driven leading FPGA vendors to launch chip designs on the latest commercial deep-submicron processes making them more competitive with the high-speed general processors in development. In addition, more functionality is being integrated over time, such as embeddable processors, memory, communication, and math structures to enhance integration. In addition, costs of large scale FPGAs are now beginning to come in line with DSP solutions.

Scalable Parallel Digital power control

Comparisons made between high-speed software based processors and FPGAs have shown at least rough parity for single thread control processing, even when the FPGA was built on an older technology [4]. The following data shows performance results comparing fault tolerant designs for a robotics application in which processing is done by a general purpose processor (Table 1) or by an FPGA (Table 2) The interesting result shown in these tables is that there is a great advantage in arranging the tasks to run in parallel in the FPGA.

# of Modules	1	2	3
LUTs (total 3888)	404	819	1284
Registers (total 2592)	115	230	345
Frequency (MHz)	24	26	22
Latency (microseconds)	0.042	0.038	0.045

Table 1 Performance of Xilinx FPGA processors based on .35?micron technology

# of Copies	Latency (microseconds)			
	Ultra SPARC[3] (300MHz)		Pentium II Xeon (450MHz)	
	Float	Fixed	Float	Fixed
1	0.184	0.099	3.866	0.033
2	0.290	0.376	7.699	0.080
3	0.462	0.646	11.704	0.126

Table 2 Performance of General Purpose Processors based on .25micron technology

Diagnostic tool

ServoDesigner meets the need for control diagnostic testing including complete access to all internal registers, embedded buffering of test parameters, and graphical Per-cycle test point monitor

Using ServoDesigner, the user has the ability to change not only parameters and variables but can also alter the control structure of the system without any programming effort. Structural and parameter changes are accomplished by selecting optional hardware logic switches through the RS232C communication port using the ServoDesigner application running on a PC. Once configuration is completed, parameters can be stored in the EEROM to facilitate rapid power-up-and-run operation

Configuration switches are available for:

- ?? Velocity Control Enable/Disable
- ?? Slip Gain Enable/Disable (PMAC or induction machine)
- ?? Hall A/B/C Initial Position Feedback Select
- ?? Current Feedback Interface Select (IR2175 or generic analog input interface)
- ?? CEMF Feed forward Gain Enable/Disable
- ?? Reference Input Select

Three diagnostic constructs are available on ServoDesigner's configuration page:

- ?? Register definitions
- ?? Functional definitions
- ?? Monitor definitions

These can be saved to a text file, so you can maintain and archive multiple versions of your configurations and share them with other members of your team.

Figure 5. shows the ServoDesigner configuration page, used to assist all stages of your motor drive development. When you first install the Accelerator product for example, you can use ServoDesigner to verify proper operation of the equipment and experiment with different motor configurations and settings. You can modify the pre-defined motor functions and monitoring configuration (trace setup, including channel select and trigger setup) and you can add your own functions to test various aspects of your new design using the included looping and delay constructs.

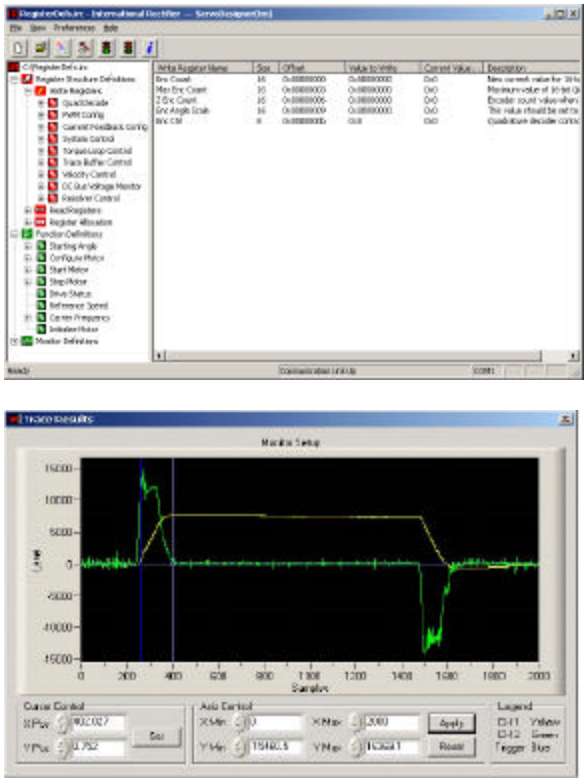

Figure 5 ServoDesigner screenshot, with real time scope display of speed and current waveforms

In summary, ServoDesigner can be used to:

- ?? Verify installation and test the reference design
- ?? Configure motor parameters and validate setup
- ?? Test FPGA design under different load and performance conditions
- ?? Capture and display real-time motor function and performance

Reliable Hardware

Accelerator™ hardware platform, the IRACS201(Figure 6), contains the complete embedded FOC control code, optimized for velocity and torque control, and is based on a single control board with separate power stage. The simple and low cost design is made possible by International Rectifier's Motion Control Mixed Signal chip set including the FPGA, IR2137 monolithic 3-phase gate drive high voltage IC, and IR2175 monolithic current sensing high voltage IC. These three ICs are directly connected, which in this minimal design, requires no other IC components to perform complete servo amplifier functions.
Once the user is satisfied with function and performance, a unique design can be created, based on the schematics and BOMs, which are also provided with the IRACS201.

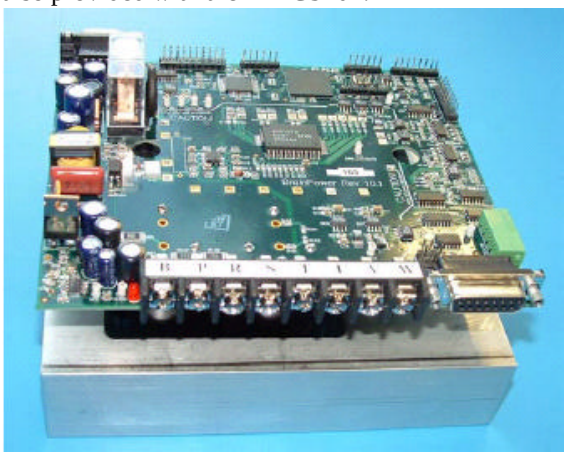

Figure 6 IRACS201 shown with heat sink for 1.5KW operation

Table 4 shows the different power ranges and voltage levels that Accelerator Design Platform can accommodate

Power Rating	750W	1.5kW	3.7kW
Product	IRACS202(*)	IRACS201	IRACS201 (larger heatsink)
Continuous Rating	3.3Arms 230V	8Arms/230V	13Arms/230V
Peak Rating	10A(rms)230V	22Arms/230V	30Arms/230V
Gate Drive	(HVIC in development)	IR2137	IR2137
Current Sense	(HVIC in development) + low side shunt resistor	IR2175 + shunt resistor	IR2175 + shunt resistor
FPGA	SpartanIIE-300 (XC2S300E-6-FT256C0823)	SpartanIIE-300 (XC2S300E-6-FT256C0823)	SpartanIIE-300 (XC2S300E-6-FT256C0823)
IGBTs	Discrete IRGB10B60KD	Module GB30RF60K	Module B50RF60I

Table 4 Hardware Platform Ratings Available
* This platform version will also support low voltage operation using Mosfets.

Application

Typical application connection diagram of the Accelerator™ platform is shown in figure 7. This diagram shows the IRACO201 Soft ASIC Object Code with Spartan2 FPGA interfacing to all the I/O peripherals.
Although this is a typical hardware configuration, users can adjust the design parameters without significant re-programming effort. As an example, motor current sensing can be done in different ways. While IRACO201 provides direct interface to IR2175 high voltage current sensing ICs, the user can still interface to other current sensing devices such as Hall Effect sensors and/or a low side shunt resistor.

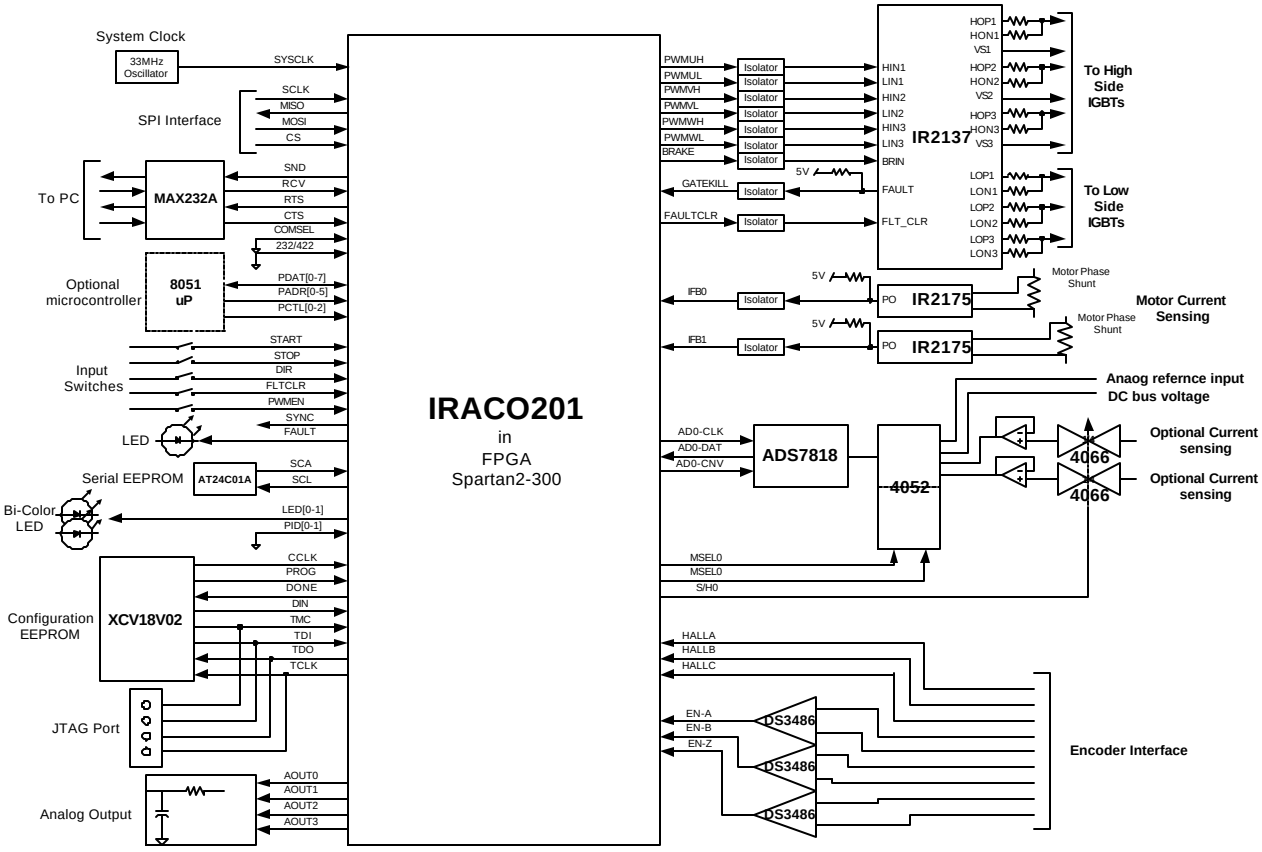

Figure 7. Application Connection of IRACO201

Accelerator™ is finding use in numerous applications demanding high performance:

- ?? Spindle control - NC machine tools
- ?? Process Servo control - material handling systems such as semiconductor wafer handling
- ?? Robotics –single and multi-axis manipulator control, propulsion control
- ?? Flight Control –actuation of control surfaces, fins, thrust direction, valve/vane actuation
- ?? Space/Aerospace – antenna control, inertial control
- ?? Ground Vehicle Propulsion – Turbine/Engine/Fuel cell driven motor control, transmission, electric power steering
- ?? Medical/Pharmaceutical – Diagnostic scan, dental/orthopedic, robotic test/manufacturing tools
- ?? Automated Assembly/Factory Automation – Wire bonding, PCB drilling, Pick-and-place assembly
- ?? Special Testing – disk/tape drive testing, motor testing

International
IOR Rectifier

Summary

The Accelerator™ Design Platform is based on International Rectifier's new Motion Control Mixed Signal Chipset, which provides a fast design solution for high performance AC servo amplifier application without any programming effort.
The "soft ASIC" approach used in the IRACO201 Object Code Design allows users to rapidly configure and optimize the system for each application's specific needs.
An industrial quality pre-configured Hardware Platform, the IRACS201, is available with International Rectifier's latest HVICs such as IR2175 current sensing IC and IR2137 3-phase gate drive IC.
A complete servo toolbox, the IRACV201, with source code library and including the IRACO201 FOC design is also being introduced, allowing users to customize their servo designs using IP Core system design methodology.
Future products include additional application-specific platform chipsets incorporating technologies such as sensorless control and integral EMI control, and ASIC based solutions for very low cost or high volume solutions.

References

[1] "Integrated Design Platform for Digital Motor Drives", David Tam, International Rectifier, http://www.irf.com.
[2] "FPGA Based High Performance AC Servo Motor Drive - Accelerator™ ",Toshio Takahashi, International Rectifier, http://www.irf.com.
[3] "PID Controller Design For Field Programmable Gate Arrays", James Bonanno, International Rectifier, http://www.irf.com.
[4] "ACS Implementation of A Robotic Control Algorithm with Fault Tolerant Capabilities", Shu-Yi Yu, Nirmal Saxena, and Edward J. McCluskey, Stanford University