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A New Half-Bridge High Voltage Monolithic IGBT Gate Driver with Full Protection and Diagnostic Feedback

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Abstract

A new half bridge gate driver IC for high voltage applications developed in high-voltage CMOS technology is described.

It includes two driving stages able to source and sink 2A and 3A respectively: one driver is referenced to ground voltage, while the other may float up to 1200V above the former.

The IC integrates the full digital section to interface a 3.3V controller and includes a set of features to protect the IGBT in case of under-voltage at main supply or short circuit at the output managing multi-phase systems and to prevent shoot-through events.

Diagnostic information is provided through I/O pin.

1 - Introduction

This paper presents a new generation of monolithic half-bridge gate driver characterized by high output current capability and very low quiescent current.

The innovative inverter output stage is able to source up to 2A and sink up to 3A driving large IGBT in the suitable way.

The device includes the IGBT de-saturation detection with a novel scheme to improve the biasing of the external sensing diode while decoupling noise generated by the switching power bridge. When a de-saturation is detected, the soft shut down turns off the respective IGBT in smooth mode preventing over-voltage and reducing EMI emissions.

An innovative solution achieves the soft shut down synchronization in a 3-phase system enabling phase-to-phase short circuit detection and management.

The open drain 3.3V compatible CMOS I/O pin reports relevant diagnostic information to the main controller.

These performances are achieved using IR 1200V CMOS technology.

2 - Integrated circuit block diagram

The block diagram of the devices is shown in fig.1.

The input stage is an Schmitt trigger comparator 3.3V compatible with minimum hysteresis of 1.6V for high noise immunity.

Suitable solution has been introduced to use the device in high power application where coupling between power and signal ground have to be avoided.

Signal and power grounds of the low voltage reference stage are separated: the power ground pin (COM) can float ±5V respect to signal ground (VSS) decoupling noise generated by the high current output stage.

The input logic checks the input signal preventing shoot through events and including 300nsec dead time.

The under-voltage function detects main supply failures, disabling the low side IGBT and generating a diagnostic signal at the FAULT pin. In the high side, the under-voltage function disables the IGBT driving stage but does not disable the low side IGBT, in order to prevent proper bootstrap startup procedure. For this reason, floating stage supply failures are not directly reported to FAULT pin.

The over current is detected sensing the de-saturation of the IGBT. When IGBT Vce increases above the comparator threshold, the main output driver goes in high impedance and the IGBT is smoothly turned off via the soft shut down driver pin, reducing transient over-voltage on the DC-BUS and EMI emissions.

The faults are reported through an open drain bi-directional output (VCC/60Ω) also used to get the shut down signal 3.3V level compatible.

The over-current fault is internally latched, and can be reset via the FLT_CLR pin.

3 - Output stage

The output inverter stage offers a rail-to-rail output voltage.

The structure is showed in Fig.2 and consists of two turn-on (Pch) stages and one turn-off (Nch) stage.

When the driver turns on its output (HOP), a first 15Ω equivalent stage is constantly activated while an additional 15Ω is maintained active only for a limited time of 200nsec. This feature enhances the total driving capability in order to fit the power switch driving requirements, enabling fast charge up to the plateau voltage, then reducing dV/dt in commutation.

At turn-off, a single 5Ω Nch sinks up to 3A and offers a low impedance path to kill the self turn-on due to the parasitic Miller capacitance in the power switch.

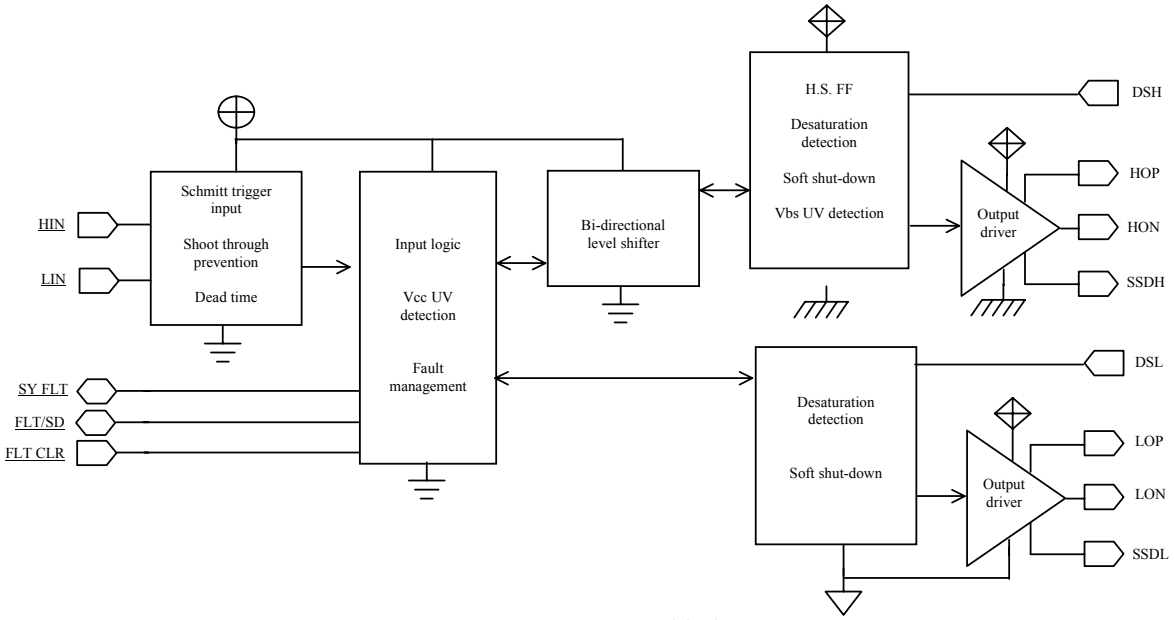

Fig.1: Block diagram

The propagation delay matching between on and off command reduces the PWM distortion in precise drive control.

3 - Soft Shut Down (SDD) and Synchronization fault features

Both the high side and low side IGBT are protected by over current by the Vce desaturation detection and soft shut down function.

The fig.2 shows the structure of the desaturation sensing and soft shut down block.

The over current is detected sensing the collector-emitter voltage of IGBT at the on condition through an external diode (BV>1200V), then the Vce is compared with a fixed 8V threshold, afterwards the resulting signal is filtered for 1μsec.

A blanking filter of 3μsec is used to don't consider the effect of the tail at the turn on of the IGBT.

Once de-saturation is detected, the output stage goes immediately into a high impedance state and the SSD driver is activated, turning off the IGBT through the SSDH/L pin with the proper impedance.

SSD events holds for 7μ sec to achieve smooth IGBT gate discharge at high collector current level. An external resistor can control discharge impedance through the dedicated SSD pin on top of a minimum 75Ω internally provided.

The short circuit detection information is shared with the other drivers through the SY_FLT I/O pin. In this way the main driver (the once detecting the short circuit) communicates with the other drivers in the local network. Once active, this signal freezes the all the other drivers status on the output regardless of the status on the inputs. The main driver itself freezes its status until the SSD takes place.

When the soft shut down is over, SY_FLT signal is disabled and diagnostic information is sent by FAULT/SD pin to micro-controller, then the main driver pulls down the FAULT/SD line forcing an hard shutdown itself. By means of the FAULT/SD pin all the other drivers in the local network are switched off and the faulty condition is reported to the main controller for diagnostic purposes.

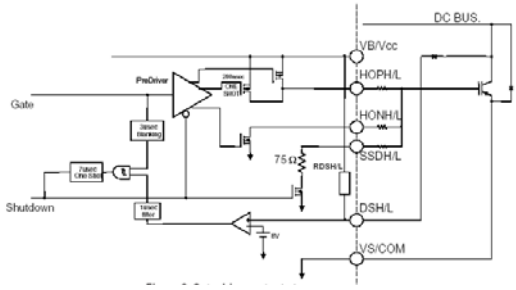

Fig. 2. Output and SSD stage, Desat sensing

4 - Active bias

To reduce the noise injected by the sensing diode connected to the power switch collector/drain, an active biasing of DSH/L function is introduced.

The noise is normally due to the parasitic capacitance associated with the high voltage sensing diode. The relevant dV/dt applied by the power transistor during the commutation at the output results in a considerable current injected through the diode's capacitance into the de-saturation detection pin (DSH/L).

The DSH/L pin present a pull-up resistor of 100kΩ respectively to VB/VCC, and a pull-down resistor of 700kΩ respectively to VS/COM.

The dedicated biasing circuit reduces the impedance on the DSH/L pin down to 90Ω when the voltage exceeds the 8V threshold (with 1V of hysteresis). This low impedance helps in rejecting the noise providing the current inject by the parasitic capacitor. When the power transistor is fully on, the sensing diode gets forward biased and the voltage at the DSH/L pin decreases. At this point the biasing circuit deactivates, in order to reduce the quiescent current at the on status.

Furthermore, being the biasing circuit integrated, the de-saturation detection does not require any other external components than the high voltage sensing diode.

The Iqbs (quiescent VBS current) required is only 800μA, allowing bootstrap supply solution for the high side stage.

5 - Package

The device is packaged in SSOP-24.

The high side pins and circuit are placed on a single side of the silicon die. In this way the high voltage and the low voltage pins are separated by the full package body width offering the higher creepage distance in the PCB layout.

6 – Conclusion

A new 1200V half-bridge gate driver with complete diagnostic has been implemented in HV CMOS technology. The IC layout, whose die size is 3.42X4.21=14.4mm2, is illustrated in Fig.3.

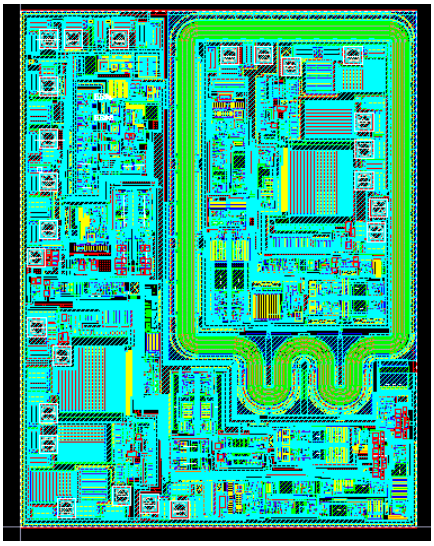

Fig.3. Micro layout of device