

From Planar to Trench - Evaluation of Ruggedness across Various Generations of Power MOSFETs and Implications on In-circuit Performance

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Abstract—In this paper we compare the ruggedness of various generations of power MOSFETs using three criteria - single-pulse avalanche robustness, forward-biased safe-operation-area (FBSOA), and body-diode reverse recovery ruggedness. We observed that the trench-gate FETs are generally inferior to planar-gate counterparts in both FBSOA and avalanche capabilities; however, both trench and planar FETs show comparable performance under certain test conditions. Moreover, the trench FETs evaluated in this study are superior in reverse recovery ruggedness.

I. INTRODUCTION

This paper evaluates single-pulse avalanche capacity, FBSOA, and body-diode reverse recovery ruggedness on different generations of middle-voltage MOSFETs. By pointing out the strengths and weaknesses of existing generations, this evaluation will provide knowledge that users need for properly selecting and better utilizing existing MOSFETs technology.

Knowing that MOSFET ruggedness depends heavily on test condition, device voltage, die size, and many other factors, we choose different generations of devices that have the same voltage-ratings, the same packages, and approximately the same die sizes to ensure silicon design generation is the sole factor of differences in the ruggedness performance.

The parts chosen for the testing are listed in Table I are all TO220 packages. Parts A1 to A5 are 100V rated with similar die sizes varying from 15.3 to 16.9 mm²; while parts B1 to B4 are 55V-60V rated, with similar die sizes varying from 5.3 to 6.2 mm². Comparisons were made separately among the devices with the same voltage ratings. The generation information of each part is in the fourth column with the smaller number indicating an earlier generation. Note that, Generations G5 and G7 are planar parts, while G8 to G10 are trench parts. The fifth and sixth columns show that a newer generation has lower $R_{DS(on)}$ and higher I_D rating than an older one.

TABLE I: Parts selected for the comparison

Device	Voltage (V)	Die Size (mm ²)	Generations	Rdson (mΩ, 10Vgs)	I _D (A)
A1	100	16.83	G5, planar	36	42
A2	100	15.35	G7, planar	23	57
A3	100	16.26	G8, trench	14	75
A4	100	16.94	G9 trench	10	96
A5	100	15.35	G10, trench	9	97
B1	55	5.70	G5, planar	40	26
B2	60	5.70	G7, planar	26	30
B3	55	5.33	G9, trench	13.6	51
B4	55	6.25	G9, trench	11	61

II. SINGLE PULSE AVALANCHE PERFORMANCE

A. Unclamped Inductive Switching (UIS) results

Increase-to-fail Unclamped Inductive Switching (UIS) test was used for characterizing avalanche ruggedness in our evaluation. The test was taken under eight conditions: two ambient temperatures (25°C and 175°C) and four inductors (20, 50, 100 and 500 μH). The detailed circuit and operation of the UIS tester can be found in application note [1]. A typical increase-to-fail UIS waveform is shown in Fig. 1. The part starts to operate at avalanche mode when the V_{DS} exceeds its break-down voltage. The peak inductor current or I_{AS} gradually increases till the part fails. The highest I_{AS} at 20 μH, 25°C and 500 μH, 25°C are listed in Table II.

For a rugged MOSFET without parasitic bipolar transistor effect, some references suggested that the avalanche failure is thermally induced. It occurs when the cell temperature reaches a critical value, beyond which the intrinsic carrier concentration exceeds the epi doping concentration [2]. Based on this understanding and the fact that the single-pulse thermal impedance curve of a MOSFET normally presents a constant slope in certain time ranges, we can conclude a linear relationship between I_{AS}

and the inductance (or between I_{AS} and T_{AV} , the avalanche time) in a log-log scale [3].

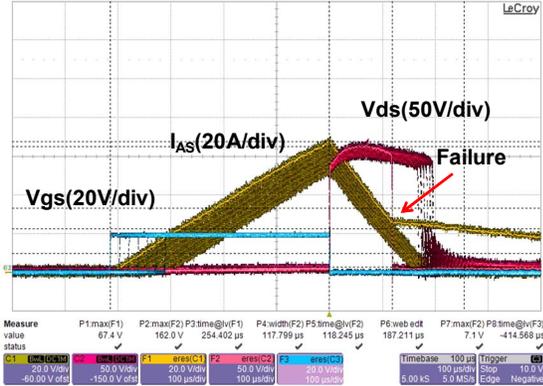


Figure 1. Typical increase to fail UIS waveform

TABLE II: Comparison of I_{AS} across parts

Device	$V_{BR(DSS)}$	I_{AS} (A) @20 μ H, 25 $^{\circ}$ C	I_{AS} (A) @500 μ H, 25 $^{\circ}$ C
A1	100	233.22	62.86
A2	100	195.36	64.16
A3	100	81.16	61.62
A4	100	84.62	61.44
A5	100	138.33	55.96
B1	55	106.30	35.16
B2	60	105.58	37.38
B3	55	114.46	34.82
B4	55	125.06	39.14

Figs. 2a-2b and 3a-3b separately compare I_{AS} of parts A1-A5 and B1-B4 with respect to the inductance under two different ambient temperatures (25 $^{\circ}$ C and 175 $^{\circ}$ C). Fig. 2a and Fig. 2b suggest that 100V planar parts have much higher I_{AS} with smaller inductors, exhibiting more robustness than their trench counterparts do; while with larger inductors, the difference between planar and trench parts is small. The dramatic fall-out of A3 and A4 (the two old trench technologies) in comparison to A1-A2 (the newer technologies) is most likely caused by the parasitic BJT, which is more prone to turn-on at high currents. In contrast, Fig.3a and Fig. 3b show that, for 55-60V parts, planar and trench parts have very close avalanche performance under all tested conditions.

B. Analysis of results and correlation to device physics

The test results obtained from the testing indicate that the newer Generation 10 trench devices have a much improved avalanche behavior compared to the older generation 8,9 trench devices. This is attributed to the design of the device structure that modifies the p-body region doping concentration through the addition of a deep P⁻ implant. The P-body now extends beyond the bottom of the trench. Additionally an N-implant at the base (tip) of the trench is also added. It is higher in concentration than the N-epi and usually similar in concentration to the P⁻ implant.

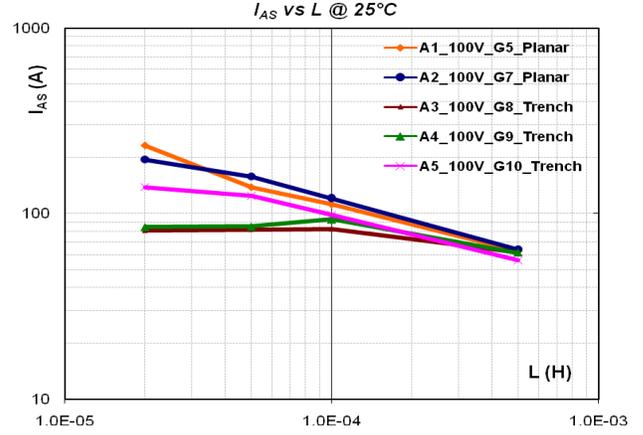


Fig. 2a I_{AS} vs inductance for devices A1-A5 under $T_A=25^{\circ}$ C

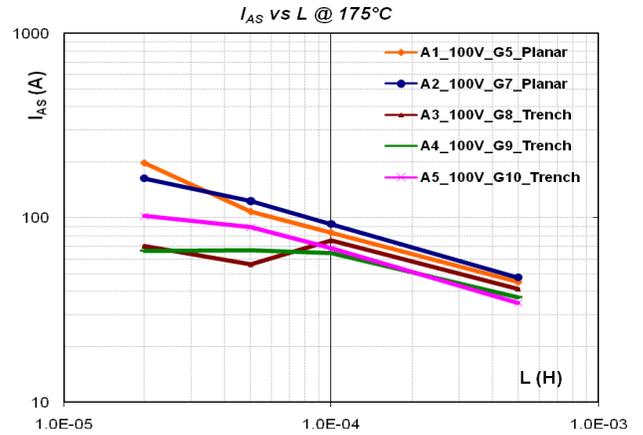


Fig. 2b I_{AS} vs inductance for devices A1-A5 under $T_A=175^{\circ}$ C

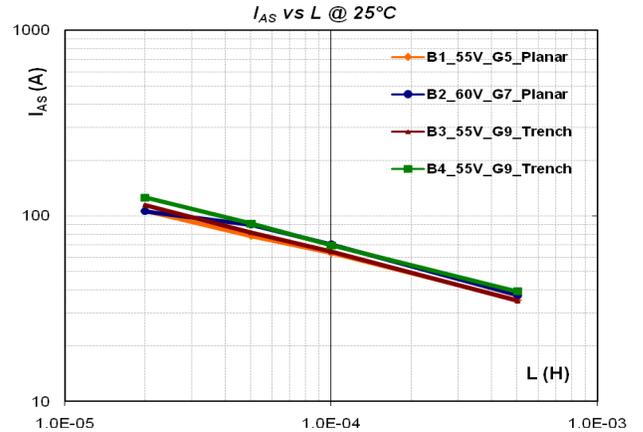


Fig. 3a I_{AS} vs inductance for devices B1-B4 under $T_A=25^{\circ}$ C

The balance of charge in these two regions, when done correctly can provide a breakdown voltage to the device that is higher than that of the plane-junction breakdown of the epitaxy resistivity chosen. Additionally the optimization of these two regions can force the breakdown of the MOSFET to occur in the region directly under the source contact, thereby preventing the hole current from providing a bias

voltage to the source and improving UIS performance as a result.

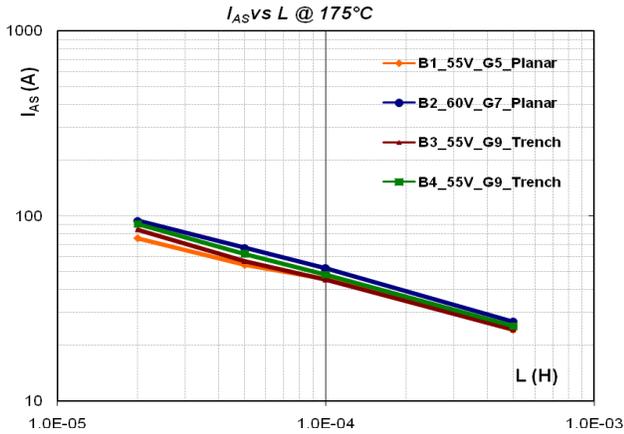


Fig. 3b I_{AS} vs inductance for devices B1-B4 under $T_A=175^\circ\text{C}$

Even though the avalanche performance of the planar FETs is better than that of all generations of trench FETs, Fig. 2a and Fig. 2b clearly show the superior avalanche performance of the Gen 10 devices compared to earlier generation 8 and 9 trench MOSFETs. Comparing Fig. 2a, 2b and Fig. 3a, 3b it is also evident that at lower breakdown voltages (55V-60V) and smaller die sizes the avalanche performance of the trench FETs is comparable to that of the planar FETs. This is most likely because at the lower breakdown voltage the destruction seems to be more energy dependent as opposed to the current density dependent as highlighted in the literature [4].

C. Choosing MOSFETs for in-circuit applications

Datasheet parameters are merely a first-pass selection criteria and should not be used by designers prima-facie. MOSFETs are subject to many stresses depending on the application and the designer needs to be aware of the parasitic inductances as well as thermal limitations of the circuit board and environment as these can lead to unexpected MOSFET failures. For example leakage inductances in a switching circuit such as a ZVT boost topology can cause FET's to avalanche on successive pulses, and although one pulse might not raise the temperature of the MOSFET to cause it to fail, successive pulses cause thermal buildup that leads to MOSFET destruction.

Additionally package inductance, heatsinking and ambient temperature are all factors that need to be closely monitored as inductances can lead to voltage spikes that can exceed the breakdown voltage and combined with higher die temperatures due to inadequate heatsinking can make it easier for MOSFETs to fail from avalanche destruction. Higher temperatures increase the gain of the parasitic bipolar in MOSFETs, which can cause latchup failures and eventual thermal runaway leading to destruction. Using tight board layout and low inductance packages (such as DirectFET™ for switching applications, designers can

minimize overall loop inductances that can cause large voltage spikes. Additionally packages such as the DirectFET™ offer better dual-sided heatsinking options and a more uniform thermal distribution across the die-surface that helps with improved avalanche performance.

III. STUDY OF FBSOA BEHAVIOR

The forward-bias safe operating area (FBSOA) of a MOSFET defines the region of safe and stable operation of the device. In comparison with planar FETs, the trench FETs have demonstrated severe thermal instability, especially at high voltage low current regions of operation. Thermal instability occurs when the rate of change of the generated power exceeds the rate of change of the dissipated power. In this paper, the Spirito approach [5] is used in order to address the thermal instability problem, which is more severe on trench FETs. The conventional thermal boundary is over-estimated, because it is calculated based on the assumption of uniform thermal distribution across the entire die area, which is not always true for the trench FETs. Fig. 4a plots the thermal instability boundary for A1-A5 devices in the same graph. Compared with the 100 μs curve in Fig. 4b, the 10 ms SOA curve in Fig. 4a drops more dramatically from the conventional boundary at larger voltages, indicating more thermal instability problems in longer period of operation. Both figures suggest that the earlier generation parts have wider SOA boundaries than the later ones.

As explained in [6], the narrow FBSOA of trench parts is not necessarily due to cell structure of trench gates. The lower the on-resistance of a MOSFET, the higher the zero temperature crossover point (point of intersection of two transfer curves at different temperatures) will be, and the less robust a MOSFET will be for linear mode applications. This applies to both trench and planar parts.

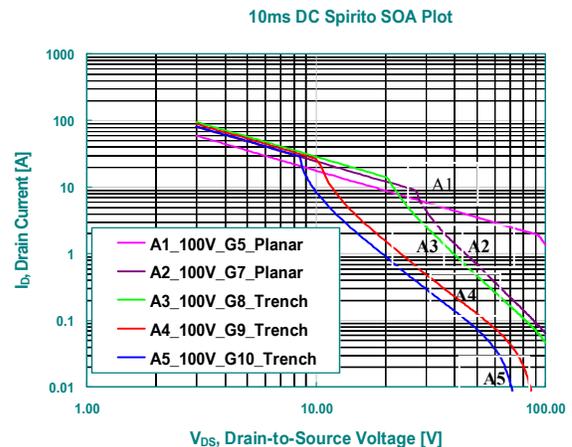


Fig. 4a Spirito SOA thermal boundaries for devices A1-A5 under 10ms

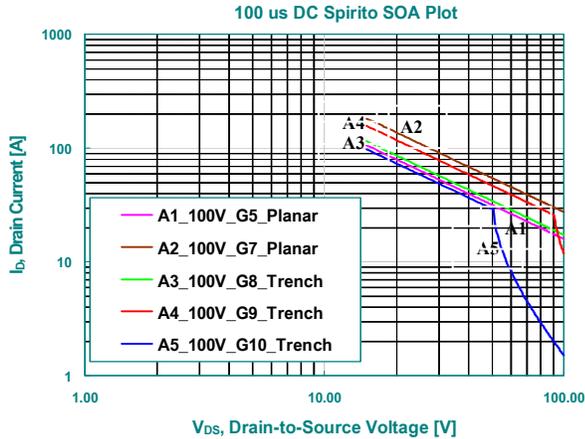


Fig. 4b Spirito SOA thermal boundaries for devices A1-A5 under 100 μ s

The low current high voltage instability region reduces the capability of the device to operate within a wider range of the SOA curve. Care should be exercised in selecting MOSFETs to guarantee robust operation in strictly linear mode applications, such as hot swap controllers, inrush current limiting circuits during turn-on of power converters, or linear controllers for fan motors. In switching applications, including clamped inductive, trench MOSFETs are most suitable because of their low R_{dson} and certain level of linear robustness. The SOA curves of the 55V-60V parts (B1-B4) were similar to that of the 100V parts in Fig 4a and Fig 4b, with vanishing Spirito Effect for shorter times (100 μ s), showing consistency in SOA behavior of trench and planar parts, with planar parts having larger SOA area compared with the trench parts.

IV. BODY-DIODE REVERSE-RECOVERY PERFORMANCE

FET body diode reverse recovery behavior is traditionally evaluated by the double-pulse test method [7, 8, 9]. Because this test methodology is intended to extract T_{rr} , Q_{rr} and I_{RRM} parameters, the applied di/dt is relatively slow (100 A/ μ s). The slow di/dt is partly an historical legacy, but also because as di/dt is increased, resolving the parameters of interest becomes more difficult due to parasitic inductance ($L di/dt$) masking the measurement of the parameters of interest. Since today's power electronics are aimed at highest efficiency, many designs push switching transition times lower, and it is not uncommon to see FETs operating with current slew-rates exceeding several thousand amps per microsecond. While this is possible for rugged trench FETs, as will be shown, older generation planar devices cannot survive these slew rates.

A. Circuit Layout

A simplified schematic of the double-pulse tester used is shown in Figure 5. The circuit board layout was designed to add minimal parasitic inductive elements into the high-current loop. The board design achieved a measured total

loop inductance of 37 nH. This includes the parasitic lead and wirebond inductances of both D²-Pak FETs, the 10 m Ω coaxial current-measuring shunt, the PCB layout, and the DC bus itself (the complete current-loop excluding the external inductor). This value is verified experimentally by turning-on both FETs and watching the current slew-rate. With a 100V bus voltage, we measured a linear current ramp of 150 amps in 55 ns across the coaxial shunt, or 2.73A/ns, thus calculating from $V=Ldi/dt$ that $L = 37$ nH. This value is also consistent with an LT Spice model of the tester developed using both measured and estimated parameters which shows a current slew-rate matching our measurement when the total loop inductance is 37 nH.

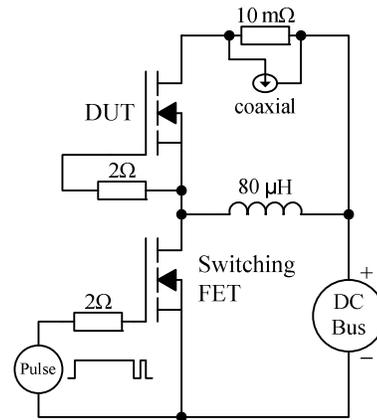


Fig.5 Double-pulse tester schematic

B. Gate Drive

Fast, low impedance gate drive is critical to obtaining double-pulse measurements that are not distorted by the switching FET operating slowly, spending significant time in transition [8]. The gate driver used is a discrete design based on reference [10] with 10-90% rise and fall times < 15 ns driving the largest gate capacitance used in this study. Both the turn-on and turn-off R_G were set to 2 Ω (not including any internal FET R_G). Switching speed in the double-pulse test benefits from somewhat lower effective C_{ISS} and no Miller-effect during the turn-on edge of the switching FET (the beginning of the reverse-recovery period). This is because the Device Under Test (DUT – the upper FET in our implementation) is still conducting during switch turn-on, thus there is little change in V_{DS} of the switched FET, and therefore virtually no Miller capacitance plateau to slow the gate voltage risetime (the drain voltage doesn't fall until long after the gate is fully enhanced – when the DUT body-diode finally recovers). Moreover, since V_{DS} is at nearly 80% of $BV_{(DSS)}$ during the entire turn-on process, the nonlinear junction capacitance is at its lowest value, thereby making C_{ISS} lower than if the drain were not effectively clamped to the bus.

C. Experimental Procedure

The double-pulse tests were run at 25°C. The DUT and the lower (switched) FET were the same device type, as would be commonly employed in a real half-bridge application circuit. The bus voltage was set to 80% of datasheet-rated $V_{BR(DSS)}$ for each device. The gate drive voltage was set to 15V, and the length of the first pulse was adjusted to achieve the desired test current I_F by the time the reverse-recovery pulse was applied. Maximum diode current was limited to $\leq I_{SM}$. When the switching FET was turned-on for pulse 2, the resulting reverse recovery current and voltage of the DUT were captured on the oscilloscope. The duration of pulse 2 was limited to 500 ns to minimize damage to the test circuit in the event of failure (the switching FET could still be turned-off safely even after the DUT had failed). Also, in our experience, if a DUT was going to fail, it would do so within <100 ns of the peak IRR, in agreement with the findings of Blackburn [11].

D. Results

The example in Figure 6a shows a typical reverse-recovery waveform example from device A1. At the beginning of the trace, the current has been flowing in the DUT body-diode (magenta trace) for 10 μ s and the V_{DS} of the DUT (Green trace) is at ~ 0 V. The switching FET is turned-on at 100 ns and the 5A forward current immediately slews negative, while the V_{DS} shows the L di/dt voltage across the FET package. The slow risetime of V_{DS} on the leading edge is due to the combined C_{OSS} of the DUT plus the switch. Once the body-diode recovers, the V_{DS} immediately slews up to avalanche at ~ 110 V, and the current reverses direction and heads back to 0, dissipating the energy stored in the parasitic inductance.

The old generation planar device shown in Figure 6a exhibits a huge reverse-recovery characteristic, despite a very small forward current. This is common of planar MOSFETs from this era. This device failed when I_{RRM} reached 67A, at an applied forward current of only 17A, as seen in Figure 6b.



Fig. 6a Typical reverse-recovery waveform from device A1

The failure in Figure 6b has the signature of a classic second-breakdown of the parasitic NPN bipolar. This occurs during normal sustaining avalanche, when the current density exceeds a (temperature dependent) threshold. The mechanism is that as the current (I_{RRM}) is increased, the bipolar device shifts from normal avalanche multiplication to avalanche injection and thus second-breakdown, characterized by the snapback of V_{DS} from $V_{BR(DSS)}$ to $\sim 1/2$ that value [11] as can be clearly observed in the V_{DS} waveform in figure 6b.

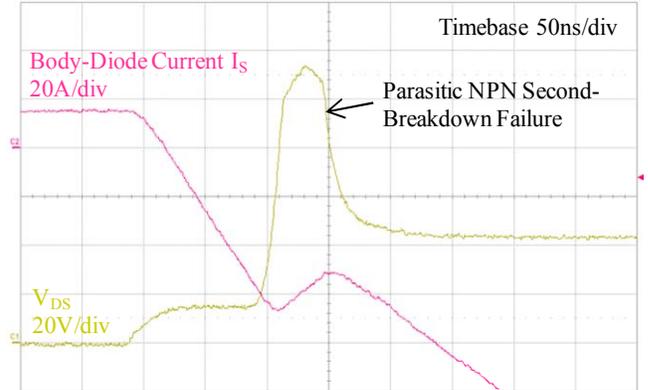


Fig. 6b Reverse-recovery avalanche failure of device A1

Each device-type in table I was tested in this method – incrementally increasing the test current until either the device failed, or I_{SM} (maximum rated source current) was reached. This data is summarized in Figure 7.

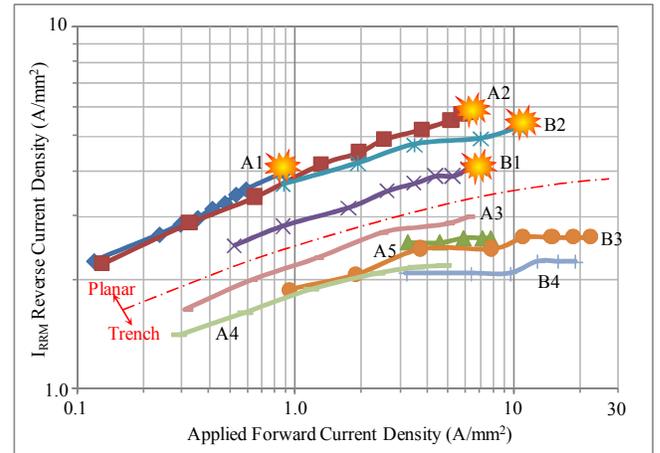


Fig. 7: Peak I_{RRM} versus I_S (normalized by area) for the devices tested

The x-axis of figure 7 shows the applied forward current through the DUT body-diode, just prior to the second pulse. The data are expressed as a current density by dividing by the respective die area, resulting in amps/mm^2 . The y-axis shows the magnitude of the resulting reverse-recovery current (similarly expressed as a current density). The orange “explosion” icons identify any data points where device failure occurred.

A red dividing-line is placed on the graph to highlight the clear separation of the data into two groups – the planar devices are all above this line, and the trench devices are all below the line. So, clearly planar FETs have higher reverse-recovery current per unit area for a given forward current-density, compared to trench FETs. Because of this, it was possible to drive all of the planar devices to a reverse-recovery current-density sufficient to cause device failure, while staying within the devices' maximum current-rating. Also, notice that the two different-sized Gen 5 devices (A1 and B1) failed at the same reverse-current density (3.98 and 4.03 A/mm² respectively). Similarly, the two different-sized Gen 7 devices (A2 and B2) failed at similar current densities (5.54 and 5.26 A/mm² respectively).

In contrast to the planar devices, none of the trench devices could be driven hard enough to cause any failures due to peak reverse-recovery current density. Even though section II shows that trench devices have lower UIS avalanche capability than their planar counterparts – suggesting that they may also have a similarly lower threshold current density for parasitic NPN second-breakdown failure, the body-diode performance was so good that the peak reverse current density we could achieve was about 2.5 A/mm². This was not sufficient to cause any failures for any of the trench FETs tested.

V. CONCLUSIONS

As MOSFET technologies evolve at break-neck speeds with the need for matching parameters to specialized applications, MOSFET ruggedness needs to be evaluated similarly from an application-circuit perspective. In our study using few different generations of planar and trench gate technologies, we have demonstrated and reiterated that Planar FETs have superior FBSOA and UIS avalanche capabilities. However, we have also shown that reverse recovery performance of the body diode of IR's trench-gate MOSFETs as characterized by the reverse-current densities show superior performance than those of planar devices. Our results also indicate that for a given technology there is a reverse current density, which is the "failure" value and exceeding this value results in destruction of the MOSFET. When selecting MOSFETs for use in their application, designers should be aware of the parasitics in their circuit, the thermal environment of operation and the specific strengths and weaknesses of the chosen MOSFET technology from a ruggedness standpoint.

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