Recommended Test Conditions for SEB Evaluation of Planar Power DMOSFETs

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***Abstract*—This paper discusses issues concerning single-event burnout (SEB) and single-event gate rupture (SEGR); explains and provides a basic overview of the preferred test conditions and procedures that would yield the most meaningful test results in evaluating power MOSFETs' SEB susceptibilities, describes how to correctly identify SEB and SEGR failure modes to derive the most feasible failure mechanisms.**

***Index Terms*—Heavy ions, power MOSFET, single-event burnout (SEB), single-event gate rupture (SEGR).**

I. Introduction

TO EVALUATE the risks of using planar power MOSFETs in space applications, it is important to characterize their susceptibilities to heavy ions, namely single-event burnout (SEB) and single-event gate rupture (SEGR). To obtain useful and meaningful test data, it is important to test devices using the proper test conditions and to interpret the different failure modes accurately.

A paper in 2003 [1] presents simulations and test results, showing that devices rated at higher voltages require longer range ions to produce the worst-case conditions for SEGR. The authors suggested that test ions with higher energies at the Texas A&M cyclotron facility are more suitable for evaluating power MOSFETs rated at mid- to high-voltage (basically, those rated higher than 100 V), allowing ample penetration into the thicker epitaxial layers in order to achieve the worst-case condition. Since that paper, there have been numerous questions and concerns about what is worst case for single-event effects (SEE), SEB and SEGR, of various products; whether or not past SEE test data are still valid or useful; how to interpret existing SEE safe operating curves published in manufacturers' datasheets; and how to safely operate devices based upon those datasheets, especially for older generations of radiation-hardened products that were SEE tested using short range ions.

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Many of those who perform SEE studies have elected to use heavier ion species at higher energies and longer penetration depths to evaluate the power MOSFET's SEE performance without fully understanding that deeper ion ranges are useful for evaluating worst case for SEGR, but not necessary for SEB. In addition, longer ranges may complicate the test results or even cause misinterpretation of the SEE failures and inaccurate conclusions.

Also due to limited number of heavy ion test facilities, limited hours available to schedule, and limited funds available for the high cost of heavy ion tests, there is a growing need to define alternative methods of evaluating the power MOSFET's SEE performance. Recently, several papers demonstrated that the use of a laser beam rather than heavy ions may provide adequate SEB characterization [2], [3].

There is also a strong and growing interest in newer generations of commercial devices for potential space applications; because, their electrical performances are usually more desirable than the older generations of devices. Test engineers are faced with significant challenges in determining how to test, characterize and understand the SEE test results of these newer devices. This is especially true since these devices may consist of very different technologies in terms of device design and process. For example, SEE tests have been attempted on advanced commercial trench power MOSFETs 4–5 years ago, but incorrect conclusions were drawn; because, those SEE tests were conducted and test data were interpreted using the same methodology that is used for planar MOSFETs, causing the test results to be improperly analyzed [4].

It is critical to obtain as much meaningful information as possible. Each SEE test trip needs to meet the following criteria: 1) provide sufficient test data to aid in the understanding of the device's failure mode and failure mechanism; 2) accurately assess a device's SEE performance; 3) understand the failure modes and failure mechanisms providing better insights in developing mitigation methods either in device optimization or application; and 4) minimize SEE testing costs.

This paper summarizes the SEE failure modes observed in planar power MOSFETs, and provides preferred test conditions to meet those criteria.

II. Failure Mechanisms of SEB and SEGR

A. Single-Event Burnout (SEB)

SEB in power MOSFETs was first published in 1986 [5]. In this work, the observed failures were catastrophic with both drain-to-source and drain-to-gate shorts. Visual examination of the die after failure revealed noticeable damage to the die surface (discoloration and/or burned regions). One device type exhibited a latched current condition during irradiation but did not fail. In this special case, it was speculated that the heavy ion generated sufficient charge to turn on the parasitic bipolar transistor triggering the regenerative process but there was insufficient energy available to thermally damage the device.

In 1987, a technique was published to characterize power MOSFETs with heavy ions and to trigger and count SEB events without actually damaging the device [6]. Basically, this technique uses a resistor to limit the available power preventing thermal run away, when the parasitic bipolar junction transistor turns on (referred to as SEB circumvention technique). By using circumvention technique, researchers are able to examine the SEB generated current pulses under different conditions and count SEB events, providing statistical data for SEB cross-sectional curves.

Before the introduction of SEB-hardened MOSFETs [7], SEB was the dominant failure mode in N-channel power MOSFETs; and, P-channel MOSFETs were found not to be sensitive to SEB. SEB-hardened MOSFETs incorporated design/process modifications such as shorter source diffusions; higher doped p-body regions, selective doping concentrations, inclusion of a buffer layer (a second epitaxial layer), and other modifications. Those SEB-hardened MOSFETs suppressed SEB, allowing safe operation at higher off-state drain voltages (V_{DS}). By suppressing the SEB failure mode and by allowing operation at higher drain voltages, SEGR soon became the dominant failure mode for those devices.

SEB is commonly referred to as the failure mode at which the device enters thermal runaway under a heavy ion strike with V_{DS} set below the rated drain breakdown voltage (BV_{DSS}). If the device is reverse biased with a V_{DS} that exceeds the secondary breakdown voltage, the charge generated by a heavy ion strike causes a transient current, which, in turn, causes the device to transcend into the negative resistance regime of the avalanche curve which then leads to thermal runaway, destroying the device. Quasi-stationary avalanche simulations [8] show clearly that SEB failure of radiation-hardened power MOSFETs is due to the turn on of the parasitic bipolar transistor inherent in the power MOSFET structure. The ultimate goal of performing SEB tests is to check the device's avalanche capability under a high V_{DS} and high transient current. If the device is designed properly and the secondary breakdown voltage is higher than the device's rated BV_{DSS}, the device should survive the heavy ion test and be deemed SEB immune. However, if the device is not optimized and/or designed properly, the device may fail the heavy ion test for SEB at a V_{DS} significantly lower than the device's rated BV_{DSS}. This is especially true for many of the commercially available power MOSFETs and older generations of radiation-hardened power MOSFETs.

A device's SEB threshold voltage is defined by performing a test iteration starting with a low V_{DS} bias and systematically increasing V_{DS} until SEB occurs, destroying the device. Since SEB destroys the device, statistic SEB data requires many test samples. For SEB failures, no significant effects have been observed, when different off-state gate-to-source voltages are used in tandem with the off-state V_{DS} during heavy ion irradiation [9], [13]. However, the device's ambient temperature has been demonstrated to affect the SEB threshold voltage [9], [10]. Further studies are needed in this regime. The SEB threshold voltage can also vary widely depending upon the generation of the device's technology. For commercial power MOSFETs, the SEB threshold voltage has been measured as low as 20% of their rated BV_{DSS}, depending upon their design and process generation. For radiation-hardened power MOSFETs, the SEB threshold voltages have been measured as low as 50% of their rated BV_{DSS} for older generation and exhibit no SEB to 100% of their rated BV_{DSS} for newer generations.

B. Single-Event Gate Rupture (SEGR)

SEGR in power MOSFETs was first published in 1987 [11], showing that MOSFETs biased in an off-state and irradiated with gold ions exhibited SEGR. After SEGR failure, there were no visible signs of damage on the die surface, even when examined under a microscope (160×); both n- and p-channel devices exhibited similar failure behavior; and post-electrical tests revealed that the devices exhibited excessive gate current leakage.

The SEGR failure mode is believed to be triggered by a heavy ion strike causing a localized transient electric field across a portion of the gate oxide, and if this electric field is sufficiently high, the gate oxide breaks down forming a localized rupture site, which, in turn, leads to the higher gate leakage current. The electric field across the gate oxide comes from two distinct sources:

1) applied gate voltage (directly places an electric field across the gate oxide); and
2) applied V_{DS} (the normal drain electric field across the gate is minimal except during an ion strike, where a portion of the drain electric field is coupled across the gate oxide localized around the strike region).

Drain bias can have significant impact upon the SEGR threshold voltage, depending upon the generation of the device and its technology. Older generations of power MOSFETs usually have large cell pitches and larger JFET widths; those types of devices typically fail at lower V_{DS} even with zero volts on the gate. If the reverse gate bias, V_{GS}, were increased, then the value of V_{DS} at which SEGR occurs would be even lower. For newer generations of radiation-hardened power MOSFETs, devices are designed more ruggedly and most do not fail until a substantial gate bias is applied.

C. SEB-Hardened Devices

It is possible via design and process optimization to fabricate a power MOSFET that is essentially SEB immune, which means the MOSFET is capable of supporting its full rated breakdown voltage under heavy ion irradiation. Even if a device is designed to be SEB immune, SEGR is still possible if the required conditions are met (i.e., higher gate biases, irradiation using heavier ion species, or selection of worst-case ion ranges).

D. SEGR Destructive or Non-Destructive

On the other hand, SEGR failure is also considered destructive, but that issue is currently being debated—SEGR may or may not be catastrophic. SEGR failure causes a localized resistive short thru the gate oxide, which increases the gate-to-drain leakage current at the failure site, while the remaining cells still function normally. An SEGR failed device may actually be capable of passing its electrical parametric specifications with the exception of gate leakage current. Gate leakage currents are typically limited to 100 nA at its rated gate voltage (typically ±20 V), whereas gate leakage currents of a SEGR failed device may be orders of magnitude higher ($> 10\ \mu$A). If the application can continue to operate under this increased level of gate leakage current, then SEGR failure may not be considered catastrophic (long term effects are still unknown). However, if additional good cells experience SEGR failure from heavy ion strikes, the gate leakage current can continue to increase and eventually alter the device's switching performance.

III. SEB Threshold Voltage Factors

A. Impact of Ion Species Upon SEB and SEGR

Selection of ion species is one area of confusion when performing SEB tests. Since Titus *et al.* presented their findings at the IEEE 2003 NSREC, there has been a strong trend to perform most SEE tests at Texas A&M to achieve worst-case scenarios. Many researchers believe that heavier ions with deeper penetration depths (ranges) should be used. Heavier ions with deeper ranges are needed for worst-case SEGR characterization, but are not necessary for SEB characterization. In addition, irradiating SEB prone devices to heavier ions with deeper ranges may complicate the test result. SEGR failures may even be mistaken as SEB failures, if the test data are not carefully evaluated and separated.

Extensive SEE evaluations have been performed on International Rectifier's (IR) proto-type R6 600VN product during the device's development. Lighter ions were found to only trigger SEB, while heavier ions were found to trigger both SEB and SEGR, depending upon the gate bias used during test. Fig. 1 shows some of those SEE test results using Krypton ions at various gate biases from zero volts to -20 V (drain bias is stepped until failure occurs). Clearly, the use of a lighter ion (Krypton) prevents SEGR from occurring even at higher gate biases, while SEB failures are readily observed. SEB is the dominant failure mode with a tight failure threshold voltage range ($570\ \text{V} < V_{DS} < 590\ \text{V}$). Fig. 2 shows some of the SEE test results using Xenon ions at various gate biases from zero volts to -15 V. For V_{GS} from zero volts to -10 V, three beam conditions were used, SEB failures are readily observed with similar failure threshold voltages as those obtained using krypton ions (again, drain bias is stepped until failure); but, at V_{GS} of -15 V, SEGR failures are readily observed at all seven beam conditions (SEGR becomes the dominant failure mode). One can conclude that lighter ions (e.g., Krypton) are more likely to trigger SEB while heavier ions (e.g., Xenon) are more likely to trigger both SEB and SEGR. This does not mean Krypton is not capable of triggering SEGR, other test data shows SEGR failures were observed on low voltage devices using Krypton beam with 50 um range.

Newer generations of radiation-hardened power MOSFETs are designed to be less susceptible to both SEB and SEGR. On those devices, SEGR is not readily observed until V_{GS} is biased at higher voltages. However, many commercial power

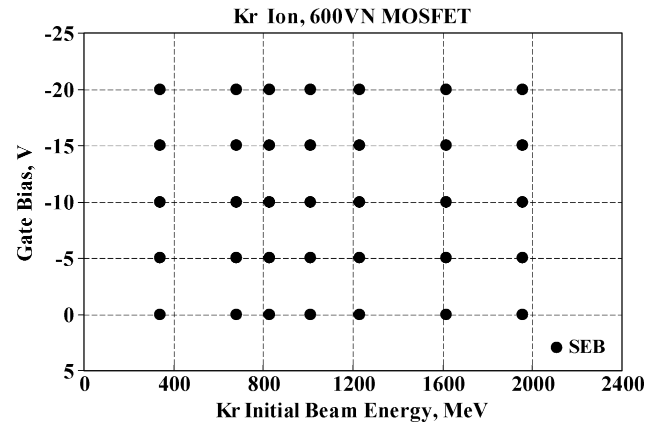

Fig. 1. Lighter ion (Krypton) only triggers SEB failures for a 600VN device regardless of ion energy, LET, ion range, or gate bias (drain voltage is incremented until failure).

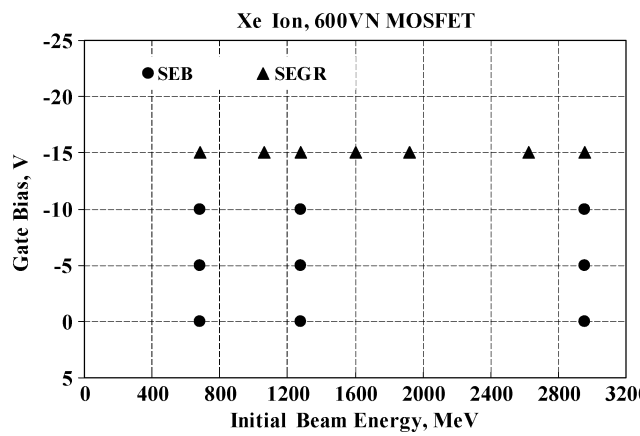

Fig. 2. Heavier ion (Xenon) triggers SEB failures for a 600VN device at lower gate biases, but triggers SEGR failures at higher gate biases (drain voltage is incremented until failure).

MOSFETs and some older generations of radiation-hardened MOSFETs exhibit SEGR even with lighter ions (e.g., Krypton), lower V_{GS} (even at zero volts), and lower V_{DS} (much lower than rated BV_{DSS}). Many of those devices were tested at Brookhaven National Laboratory (BNL), and both SEB and SEGR failures were recorded. Thus, when performing SEB characterization on commercial and older generations of radiation-hardened power MOSFETs, proper selection of ion beam conditions and biases are critical to avoid SEGR and to prevent complicating the SEE test results. In this case, lighter ions, zero volt gate bias are recommended to study a power MOSFET's SEB susceptibility. Most ions at either BNL or Texas A&M are capable of generating transient currents sufficient to trigger SEB. SEB characterization using a laser is being studied as an alternative to heavy ions [2], [3]. Laser irradiation triggers SEB with energies as low as 2 to 3 nJ.

B. Impact of Ion Range Upon SEB

Selection of a proper ion beam for SEB evaluation is an area of confusion. There is a strong trend to perform SEE tests upon power MOSFETs at Texas A&M to produce worst-case scenarios (it is assumed that heavier ions with deeper ion ranges produces worst-case conditions). However, deeper ranges may

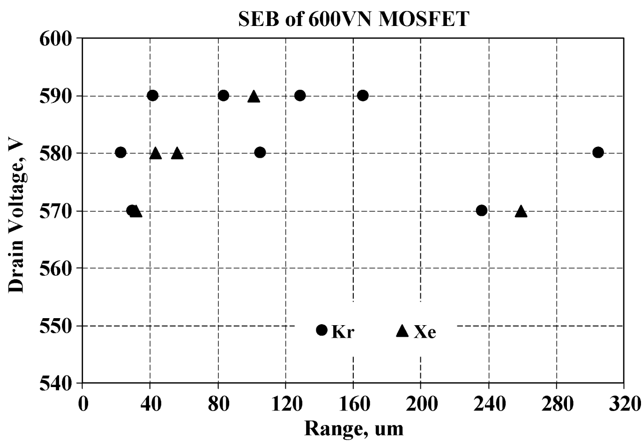

Fig. 3. Test data showing that SEB failure threshold is not impacted by selection of ion species, range, or its energy (range and energy are directly related to each other) for a 600VN device.

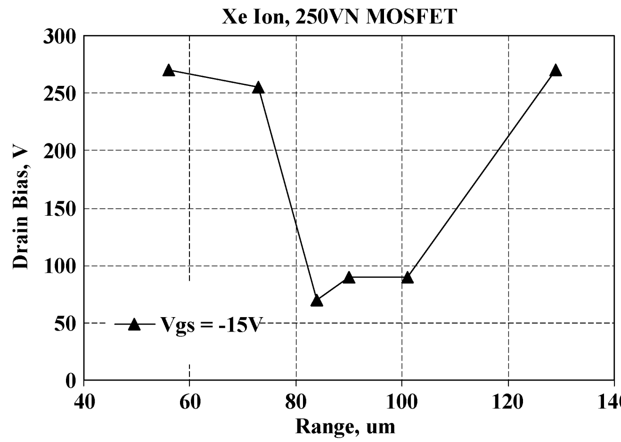

Fig. 4. SEE test results on IR's R6 250VN device with Xe beam and V_{GS} of -15 V showing that there are worst-case ion conditions for SEGR.

not be required for SEB evaluations. In fact, heavier ions with longer ranges may complicate the SEB test results and lead to misinterpretations of the test data.

First, let us re-examine the SEE test results presented in Fig. 1 and Fig. 2, which shows SEB failures as a function of initial ion energy. These data show that SEB is independent of the ion's energy and that the SEB failure threshold is not affected by the ion's penetration depth (ion energy directly relates to the ion penetration depth). Fig. 3 shows some of the SEE test results of IR's R6 600VN proto-type when exposed to Krypton and Xenon at different penetration depths (ion range). The SEB failure threshold voltage stays at $\sim$580 V even when the ion range changes from $\sim$ 23 μm to $\sim$ 305 μm. Clearly, ion range has little impact upon the SEB failure threshold voltage when either Kr or Xe was used. These voltages represent the actual voltages at which the device failed; the drain voltage was increased in 10 V steps. The measured variations ($\pm$10 V) in the SEB failure threshold voltage are most likely related to process variations across a wafer and variations from wafer-to-wafer.

However, the initiating step for SEB is the turn on of parasitic bipolar transistor. To turn on the parasitic bipolar transistor, a high current flow is needed in the base region (sufficient voltage drop along the current flow path in the base region forward biases the emitter-base junction). To evaluate a device for SEB, charge deposition/current flow is needed in the base region. This means that the ion beam needs to reach the first several microns of silicon where the base-emitter junction of the parasitic bipolar transistor is formed [6].

A. Luu *et al.* show some interesting test results [3]. When the heavy ion enters from the top of the die, SEB is observed at drain biases between 90 V and 100 V. When the heavy ion enters from the bottom of the die and almost penetrates the entire die thickness, SEB is detected at drain biases between 90 V and 100 V. However, when the ion enters from the bottom of the die and is stopped at $\sim$ 100 μm from the die surface, SEB is not observed or when stopped at $\sim$ 50 μm, SEB is observed at much higher drain biases. As long as the ion beam has sufficient depth to penetrate the die surface and reach the sensitive parasitic bipolar transistor junction (which is usually 1 to 2 μm below the active silicon surface) with sufficient energy deposition, SEB should be triggered, if present. There is no need to use ions with much deeper ranges for SEB evaluation. The actual amount of energy deposition (LET value) needed to induce SEB is still under investigation. Based on historical data, ions such as Krypton, Bromine, Iodine, Xenon, with $\sim$30 um ion range are all adequate to be used for SEB evaluation.

C. Impact of Ion Range Upon SEGR

It has been demonstrated that worst-case ion conditions exists for SEGR failures [1], [12], [13]. Worst-case responses are achieved for higher Z ion species with a penetration depth (range) that maximizes the energy deposition in the epitaxial layers producing the lowest SEGR failure threshold voltages. This has also been shown on the newer generation of radiation-hardened power MOSFETs (such as IR's R6 products). A worst-case condition for SEGR occurs when the Bragg peak for the ion is positioned at or near the interface between the epitaxial buffer layer and high-resistivity substrate [13]. Fig. 4 shows SEGR data on IR's R6 250 V N-channel MOSFET where a worst-case condition for SEGR occurs with a penetration depth between 84 and 101 μm at Vgs of -15 V. When the ion range is shorter than 73 μm or deeper than 129 μm, the device survives at full-rated drain bias and V_{GS} of -15 V. Fig. 5 is similar to Fig. 4 except it shows data on IR's proto-type R6 600VN MOSFETs. Worst-case ion conditions exist but span a wider range. Therefore, to avoid SEGR failures and not complicate SEB evaluations, shorter range ions are recommended for SEB studies.

D. Impact of LET Value Upon SEGR Performance

When evaluating power devices' SEE performance, LET value has always been emphasized and is still used as a critical specification for qualification of products for many space systems. While it is sensible to use LET as a criteria for low-voltage SEE testing (such as integrated circuits), it may not be the best yardstick for power devices and not for SEGR evaluation. SEE test ultimately is a test of device's capability of handling localized charge deposition anywhere in the device when gate and drain are biased at desired conditions. For

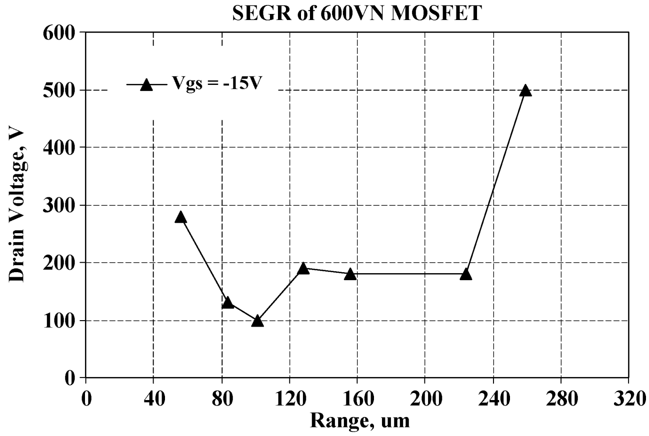

Fig. 5. SEE test results on IR's proto-type R6 600VN device with Xe beam and V_{GS} of -15 V showing that there are worst-case ion conditions for SEGR.

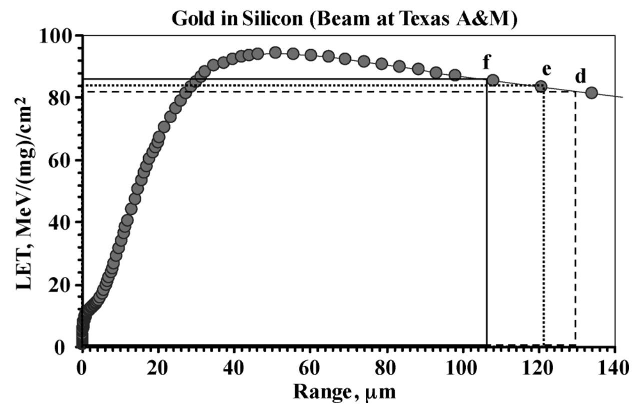

Fig. 7. Texas A&M example of energy deposition in sensitive region with initial LET of 82 $\mathrm{MeV/mg/cm^2}$ for a power MOSFET with total 15 μm epi thickness. LET profile determined using SRIM 2003 [14].

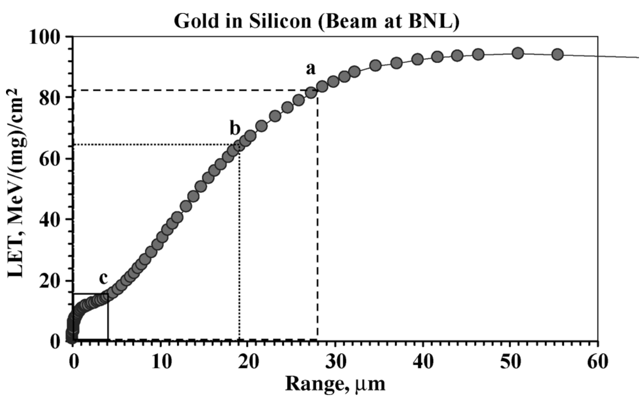

Fig. 6. BNL example of energy deposition in the sensitive region with initial LET of 82 $\mathrm{MeV/mg/cm^2}$ for a power MOSFET with total 15 μm epi thickness. LET profile determined using SRIM 2003 [14].

worst-case analyses, the maximum charge deposition needs to be placed inside the sensitive region.

Fig. 6 is a typical LET versus range curve for Gold ions available at BNL, which is selected to achieve an initial LET of 82 $\mathrm{MeV/mg/cm^2}$. At this facility, the initial ion energy is 320 MeV with a range in silicon of 27.5 μm (point a). On a typical radiation-hardened power MOSFET, the ion has to travel ~ 9 μm top dead layer before it reaches the active silicon layer (see point b) and the LET of the ion decreases from 82 to 65 $\mathrm{MeV/mg/cm^2}$. Assuming the device has a total epitaxial layer thickness (epitaxial layer plus any buffer layer) of 15 μm, then the SEGR sensitive region spans 15 μm across the active silicon to the epitaxial/substrate interface based upon our understanding of worst case SEGR. The LET at this interface is 15 $\mathrm{MeV/mg/cm^2}$ (point c). Then, the ion comes quickly to rest near the epitaxial/substrate interface. The total energy deposition in the active silicon ($\sim$150 MeV) is about $\sim$47% of the initial ion energy (an average LET of 42). This charge deposition is not uniform and the charge deposition near the critical epitaxial/substrate junction is small compared to charge deposited near the active layer surface. This example clearly shows that high initial LET does not translate into large charge deposition thru the sensitive region and the critical junctions.

Fig. 7 is a typical LET versus range curve for Gold ions available at Texas A&M, which is selected to achieve an initial LET of 82 $\mathrm{MeV/mg/cm^2}$ as well. Here, the initial energy is $\sim$ 2450 MeV with a range of $\sim$ 130 μm (point d). We define the same layer thicknesses as used in Fig. 6. After traversing the top layers, the LET increases from $\sim$ 82 to $\sim$ 83 $\mathrm{MeV/mg/cm^2}$ (point e) and the energy decreases to $\sim$2250 MeV. The LET at the bottom of the epitaxial/substrate interface is $\sim$ 86 and ion energy is $\sim$ 1950 MeV (point f). The ion continues to travel deep into the substrate. The total energy deposited in the active silicon ($\sim$ 500 MeV) is about $\sim$ 26% of the initial ion energy but with average LET of $\sim$ 84.5 $\mathrm{MeV/mg/cm^2}$. This charge distribution is uniform and the charge deposition near the epitaxial/substrate interface is comparable to the charge deposited near the active layer surface.

These two examples (Figs. 6 and 7) show that a SEE specification stating only a LET requirement presents problems when testing for SEGR. Clearly, there are two energy conditions that typically meet the LET specification with one yielding a uniform deposition throughout the sensitive region and the other yielding a non-uniform deposition with very little charge deposited near the critical interface. Fig. 8 shows LET versus ion energy for three ions: Gold, Xenon and Krypton. For each ion, there are two possible energies that yield the same LET. One falls on the low-energy side of Bragg Peak; LET is highest at the surface and decreases linearly and rapidly to zero. Those ions are readily available using the Tandem Van de Graff generator at BNL. For years, SEE tests were performed with lower range ion beams, with maximum energies of 400 MeV (depending upon the ion species), ranges up to 40 μm in silicon, and LETs up to 83 MeV/(mg/cm^2). Test results were considered valid as long as the initial LET met the requirement, even if the ion range was under 30 μm. Now, we know that lower energy and range ions may be adequate for SEB characterization, but not for SEGR characterization. The other falls on the high-energy side of the Bragg peak; LET may not be the highest at the surface but slowly increases until reaching the Bragg peak energy then begins to rapidly decrease. Those ions are readily available using a Cyclotron (e.g., at Texas A&M). If the high-energy side ion is properly selected to position the Bragg Peak near

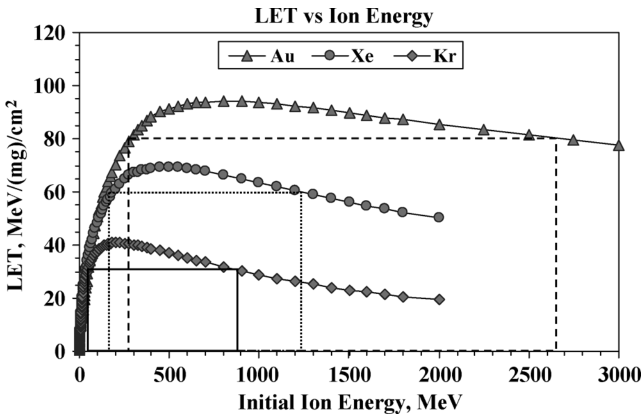

Fig. 8. Examples showing for a given ion, there will be two very different beam conditions for the same LET value. One falls to the left side of Bragg Peak, with low initial ion energy, while the other falls to the right side of Bragg Peak with high initial ion energy.

the epitaxial/substrate interface, then the lowest SEGR failure threshold voltage can be determined (worst-case).

E. Impact of Drain Bias Upon SEB

Drain bias is the most important factor during SEB evaluation, and is also a simple one. If the device catastrophically fails at the rated BV_{DSS} under heavy ion irradiation and shows visual signs of damage (e.g., burn marks) in the die active area, the failure is most likely SEB. For any given device, the SEB failure threshold voltage is determined by its design and process.

Fig. 9 is a typical quasi-stationary avalanche simulation curve; the secondary breakdown voltage is directly related to the SEB threshold voltage [8]. SEB should not occur when the drain bias is less than 578 V, but should occur when the drain bias is at or above 578 V and transient drain current is at or above 10^{-3} A (or 10^{-5} A when considering thermal effects). If the transient current is sufficient, then the SEB failure threshold voltage for the drain bias is determined by the secondary breakdown voltage. Of course, this assumes that all the devices being tested are manufactured identically and have the same secondary breakdown voltage. In reality, the SEB failure thresholds will vary due to normal part-to-part, wafer-to-wafer, lot-to-lot, and manufacturing life variations.

SEB failure threshold voltages can be experimentally obtained by subjecting the device to a suitable ion, by initially setting V_{DS} to a safe operating voltage, and then by increasing V_{DS} systematically until SEB failure occurs. Fig. 10 shows one measured variation of SEB failure threshold voltages obtained from forty-four samples of IR's proto-type 600 V MOSFET. Clearly, SEB failure threshold voltage (i.e., secondary breakdown voltage) for this population varied from 570 V to 600 V (i.e., 585V±15V).

F. Impact of Gate Bias Upon SEGR

Gate bias, V_{GS}, has little, if any, impact upon SEB, but has drastic impact upon SEGR. The danger of using V_{GS} bias during SEB evaluation is that the use of V_{GS} biases may trigger SEGR failures. If SEB is present, SEGR competes as a failure mode especially at higher V_{GS}, complicating the SEB evaluation. Recall, Fig. 2 shows that the failure mode is exclusively

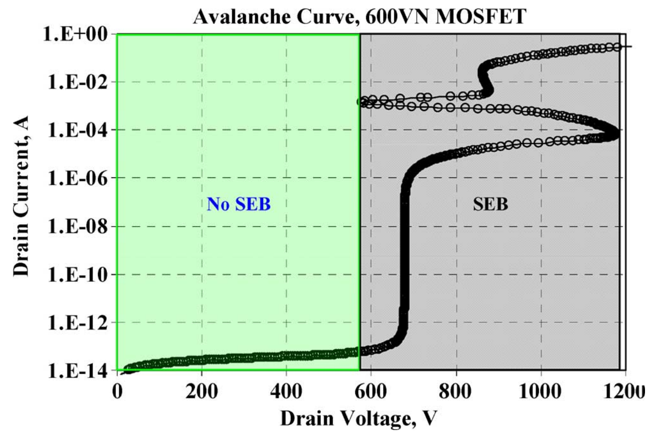

Fig. 9. Typical quasi-stationary avalanche curve of a 600VN device showing SEB immunity when drain bias is less than 578 V but SEB will occur when drain bias is at or above 578 V.

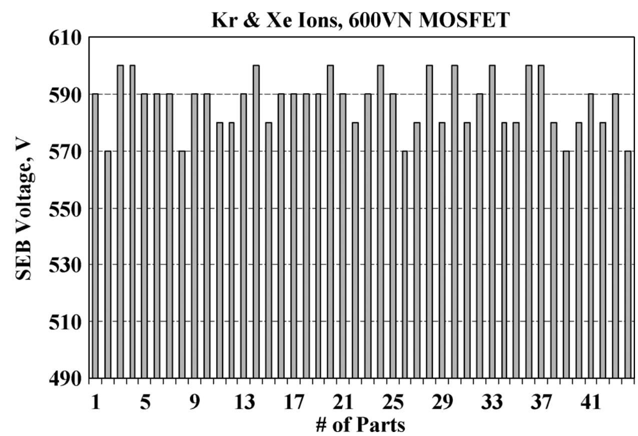

Fig. 10. Variation of SEB threshold voltage for 600 V MOSFETs based upon 44 samples. Ions used were Kr and Xe, the gate biases were set either at 0 V, −5 V, −10 V, −15 V or −20 V.

SEB at V_{GS} of 0 V, −5 V and −10 V. At V_{GS} of −15 V, the failure mode is exclusively SEGR.

Of course, SEGR sensitivity to V_{GS} may vary across product lines. For commercial power MOSFETs or even older generations of radiation-hardened power MOSFETs, SEGR may occur at V_{GS} of zero volts and at V_{DS} well below the device's rated BV_{DSS}. Thus, it is always a good idea to perform a complete evaluation to identify the device's SEE capability in terms of safe operating areas for both SEB and SEGR.

IV. Typical Signatures of Different Failure Modes

It is equally important to choose the proper ion conditions, to choose the proper bias conditions for SEB or SEGR characterization, and to analyze/confirm the SEE failure modes before drawing any conclusion from the SEE test results. If failure modes are not properly identified, then the test efforts may be wasted or the wrong conclusions may be drawn (causing confusion or misleading information).

A. Typical Signatures of SEB Failure

First, by definition, SEB failure is the destructive failure of a device not to be able to support its rated breakdown voltage under heavy ion irradiation. That means the device catastrophically fails at V_{DS} less than or equal to the device's rated breakdown voltage when subjected to heavy ion irradiations. Second, SEB failure is the result of thermal runaway due to the turn-on of the parasitic bipolar transistor. SEB is dependent upon V_{DS} and not V_{GS}. Three steps to verify SEB: 1) review in-situ leakage current logs—I_{DS} should increase substantially and I_{GS} stays unchanged; 2) inspect the failed parts visually—SEB creates burn marks in active area; 3) perform post-SEE electrical testing—drain to source is shorted and gate is intact.

B. Typical Signatures of SEGR Failure

SEGR failure is the failure of the gate oxide not to be able to insulate high current flows from gate to drain under heavy ion irradiation. SEGR is sensitive to changes in both V_{DS} and V_{GS}. As V_{GS} is increased, SEGR becomes a more likely failure mode. Three steps to verify SEGR: 1) review in-situ leakage current logs—I_{GS} increases substantially followed by a similar increase in I_{DS}; 2) inspect the failed parts visually—SEGR leaves no visual signs of damage in the active area; 3) perform post-SEE electrical testing -drain to gate is resistively shorted at higher V_{GS} bias, while BV_{DSS} and V_{TH} values remain the same.

C. Typical SEB & SEGR Curves

Fig. 11 is a summary of SEE curves potentially applicable to a 200VN device. The curve (diamonds) indicates that the device exhibited no SEB when tested to the device's maximum rated drain voltage but failed for SEGR at V_{DS} of 160 V and V_{GS} of -20 V. The curve (circles) indicates that the device failed for SEB at a drain voltage of 180 V and failed for SEGR at V_{GS} -15 V and -20 V. The curve (triangles) indicates that the device failed for SEGR at V_{DS} at 190 V and V_{GS} at zero volts. The SEGR threshold voltage for the drain decreases as the gate becomes more negatively biased. Here, SEGR is the dominant failure mode, because the SEB threshold for the drain voltage is higher than 190 V for this device. The curve (squares) indicates that the device failed for SEB at V_{DS} 170 V irrespective of the gate bias. Here, SEB is the dominant failure mode, because the SEGR threshold has a drain bias greater than 170 V and/or the gate voltage to be more negatively biased than -20 V.

Though curves with round dots, square dots and triangles are not desirable for an intended 200VN device, they each define a SEE safe operation area based on test ions used. Based on current understanding, the SEB threshold voltage does not change with ion species, but SEGR threshold voltage will. The heavier the ion, the lower the SEGR threshold voltage will be. SEGR threshold voltage will also change with ion range. This is where the difficulty/confusions arise when trying to interpret SEE SOA curves in manufacturer's data sheets for the SOA for a specific application.

D. Typical Failure Modes Other Than SEB and SEGR

There can be SEE failures that do not belong to either SEB or SEGR [15]–[21]. Failure could happen due to mishandling such as adjusting bias conditions while ion beam is on or device fails for SEFF—a new SEE failure mode found on trench devices most recently [15]. Sometimes the device can fail due to sudden

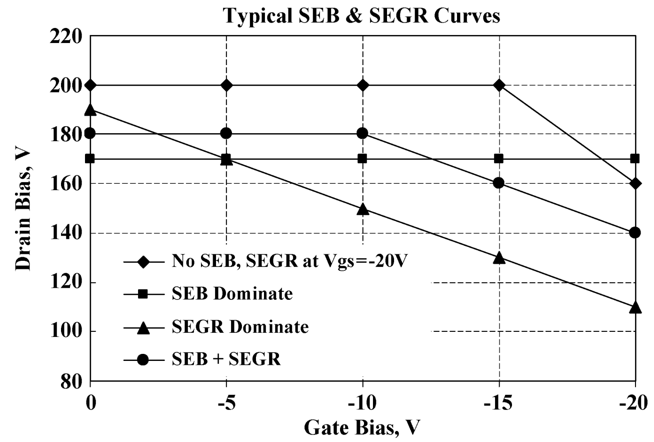

Fig. 11. An example showing typical SEB and SEGR SOA curves for four different failure modes.

increases of both gate current and drain current [16]. Failures of this kind usually end up with massive burn spots near gate runners. Failure mechanisms of this failure mode are still under investigation.

V. Summary

SEB can be triggered under most heavy ion beams available at most facilities. For evaluation of SEB, it is preferred to use lighter, shorter-range ions with the gate bias at zero volts to minimize the test result complications, which may arise from competing failure mechanism (specifically SEGR). This is even more critical when evaluating commercial power MOSFETs' and older generations of radiation-hardened power MOSFETs' SEB susceptibility. Heavier, deeper-range ions will give worst-case SEGR results, and should be avoided while studying SEB failures. It is also suggested to identify the true failure mechanism by closely checking in-situ logged leakage current data, visual inspection on failed parts and compare with pre/post SEE electrical test results. If using backside laser test method, make sure the laser beam does reach die surface. For testing of devices with little SEE background info, it is suggested to evaluate parts with all possible test conditions (ion species, ion range, ion angle and bias conditions) and review test data carefully.

We hope this paper clarifies many test issues in regards to SEB and SEGR type failures and assists those who perform these tests, who need to interpret test results, and provides some general guidance on SEE safe-operating-area.

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