IRPP3637-18A *POWIR+ Chipset* Reference Design

18Amp Single Phase Synchronous Buck *POWIR+™ Chipset* Reference Design using IR3637SPBF PWM & Driver IC and IRLR8713PBF & IRLR7843PBF D-Pak MOSFETs

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Table of Contents

Introduction

The IRPP3637- 18A is an optimized POWIR+™ Chipset reference design, targeted at low cost, medium-to-high power synchronous buck applications up to 18A output current. The IRPP3637-18A uses International Rectifier's IR3637SPBF single channel PWM controller in an 8-pin SOIC and IRLR8713PBF & IRLR7843PBF D-Pak MOSFETs. The IRLR8713PBF is utilized as a high side control FET, and the IRLR7843PBF is utilized as a low side synchronous FET. This reference design has built-in power design expertise regarding component selection and PCB layout, and is representative of a realistic final embedded synchronous buck design, intended to simplify the design in effort without unnecessary design iterations. The design is optimized for 12V input and 3.3V output @ 18A and 400kHz switching frequency, including considerations on layout and passive & magnetic component selection. The IRPP3637-18A delivers the complete 18A design in approximately 2.1in^2 board area at up to 87% full load electrical efficiency and up to 88.8% peak efficiency.

International Rectifier also offers the POWIR+ Chipset on-line design tool **(http://powirplus.irf.com)** allowing the customization of the IRPP3637-18A reference design to meet individual requirements. Based on specific inputs, the POWIR+ Chipset on-line design tool will provide a tailored schematic and bill of materials, from which the engineer can run a full suite of on-line design simulations, and then order the fully assembled and tested customized reference design (see details on page 14).

Design Details

The IRPP3637-18A reference design is optimized for an input voltage range of 12V+/-10% and an output voltage of 3.3V at a maximum of 18A load current, using the IRLR8713PBF and IRLR7843PBF D-Pak MOSFETs.

This chipset is operated at 400kHz switching frequency to allow a good trade off with size and performance at the specified operating conditions. All the essential components that contribute to a low cost compact solution are enclosed by the rectangular box shown on the PCB, showing a total solution size of 1.4" x 1.5" (2.1" sq). The electrical connection diagram is shown in figure 1 and the corresponding circuit schematic is shown in figure 2.

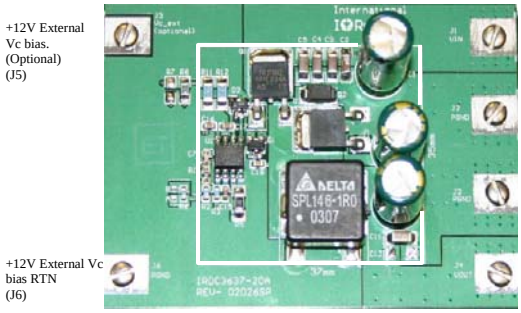

Figure 1: IRPP3637-18A Electrical Connection Diagram

Input/Output Connections

J1: Input power connection terminal
J2: Input power return preferred connection terminal
J3: Output power return preferred connection terminal
J4: Output power connection terminal
J5: External bias power connection terminal. This terminal is unused for standard reference design configuration.
J6: External bias power return preferred connection terminal.

This terminal is unused for standard reference design configuration.

Start-Up Procedure

The 12V input power is connected between terminals J1 and J2 and the 3.3V, 18A output power is obtained through terminals J3 and J4.

The V_{CC} and V_C pins are the low side driver and high side driver power input pins respectively. The V_{CC} pin also includes the housekeeping power of the PWM controller. An under-voltage lockout (UVLO) feature is associated with each of these pins, which is set to 4.2V for V_{CC} and 3.3V for V_C. A charge pump circuit comprised of C18, D1, and C17 applies adequate voltage to the V_C pin to allow fast driving capability, hence reducing the switching losses of the control FET (Q1). A 100Ω resistor (R11 in parallel with R12) is added in series with the charge pump circuit to maintain the V_C voltage below 20V to reduce the temperature of the PWM controller IC.

Upon application of the input power, the output starts ramping up to regulation within 4ms. The ramping time can be adjusted through the soft start capacitor C16. The output voltage of the synchronous buck regulator is set to 3.3V using the internal 0.8V reference voltage.

The following equations are used to calculate the MOSFET power loss. Refer to the IRLR8713PBF and IRLR7843PBF datasheets to select the parametric values of the power loss equations terms.

Control FET Losses:

Eq (1):

$$P_{Q_1} = I_{Q_1}rms^2.R_{DQ1}.R_{Dn} + (I_o.\frac{Q_{sw1}}{I_{g1}}.V_{in} + Q_{gQ1}.V_{dd} + Q_{ossQ1}.V_{in}).F_{SW}$$

Synchronous FET Losses:

Eq (2):

$$P_{Q_2} = I_{Q_2}rms^2.R_{DQ2}.R_{Dn} + \left(\frac{Q_{ossQ2}}{2}.V_{in} + Q_{gQ2}.V_{dd} + Q_{rrQ2}.V_{in}\right).F_{SW}$$

Deadtime losses:

Eq (3):

$$P_{td} = V_{SD}.I_o.t_d.F_{sw}$$

Total FET losses:

Eq (4):

$$P_{FET\_total} = P_{Q1} + P_{Q2} + P_{td}$$

Where,

I_{Q1rms} and I_{Q2rms} are the rms currents for control and sync FETs respectively, in Amps

I_o is the output load current in Amps

R_D is the R_{DSON} in ohms of the FETs and R_{Dn} is the normalized R_{DSON} factor vs temperature extracted from the MOSFET datasheets.

Q_{SW} is the FET switch charge in nC

V_{IN} is the input voltage of the sync buck converter

Q_g is the total gate charge in nC.

V_{dd} is the FET drive voltage, which is 8V.

I_g is the drive current which is 0.25A.

Q_{OSS} is the FET output charge in nC.

Q_{rr} is the sync FET internal body diode reverse recovery charge in nC

V_{SD} is the sync FET internal body diode forward voltage drop in volts. If an external Schottky diode is used, then V_{SD} needs to be the forward voltage drop of the Schottky diode.

F_{SW} is the switching frequency of the sync buck converter in hertz.

td is the dead time caused by the PWM controller IC in seconds. This parameter is specified in IR3637SPBF datasheet.

For design calculations related to programming the output voltage and the soft start time, selection of input/output capacitors and output inductor and control loop compensation, refer to the

guidelines outlined in the IR3637SPBF PWM controller datasheet.

IR's online design tool POWIR^{+} should be used to customize a design for applications outside the standard 12V+/-10% input range and 3.3V output, and for varied design goal objectives.

Layout Considerations

The IRPP3637-18A reference design PCB layout offers compact design with minimum parasitics at 400kHz switching frequency. The board is designed with 4 layers using 1 oz copper weight per layer. Figures 3a through 3d represent the layout of each layer. To minimize the parasitics, the following was observed:

1. The switch node connection path is made as short as possible by placing the output inductor L1 close to the drain of the synchronous FET.
2. The input decoupling 10uF ceramic capacitors C2, C3, C4 & C5, are placed across the drain of the control FET and the ground plane. The 1000uF electrolytic capacitor C1 represents the input bulk capacitance of the synchronous buck regulator.
3. A solid ground plane is furnished in mid-layer 2. The connection of the signal ground to power ground is done at a single point in the bottom layer as shown in figure 3d.
4. The feedback track from the output V_{OUT} to FB pin of the IC is routed as far away from noise generating traces as possible in mid-layer 2 as shown in figure 3c.

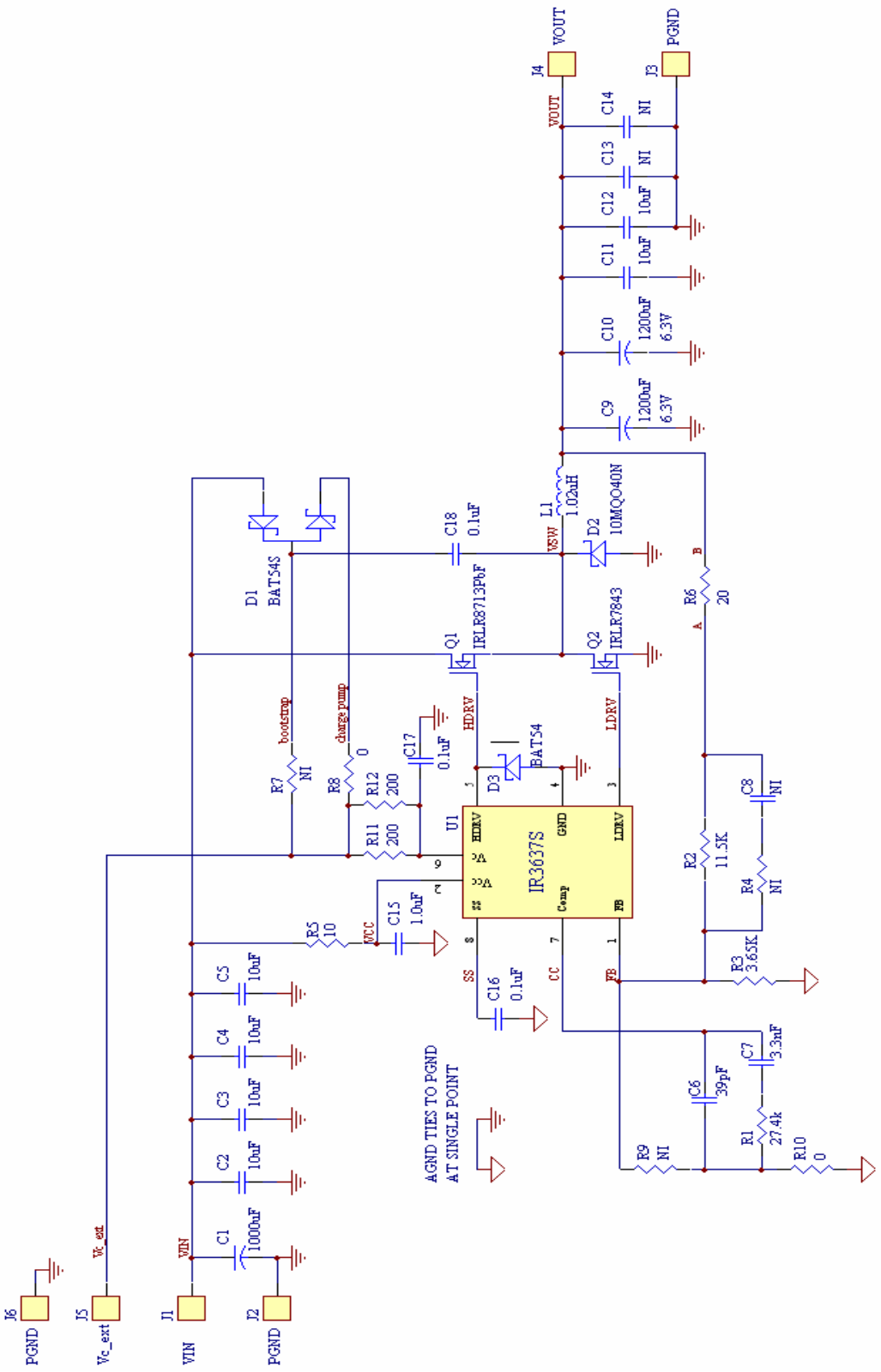

Figure 2: Schematic Diagram for IRPP3637-18A Reference Design

QTY	REF DESIGNATOR	DESCRIPTION	SIZE	MFR	PART NUMBER
1	C6	Capacitor, ceramic, 39pF, 50V,NOP, 5%	0603	KOA	NPO0603HTTD390J
1	C7	Capacitor, ceramic, 3.3nF,X7R,50V,10%	0603	KOA	X7R0603HTTD332K
3	C16, C17, C18	Capacitor, ceramic, 0.1µF, 50V, X7R, 10%	0603	TDK	C1608X7R1H104K
1	C15	Capacitor, ceramic, 1.0µF, 16V, X5R, 10%	0603	TDK	C1608X5R1C105K
4	C2, C3, C4,C5	Capacitor, ceramic, 10uF, 16V, X5R, 20%	1206	TDK	C3216X5R1C106M
2	C11, C12	Capacitor, ceramic, 10uF, 6.3V, X5R, 20%	1206	TDK	C3216X5R0J106M
1	C1	Capacitor, aluminum electrolytic,1000uF,16V	8mm X 20mm	Sanyo	16ME1000WGL
2	C9,C10	Capacitor, aluminum electrolytic,1200uF,6.3V	8mm X 16mm	Sanyo	6ME1200WG
1	D3	Schottky Diode, 30V,200mA	SOT23	IRF	BAT54
1	D1	Schottky Diode, 30V,200mA	SOT23	IRF	BAT54S
1	D2	Schottky Diode, 40V,1.5A	D64	IRF	10MQ040N
3	J1, J4, J5	Red Banana Jacks-Insulated Solder Terminal	4.44mm	Johnson	108-0902-001
3	J2, J3, J6	Black Banana Jacks-Insulated Solder Terminal	4.44mm	Johnson	108-0903-001
4	J1, J4, J5, J6	Pan Head Slotted,screw 1/2"	-	McMaster-Carr	91792A081
2	J2, J3	Pan Head Slotted,screw 1/4"	-	McMaster-Carr	91792A077
6	J1, J2, J3, J4, J5, J6	Machine Screw Hex Nuts	-	McMaster-Carr	91841A003
1	L1	1.02uH,30A,1.8mΩ	13mmX12.7mmX6.5mm	Delta Electronics	SN146-1R0IR
1	R8	Resistor,thick film, 0Ω	0805	ROHM	MCR10EZHJ000
1	R10	Resistor,thick film, 0Ω	0603	ROHM	MCR03EZHJ000
1	R5	Resistor,thick film,10Ω, 5%	1206	DALE	CRCW1206-100JRT1
1	R6	Resistor,thick film,20Ω, 1%	0603	KOA	RK73H1JLTD20R0F
2	R11,R12	Resistor,thick film,200Ω, 1%	1206	KOA	RK73H2BTTD2000F
1	R1	Resistor,thick film,27.4kΩ, 1%	0603	KOA	RK73H1JLTD2742F
1	R3	Resistor,thick film,3.65kΩ, 1%	0603	KOA	RK73H1JLTD3651F
1	R2	Resistor,thick film,11.5kΩ, 1%	0603	KOA	RK73H1JLTD1152F
1	Q1	N-FET,25V,4.8mΩ,17nC	DPAK	IR	IRLR8713PbF
1	Q2	N-FET,30V,3.3mΩ,34nC	DPAK	IR	IRLR7843
1	U1	PWM Controller	SO-8	IR	IR3637SPbF
6	C8, C13, C14, R4, R7,	Not installed			

Table 1 – Complete Bill of Materials for IRPP3637-18A Reference Design

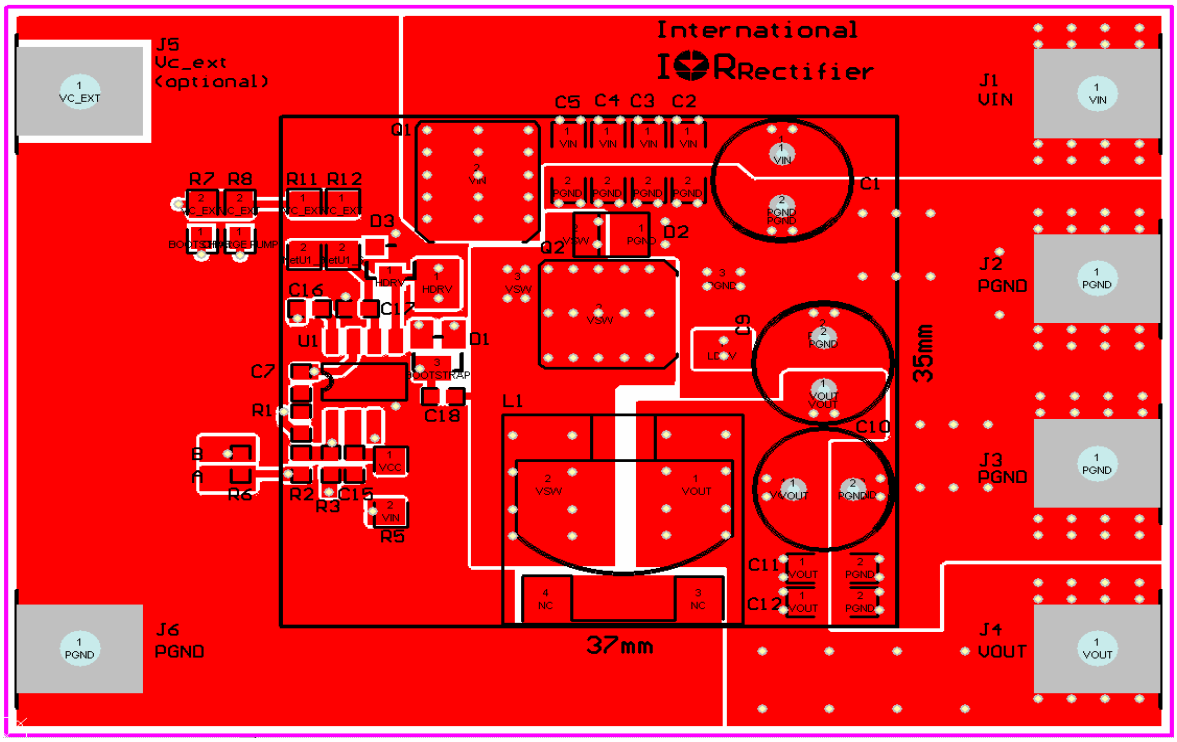

Figure 3a: IRPP3637-18A Reference Design top layer placement and layout.

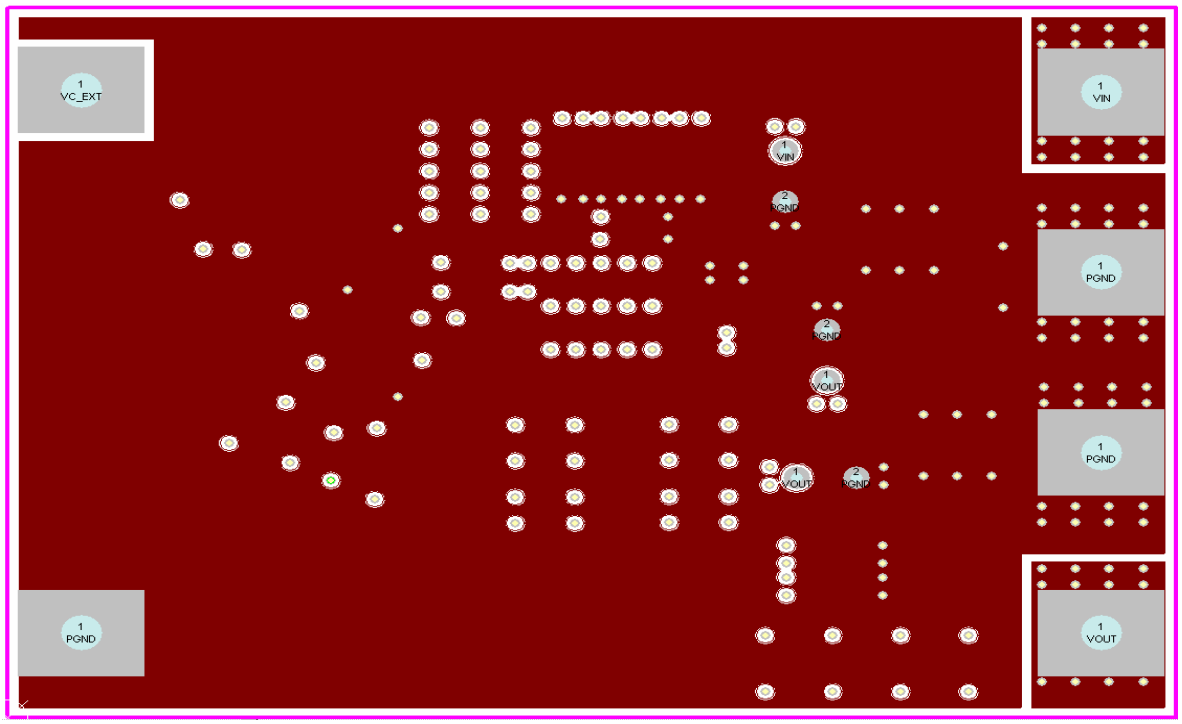

Figure 3b: IRPP3637-18A Reference Design mid-layer1 ground plane

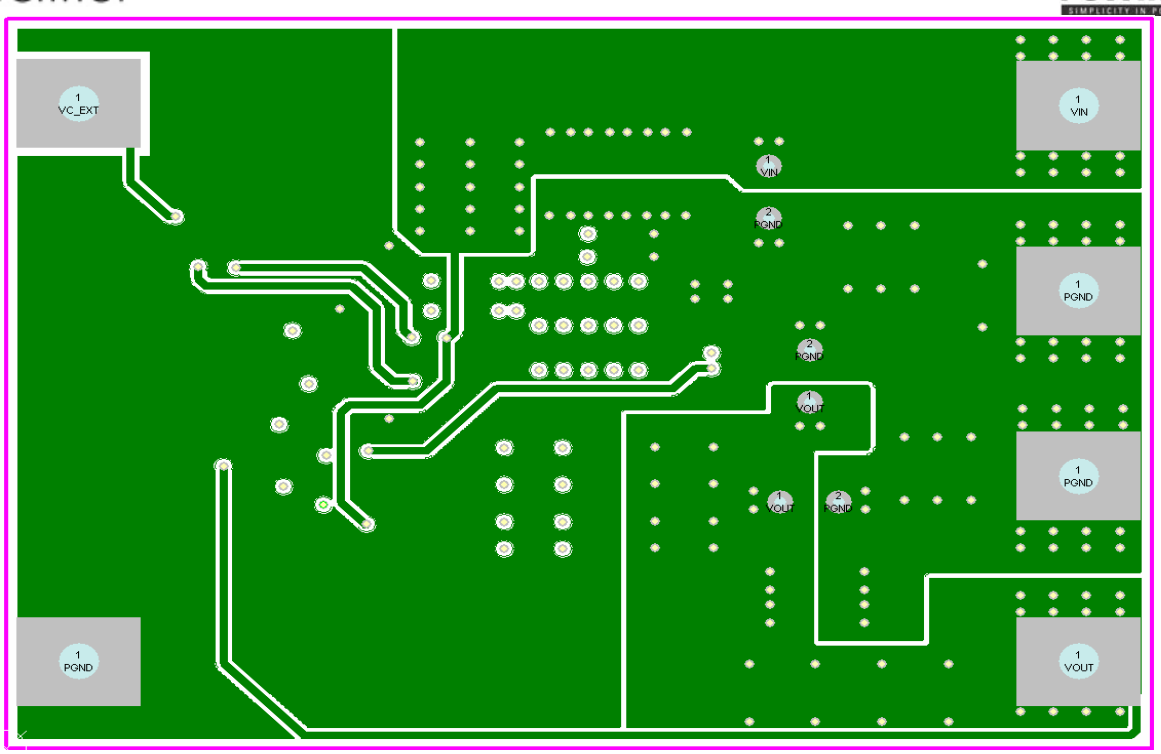

Figure 3c: IRPP3637-18A Reference Design mid-layer2 layout.

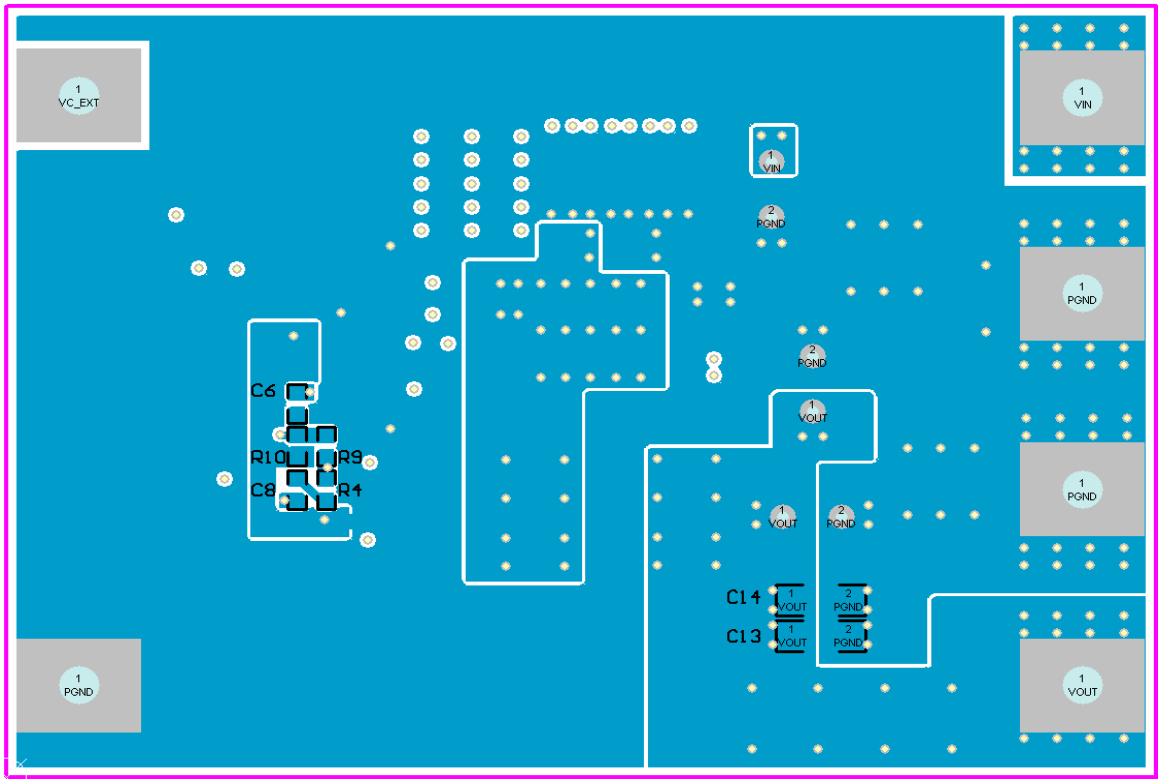

Figure 3d: IRPP3637-18A Reference Design bottom layer layout.

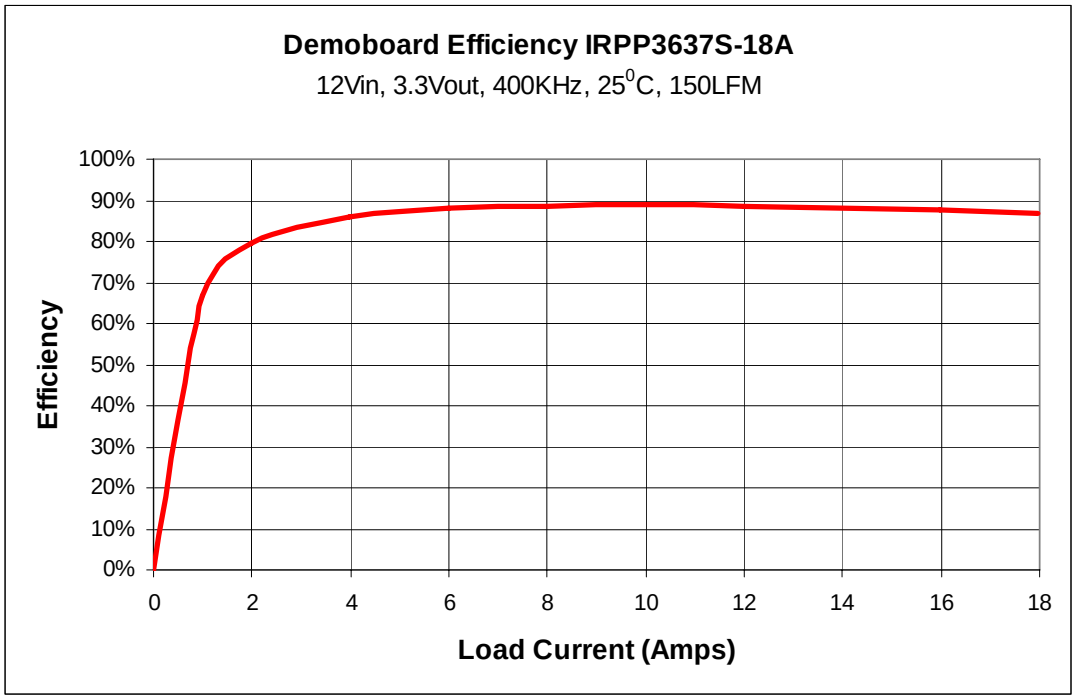

Figure 4a: IRPP3637-18A Reference Design Electrical Efficiency

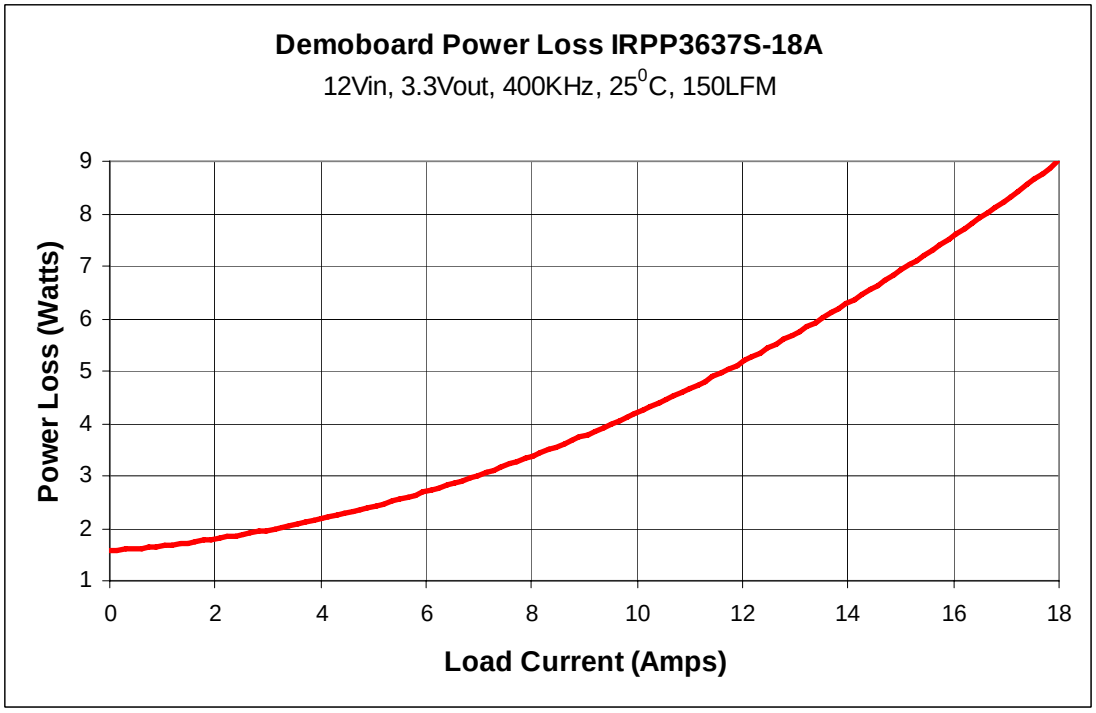

Figure 4b: IRPP3637-18A Reference Design Power Loss Curve

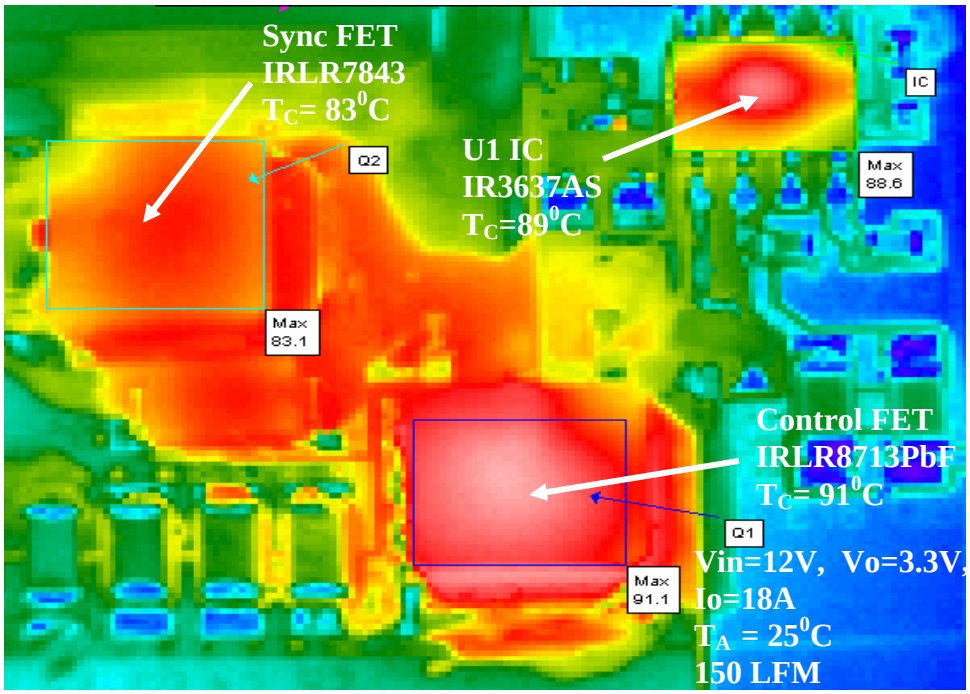

Figure 5: IRPP3637-18A Reference Design Thermograph at 18A load

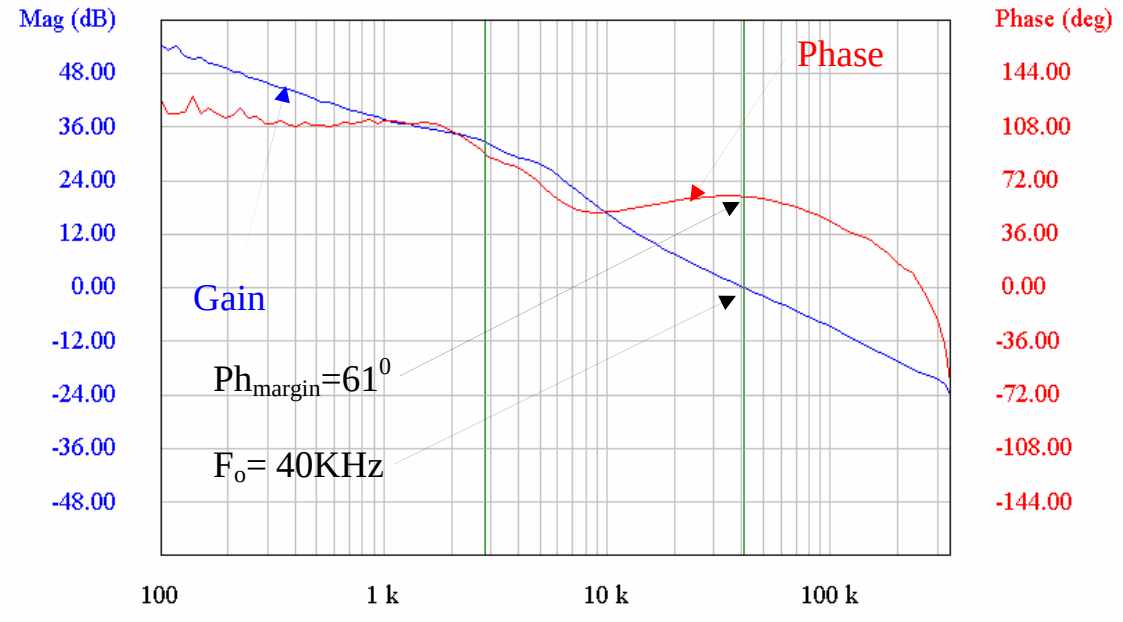

Figure 6: IRPP3637-18A Reference Design Bode Plot of the Control Loop at 18A load.

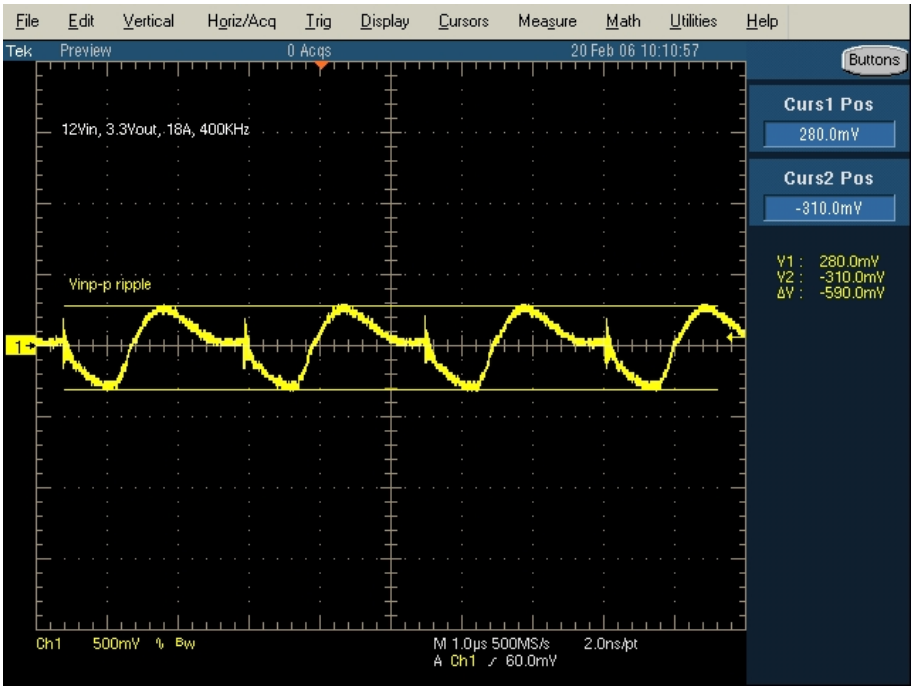

Figure 7: Input ripple, I_O=18A

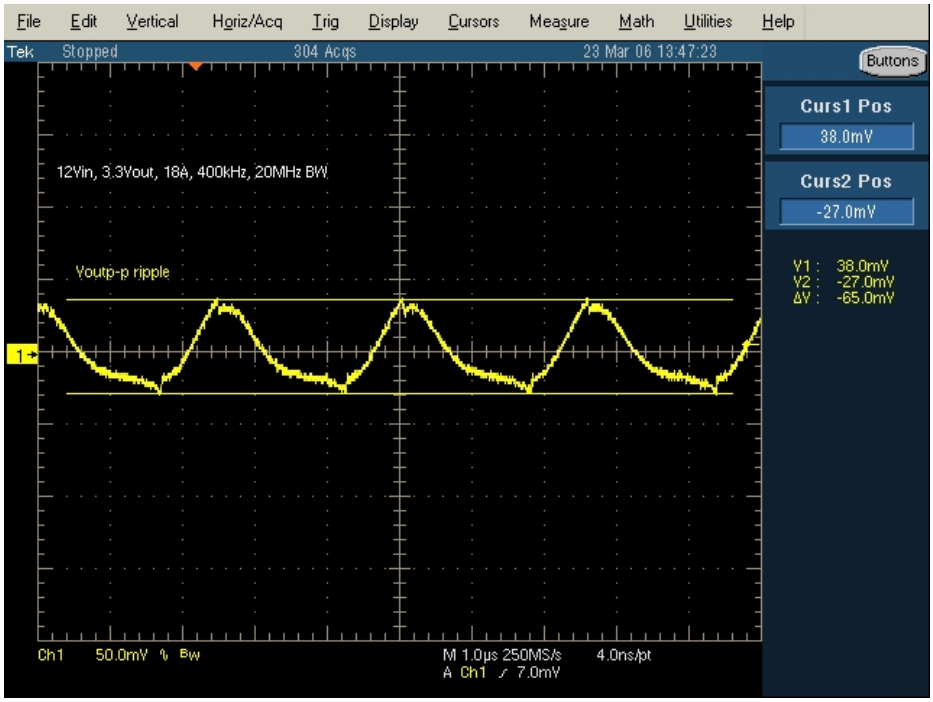

Figure 8: Output ripple, I_O=18A

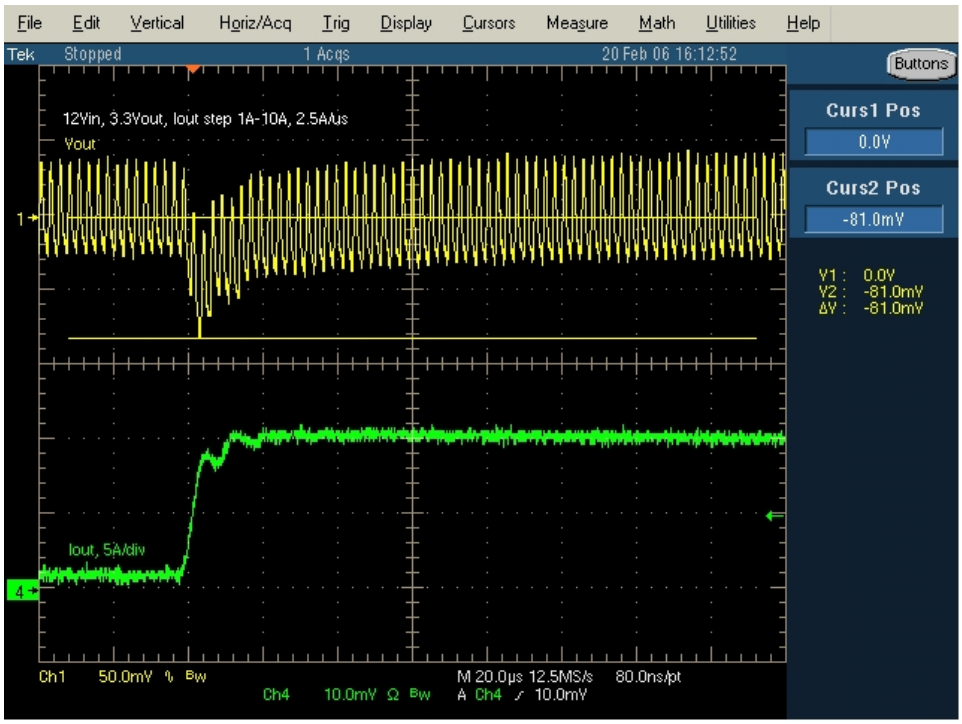

Figure 9: Output Voltage undershoot due to 1A to 10A load step, di/dt=2.5A/us

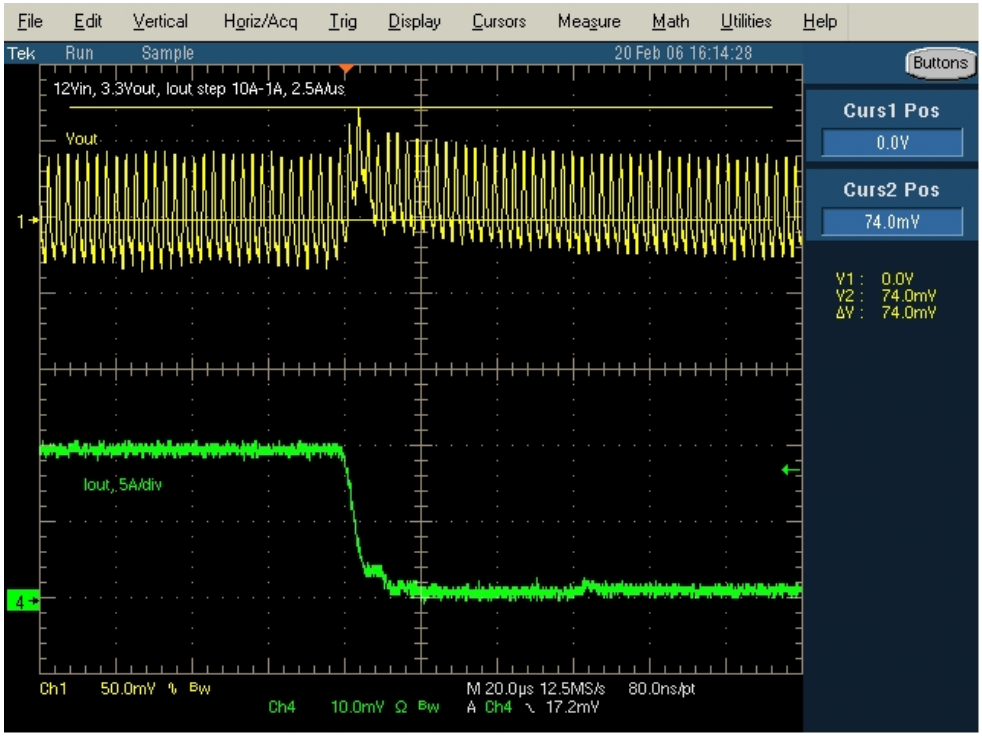

Figure 10: Output Voltage overshoot due to 10A to 1A load step, di/dt=2.5A/us

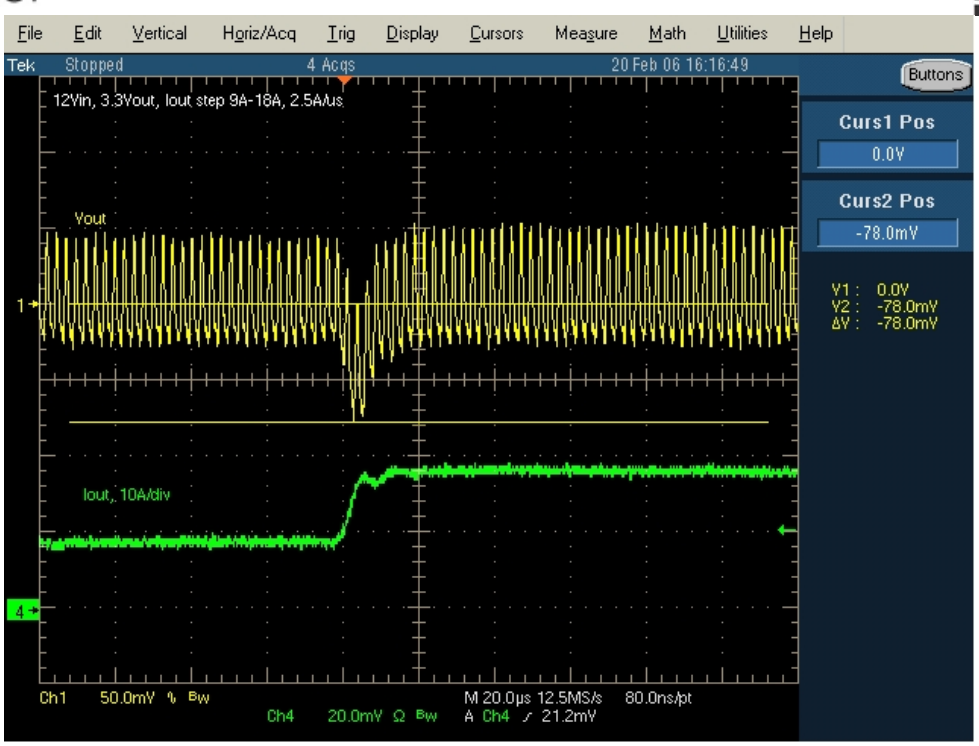

Figure 11: Output Voltage undershoot due to 9A to 18A load step, di/dt=2.5A/us

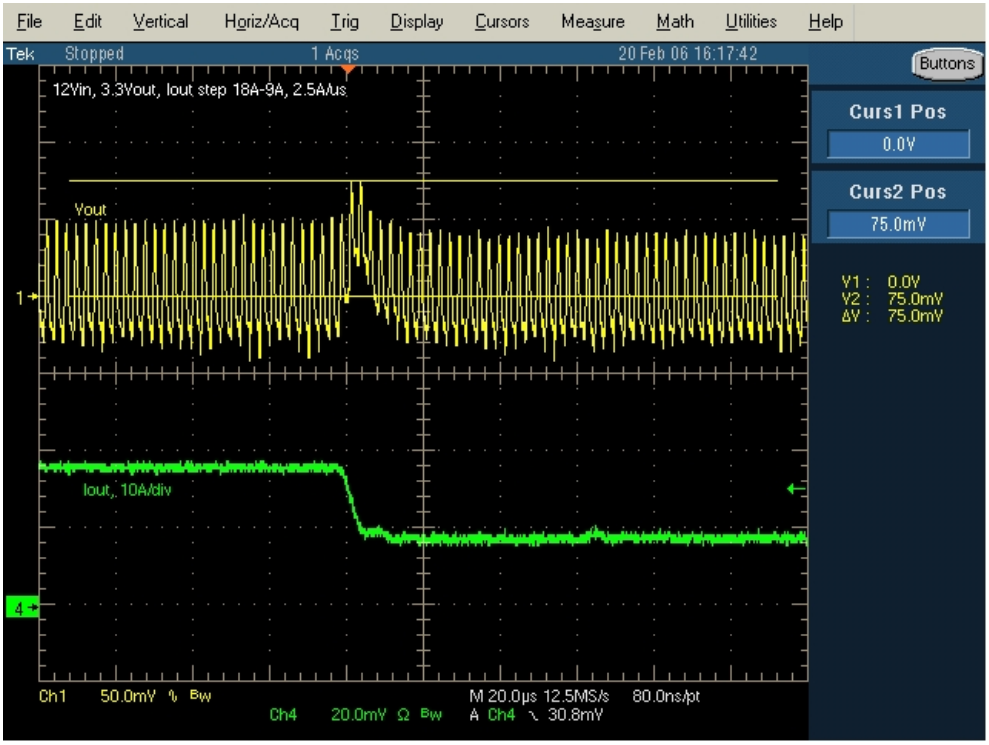

Figure 12: Output Voltage overshoot due to 18A to 9A load step, di/dt=2.5A/us

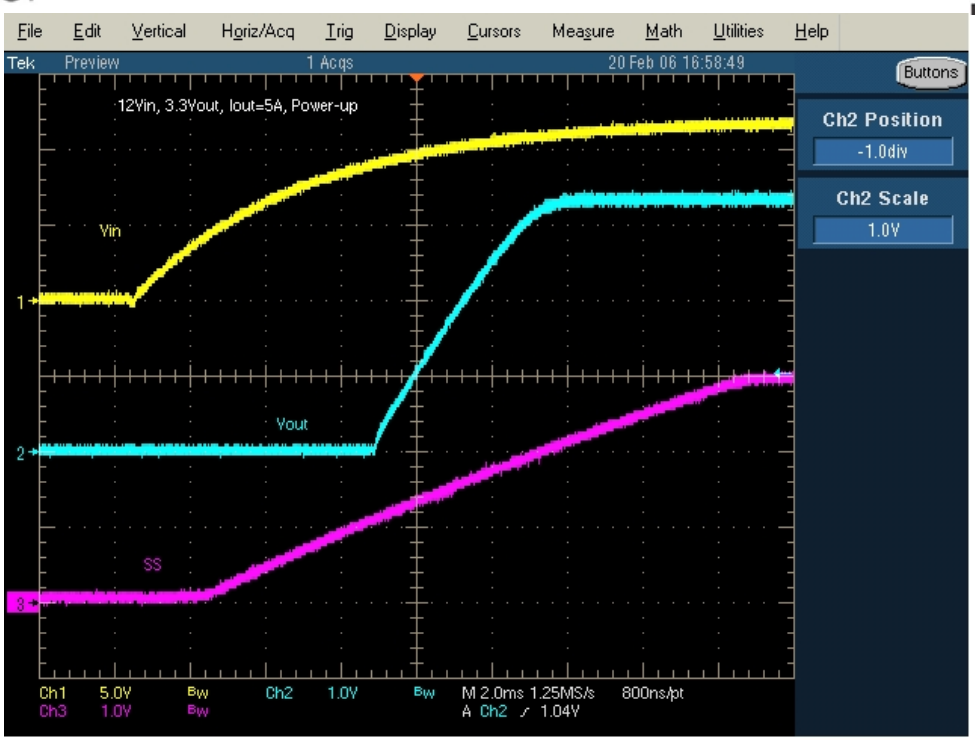

Figure 13: Power up. Ch1=V_{IN}, Ch2=V_{OUT}, Ch3=Soft Start

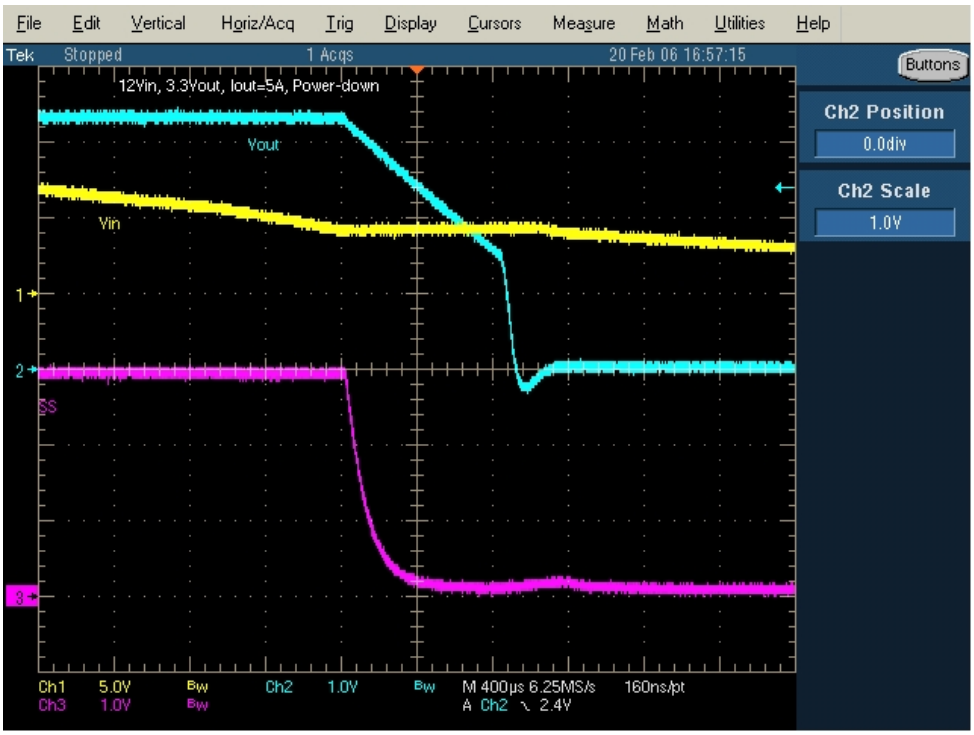

Figure 14: Power down. Ch1=V_{IN}, Ch2=V_{OUT}, Ch3=Soft Start

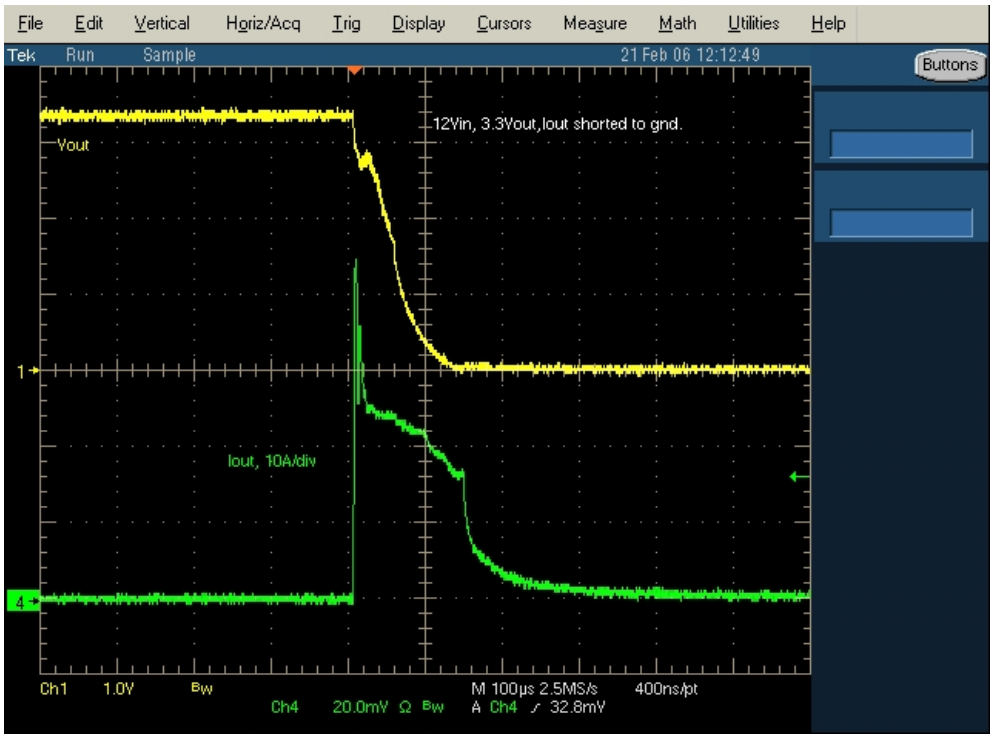

Figure 15: Output short circuit protection. Ch1=V_{OUT}, Ch4=I_{OUT}10A/div

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (A)	Max Power (W)	Efficiency (%), 25^{0}C, 150 LFM	$V_{INripple}$ (mVp-p)	$V_{OUTripple}$ (mVp-p)	Line Regulation (%)	Load Regulation (%)
12V	3.3V	18A	60W	88%	590mV	65mV	0.06%	0.16%

Table 2 – IRPP3637-18A Reference Design Performance Summary
(all values are typical)

Part Number	Input Voltage	Output Voltage	Output Current	Switching Frequency	Power Semi BOM	Delivery Time	Comments
IRPP3637-06A	5V	1.25V	6A	600kHz	IR3637AS (SO-8), IRF8910 (Dual SO-8)	24-48hrs	Standard Reference Designs Fixed BOM
IRPP3637-12A	12V	1.8V	12A	400kHz	IR3637S (SO-8), IRF7823 (SO-8), IRF7832Z (SO-8) Option to populate S-Can DirectFETs		
IRPP3637-18A	12V	3.3V	18A	400kHz	IR3637S (SO-8), IRLR8713 (D-Pak), IRLR7843 (D-Pak)		
Custom IRPP3637-06A	3.0V to 13.2V	0.8V to 5.0V	Up to 6A	400kHz or 600kHz	Various	1-2wks	Customizable Reference Designs via POWIR+ Chipset On-line Design Tool at http://powirplus.irf.com
Custom IRPP3637-12A			Up to 12A				
Custom IRPP3637-18A			Up to 18A				

Table 3 – Complete IRPP3637-xxA Reference Design Selector Table