

# Efficiency in SMPS Output Stage

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**Abstract.** By means of the SPICE Schottky diode model, developed recently by International Rectifier, we are able to predict the efficiency in Switch Mode Power Supply (only considering the output stage). The strength of the mathematical model is represented by the possibility to know the forward voltage drop and the leakage current as a function of temperature.

## 1. Introduction

The possibility to know and predict the efficiency of an application is thus far one of the most vital and fascinating pieces of information both for the designers and for the application engineers (not to mention the marketing and sales people).

In this paper, we provide answers to the request of an efficiency evaluation at different temperatures of a Switch Mode Power Supply (SMPS). We consider only the output stage and, in particular, the forward and push-pull topology.

In forward topology, the two diodes are supposed to have two different duty cycles. Specifically, these are equal to 32% and 68%, when the application works at maximum temperature. In push-pull topology, instead they have the same duty cycle: 50%.

For Schottky diodes, these two topologies provide the same power dissipation, as it comes out straightforwardly from the mathematical model.

The range of voltage and current reckoned with is respectively comprised between 3.3 V and 5 V and between 20 A and 30 A. The tool is, in any case, versatile enough to allow any physical range.

Explicitly, we build the following matrix, in which we report also the suitable diodes.

The paper is structured in the following way. In section 2, we described briefly the theory and the procedure to evaluate the efficiency. In section 3, we present and discuss some results. Finally, in section 4, the conclusions are drawn and future work is discussed.

Output Current	Output Voltage	Diodes	Diodes
30A	30A	40CTQ30	47CTQ20
30A	30A	47CTQ20	40L15
20A	20A	30L30	30L20*
20A	20A	19TQ15	19TQ15

## 2. How we evaluate the efficiency

The scheme to evaluate the efficiency is very simple, even though there are some mathematical subtleties.

Let us try to elucidate this statement.

It is known that for any diode there exists a critical temperature  $T_c$  so that the

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\*30L20 is not yet available, but one of the possibilities of the developed SPICE model is to predict the alteration in the characteristic once the process is maintained fix and the area is accordingly scaled.

forward power loss is equal to the reverse power loss, and this is true for any level of current.

This is equivalent to say that, for any I,  
 $P_F(I, T_c) = P_R(T_c)$

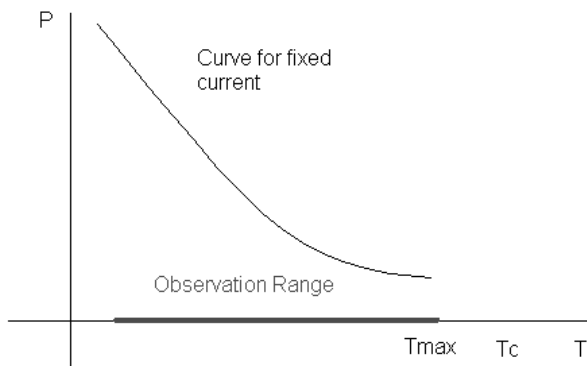
Usually for commercial diodes, before  $P_R$  becomes of the same order of magnitude of  $P_F$ , we need a very high critical temperature (more than 150°C).

The total dissipated power P is defined as the sum of the forward and reverse dissipated power.

Let us distinguish two cases.

1. If the range of temperatures, in which we perform our analysis, is limited and the maximum temperature is below  $T_c$ , we have only the contribution coming from  $P_F$ .

Considering that for any level of current, the forward power loss is a decreasing function of the temperature, we get the following plot.



In this case, the equation

$$P(T_{eq})R_{th}^{j-a} = T_{eq} - T_{amb}$$

is invertible, i.e. it provides a unique solution for any equilibrium temperature.

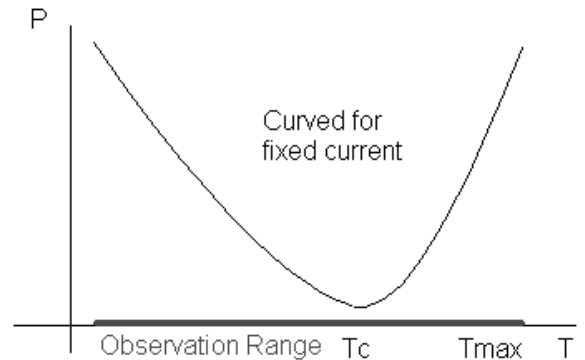
2. Conversely, in the case of diodes with Low Schottky Barrier Height Diodes (hereafter

LSBHD) or Trench Schottky Diodes (hereafter TSD) with high leakage current, the scenario is deeply different. If the observation range is wide enough, the total power loss, for any level of current, is portrayed by a decreasing branch (mainly due to forward power loss) and an increasing branch (mainly due to reverse power loss).

Unfortunately, in this case, the equation

$$P(T_{eq})R_{th}^{j-a} = T_{eq} - T_{amb}$$

is not invertible, since we have two possible temperatures, which provide the same power loss.



From this premise, it should be clear that for the diodes of the first category, at any current, the efficiency is an increasing function of the temperature. In this case, the maximum efficiency is reached at the maximum allowed temperature (provided it be less than the critical temperature,  $T_c$ )

We will see in a moment that the current and the temperature are related each other by means of a quantity defined as thermal resistance. In this last case, we refer to the temperature as the *equilibrium temperature*.

On the contrary, for LSBHD and TSD there exists a temperature, which

maximizes the efficiency for any level of current.

For the first category of diodes, stated a particular level of current, we can define the equilibrium junction temperature choosing accordingly the junction-to-ambient thermal resistance.

Not only, but since we can invert the equation

$$P(T_{cq})R_{th}^{j-a} = T_{cq} - T_{amb}$$

we can also choose the thermal resistance so that it matches a particular maximum temperature at the maximum current.

Once this is made possible, an interesting chart for the designer can be deduced; in it, we represent the efficiency as a function of the current and of the maximum temperature at maximum current (i.e. the junction-to-ambient thermal resistance). *Evidently in this plot, moving along the current, with constant thermal resistance, implies increasing the equilibrium temperature.*

Another meaningful chart is made up of the plot of efficiency in function of the current and the temperature (mind not confusing this non-equilibrium temperature with the foremost one). Now the plot is similar like whether we could vary *ad hoc* the junction-to-ambient thermal resistance. In this kind of chart, we proceed to evaluate the maximum point of efficiency (I, T) and then to estimate for that current what is the thermal resistance able to provide T as equilibrium temperature. At this point, we need to suppose that the thermal resistance value is compatible with silicon, package and heatsink of the device and application.

This second chart is much more interesting for LSBHD and TSD, since the temperature is crucial to identify the best efficiency operating point.

Any time the maximum observation temperature is below the critical temperature, we use the following scheme:

- 1) We start from calculating the junction-to-ambient thermal resistance, which provides a certain maximum junction temperature, when operating at maximum output current. The equation is

$$R_{th}^{j-a}(T_{max}) = \frac{T_{max} - T_{amb}}{P_d(I_{max}, T_{max})}$$

- 2) Now, with that fixed thermal resistance, we are able to evaluate the various equilibrium temperatures at different levels of current. Evidently for current equal to the maximum one, we get an equilibrium temperature equal to the maximum temperature, related to that particular thermal resistance.

The equation to solve for any current is then

$$P_D(I, T_{cq}, \delta_1, \delta_2) \cdot R_{th}^{j-a} = T_{cq} - T_{amb}$$

- 3) Finally we can obtain the efficiency directly from the formula

$$\varepsilon = \frac{V_{out} \cdot I}{V_{out} \cdot I + P_D}$$

$$P_D = P_{D1} + P_{D2}$$

$$P_{D1} = V_F[I, T_{cq}(I)] \cdot I \cdot \delta_1 + I_R[V_{out}, T_{cq}(I)] \cdot V_{out} \cdot (1 - \delta_1)$$

$$P_{D2} = V_F[I, T_{cq}(I)] \cdot I \cdot \delta_2 + I_R[V_{out}, T_{cq}(I)] \cdot V_{out} \cdot (1 - \delta_2)$$

We implement the model to take in consideration the fact that the duty cycle depends on

the rated current. This means that we suppose  $\delta_1$  and  $\delta_2$  varying linearly with the current, respectively from 10% to 32% (50%) and from 90% to 68% (50%). The range of current in which this variation occurs is between 5% and 100% of the rated current.

In the other case, for LSBHD and TSD, we apply the above scheme but limiting to temperature inferior to the critical temperature.

### 3. Results

We are now ready to show some of the results.

As far as the efficiency has a double dependency on the maximum temperature at maximum current and on the peak current, we need to represent the results using a contour chart (type I).

We do the same also for the case in which we plot the efficiency as a function of the non-equilibrium temperature\*\* and of the current (type II).

The meaning of this kind of chart is somewhat simple, because at any color it corresponds a definite range of efficiency defined in the legend.

*Example 1. IR19TQ15 for 3.3V and 20 A*

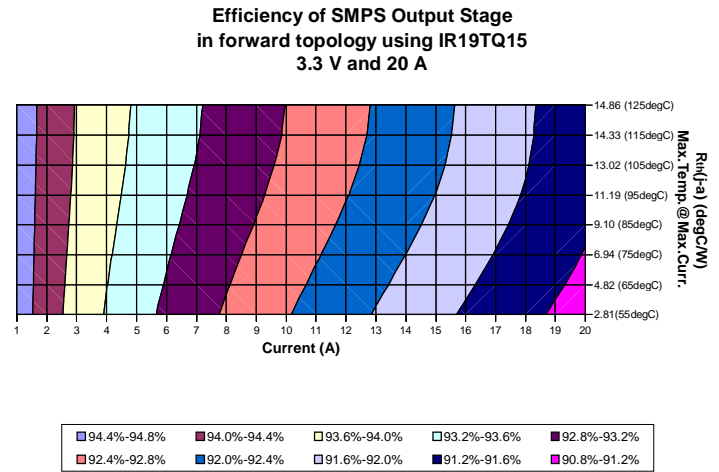
Only for this case, we are going to show all the charts we can obtain directly from our Schottky Spice model.

In Fig.1, you can easily recognize that for 20 A and 3.3 V, the efficiency occupies several large regions. Not only but, fixing the junction-to-ambient thermal resistance,

\*\* The kind of approach used in this paper can be easily extended to other devices if we exchange the role of temperature with frequency.

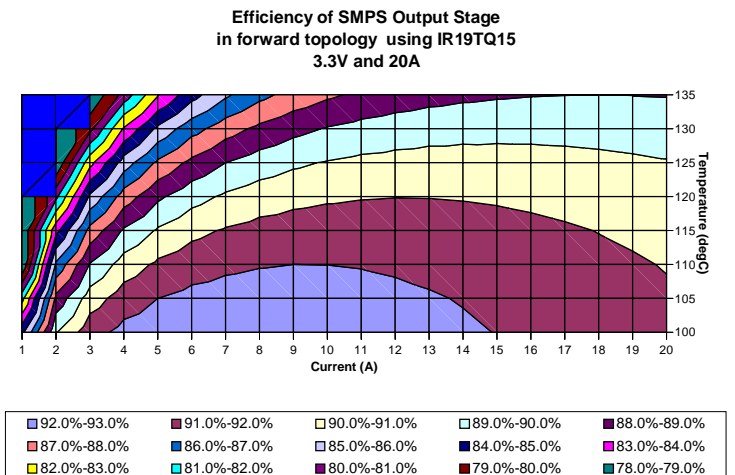
we see that the efficiency decreases as we increase the current.

What is likely more interesting is represented by the efficiency plotted in function of the temperature and of the current (see Fig.2).



**Figure 1. Efficiency Contour Chart of SMPS plotted as a function of current and junction-to-ambient thermal resistance.**

In fact, in the contour plot, a maximum efficiency region is clearly visible in bleu. In this region, the efficiency varies between 93% and 92%.



**Figure 2. Efficiency Contour Chart of SMPS plotted as a function of current and temperature.**

This region extends up to 110°C in temperature and is between 3.6 A and 14.8 A in current.

Then we move into the plum region of efficiency between 92% and 91% and so on.

In Fig.3, we extract a piece of information from the contour plot of Fig.2, fixing the temperature at 110°C and 135°C.

As we can see at 110°C there exists a maximum of efficiency of approximately 92% for about 10 A.

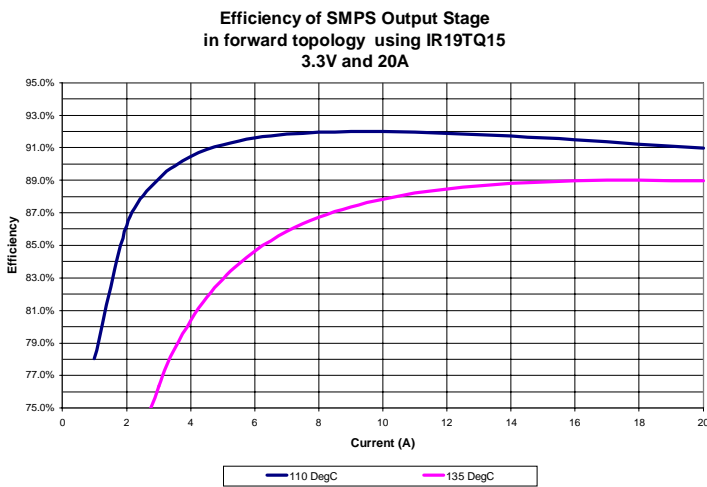


Figure 3. Efficiency at two fixed temperatures in function of current.

Not so good is the situation at 135°C, where likely the maximum is located at 17.5 A. The maximum efficiency reaches 89%, that is 3% less in this case compared with the aforementioned.

From these first plots, we can easily be acquainted with the information provided by this tool.

Example 2. IR30L30 vs. IR30L20 for 5V and 20 A

This example has the aim to show at what extent it is true that a smaller device is less efficient than a bigger one.

*A priori*, we know that altering only the die size changes the saturation current and

the series resistance. Formally the first one increases with the area, while the second one decreases. The first one increases the overall diode current, especially in the reverse direction, while the second one limits the forward voltage drop.

These opposite trends have allowed estimates and opinions, based upon the experience, but characterized by the flaw of uncertainty.

Now, we would like to assert that our tool is undoubtedly able to yield the efficiency values and to compare the same device but scaled down in die size.

That is, while IR30L30 has a die size of 125x125 mils<sup>2</sup>, IR30L20 has 105x125 mils<sup>2</sup>.

The application taken in consideration in this example has as voltage output 5 V and maximum rated current 20 A.

As it is clear looking at Fig.4, IR30L30 is always better than IR30L20.

Another interesting feature is the high efficiency offered by this component, since it is superior to 92%.

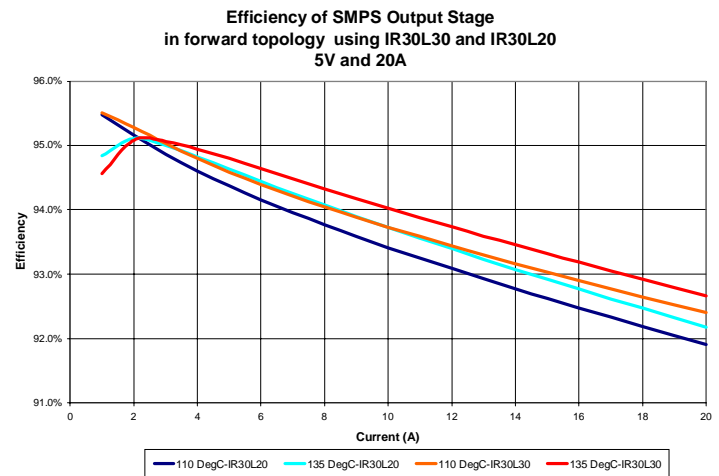


Figure 4. Comparison between IR30L30 and the same device scaled down in the die size.

Example 3. IR40L15 vs. IR47CTQ20 for 3.3 V and 30 A

Now we are going to propose a comparison between IR40L15 and

IR47CTQ20 for the SMPS working at 3.3 V and 30 A.

Efficiency of SMPS Output Stage in forward topology using IR40L15 at 3.3 V and 30 A

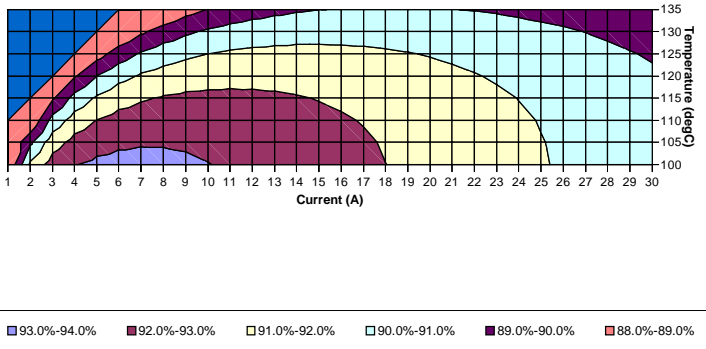


Figure 5. Efficiency Contour Chart of SMPS plotted as a function of current and temperature.

We can appreciate in this example the different behavior of LSBHD (Fig.5) and of standard diode (Fig.6).

A standard diode belongs to the first category examined above at the beginning of the paper. We have explained that this kind of diodes does not show the minimum in the power loss and then equivalently does not show the maximum of efficiency, except over the critical temperature  $T_c$ .

On the contrary, LSBHD and TSD do show definitely a maximum efficiency point.

Efficiency of SMPS Output Stage in forward topology using IR47CTQ20 at 3.3 V and 30 A

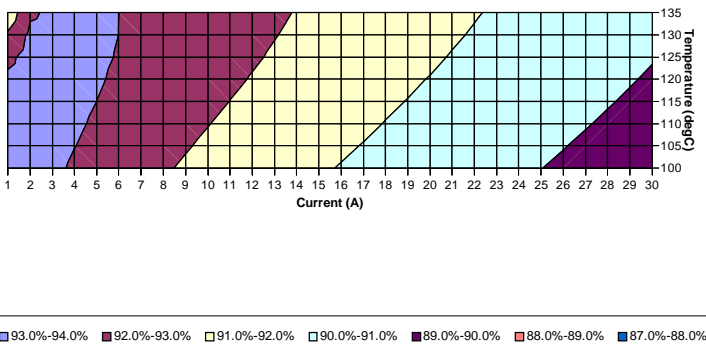


Figure 6. Efficiency Contour Chart of SMPS plotted as a function of current and temperature.

In Fig.7, we can see the different efficiency values for two fixed temperatures, namely 110°C and 135°C.

Efficiency of SMPS Output Stage in forward topology using IR40L15 and IR47CTQ20 at 3.3 V and 30 A

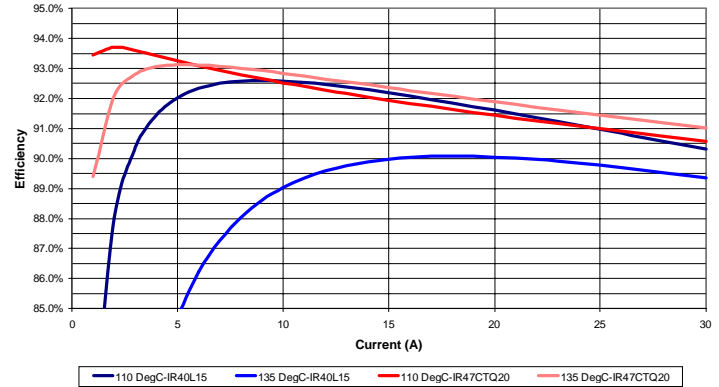


Figure 7. Efficiency comparison for forward topology.

This comparison is very intriguing because of the opposite behavior of the two devices: IR40L15 decreases drastically its efficiency when we raise the temperature from 110°C to 135°C; IR47CTQ20 performs exactly in different way, as it raises its efficiency with the increase of temperature.

This means that for 110°C, IR40L15 is more efficient for current comprised between 10 A and 24 A. For 135°C, IR47CTQ20 is evidently much more efficient than IR40L15. In any case, compelled to choose a device for a real SMPS application, we would have no doubts to suggest the use of IR47CTQ20

Example 4 IR42CTQ30 vs. IR47CTQ20 for 5V and 30 A

This example aims at illustrating again the main feature of this tool: the possibility to predict qualitatively and to estimate quantitatively the efficiency of a SMPS (output stage) comparing different devices, *a priori* suitable for this application.

In this simulation the application considered is 5 V and 30 A.

Efficiency of SMPS Output Stage  
in forward topology using IR42CTQ20 and IR47CTQ30  
at 5 V and 30 A

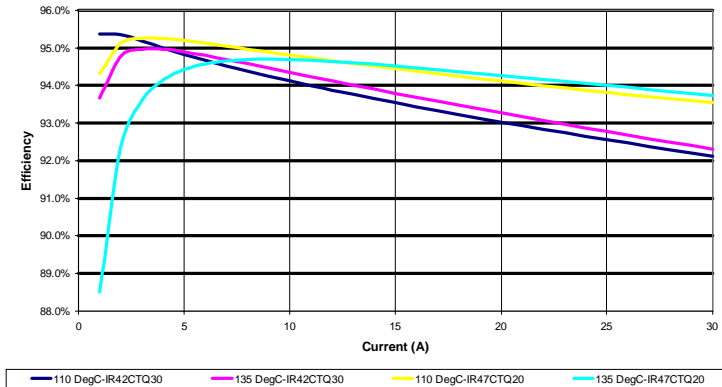


Figure 8. Efficiency comparison for forward topology.

In Fig. 8, it is evident that IR47CTQ20 performs better than IR42CTQ30 at the two different temperatures, taken in consideration.

#### 4. Conclusions

In the paper, we have presented few example of a new tool that International Rectifier has recently developed to estimate the efficiency in a Switch Mode Power Supply, considering only the output stage.

The tool is not only able to yield the different values of efficiency but it visually shows the different patterns associated to a certain device in a particular application.

What is going to surface by this work is the necessity to develop a new language for International Rectifier, probably much closer to the customer.

The old and overused approach to the diode performance, regarding as fundamental the forward voltage drop and the reverse leakage current, must be enlarged to embrace for example the efficiency of the application.

A simple Excel Macro will be soon available to run simulation and comparison using a database of SPICE models of International Rectifier Schottky diodes.

Using this simplified version of the software program written during this study, every SMPS design engineer will be able to easily select the best output rectifier for any type of converter stage.

#### Acknowledgements

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