

# Intelligent Power Switches (IPS): Basic Features & Protection

By X. de Frutos and A. Mathur, International Rectifier

## INTRODUCTION

Intelligent Power Switches (IPS) are IR's High Side and Low Side Protected Power MOSFETs. IPS devices are designed to safely handle ordinary overload conditions as well as several extraordinary conditions. In this Design Tip, we will look at some of the most important, though basic, protection features that IPSs offer. Initially, however, we will overview the main considerations for various loads, and how to choose an IPS based on these considerations.

### 1. CHOICE OF IPS FOR DIFFERENT LOADS

#### 1-1 Filament bulbs

As shown in Fig. 1a, the inrush current from a filament bulb can exceed 10 times the rated current. Therefore IPSs with current limitation features are preferred. To decide on the current limitation value,  $I_{lim}$ , one needs to make a trade-off between the power dissipated (in the linear mode) and the protection level. As an initial approximation, a value of about 6 times the nominal current is commonly used for  $I_{lim}$ . However, it is important to ensure that the junction temperature does not exceed the protection temperature limit (Fig 1c). Perform tests to verify that the difference between the highest junction temperature and the protection limit (shown in Fig 1c as  $\Theta_{margin}$ ) is a safe value. If needed, a detailed temperature profile can be evaluated by simulation (using a bulb model).

#### 1-2 Inductive loads

Inductive loads are efficiently protected by an IPS with either over-current (OI) shutdown or current limitation features. There are several points to bear in mind when designing around an inductive load. First, for electromechanical devices (electrovalves, relays, etc), the inrush peak current due to the inner air gap must not trigger the OI shutdown. Second,

one should ensure that the current and temperature never exceed the protection limit for the worst condition. Third, the Active Clamp effect (described in Section 3) also has to be accounted for. However, for a first order approximation, use the curve 'Max. Current-out vs Load Inductance' shown in the datasheets. (Fig. 10 in the IPS 511 datasheet is an example of such a graph).

#### 1-3 Resistive Loads

Resistive loads are efficiently protected by an IPS with either an over-current shutdown or a current limitation. As a first order design approximation, refer to the datasheets for the table 'Recommended Operating Conditions' and for the graph 'Current-limit vs. Junction Temperature,' (e.g. Fig. 13 in the IPS511 datasheet). After this, one should evaluate the current and temperature for the worst operating conditions, to ensure that they are within the protection limits. Change the design accordingly.

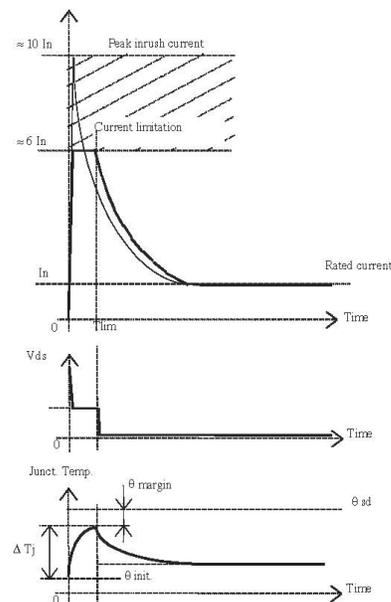


Figure 1: Filament Bulb Inrush Current.  
 (a) Current Profile (b) Vds Profile (c) Temperature Profile

## 2. OVER-CURRENT & OVER-TEMPERATURE PROTECTION

In many applications, extra protection circuits are required to satisfy the safety and reliability of the end system. The two most common (and lethal) problems are over-current and over-temperature. IR's IPS devices have been designed to protect against, among other things, these two basic maladies.

### 2-1 Over-Current Shutdown (OI)

The basic premise of over-current shutdown is self-explanatory: when the current exceeds the Current Shut Down limit ( $I_{sd}$ ), the switch is turned-off (shut down). There are two possible modes for overcurrent. One is caused when the load short-circuits under constant input. Fig. 2a shows the waveforms associated with the shutdown for this case.

The other mode of over-current is when the switch turns on with a short-circuit of load. See Fig. 2b for the shutdown for this type of over-current. The time taken to shut down can be evaluated from the ' $I_{ds}$  vs. Time' curve. For instance in Fig. 2a, Curve 2, the shutdown time (the time between the initial rise of current and subsequent return to normal) is about 14 micro-seconds, while in Fig. 2b, it is about 11 micro-seconds. (The current shutdown time is actually a function of the peak current, the inner delay, and the  $dI/dt$  slope.) Note that the Active Clamp is activated at the end of each short-circuit as evidenced by the rise in  $V_{cc}$ . To reset the IC,

hold the input voltage low for the minimum reset time ( $T_{reset}$ ), as specified in the Protection Characteristics Table in the datasheet.

### 2-2 Current Limitation ( $I_{lim}$ )

In the current limitation protection type, the IC continuously checks the drain current. When the drain current reaches the  $I_{lim}$  value, an inner current loop drives the power MOSFET in a linear mode. However, this protection type reacts differently under the two possible modes of over-current. In the first case, where the load short-circuits during an on phase (Fig. 3a), there is a sharp current peak before the current limiting protection sets in. However, in the second case (when the switch turns on with the drain short-circuited), the limitation is a lot smoother. As can be seen in Fig 2b, there is no sharp spike in the current. Yet, the response time in both cases keeps the instantaneous current within the power MOSFET Safe Area. Current limitation is sustained until the over-temperature protection sets in (Section 2-3).

### 2-3 Over-Temperature Protection

Over-temperature protection is the last line of defense against slow current increases, e.g. during an over-load. As the name implies, when the junction temperature exceeds the shutdown temperature limit,  $T_{sd}$  (typically 165°C), the switch is turned off. Actually, this type of protection causes the switch to latch off.

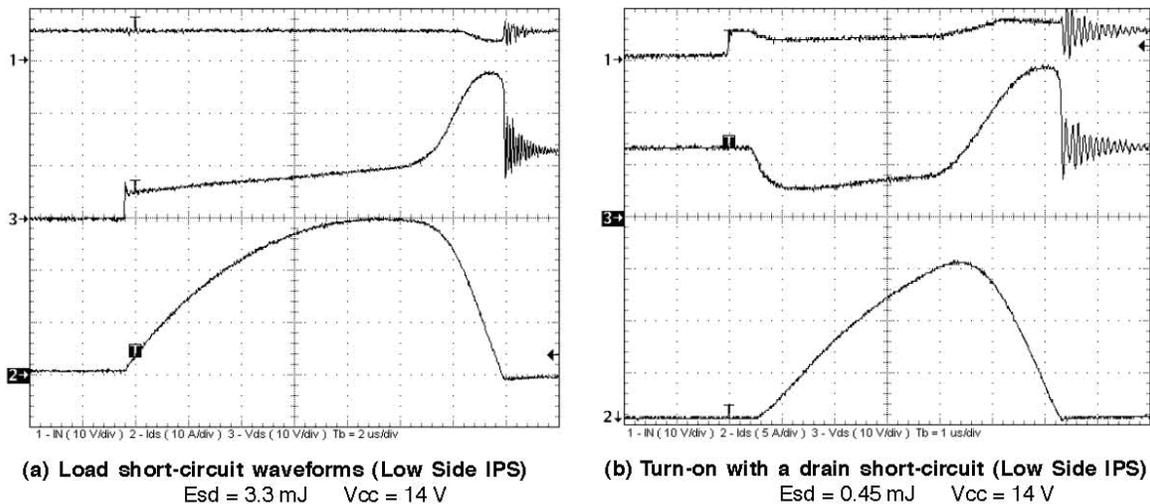


Figure 2: Over-current Shutdown

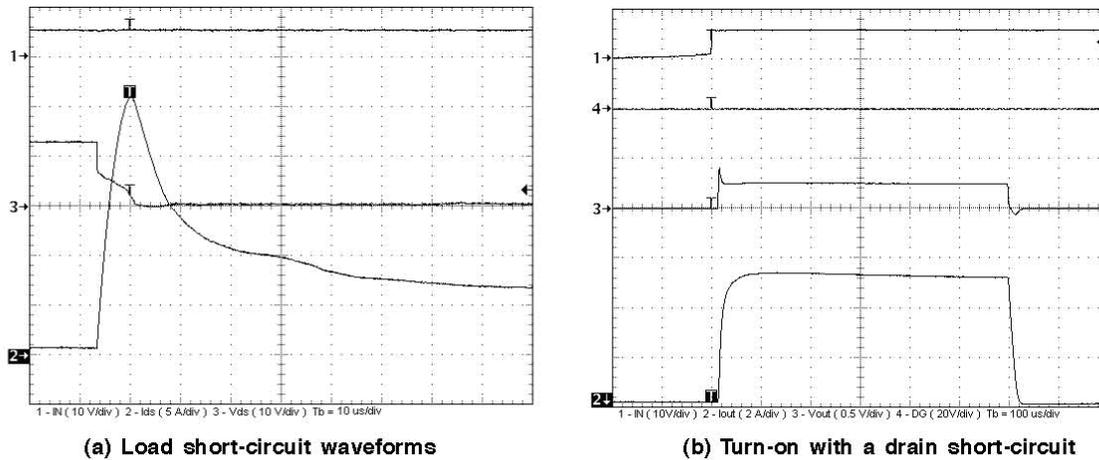


Figure 3: Current Limitation Protection

To reset the IPS, hold the input voltage low for a minimum reset time,  $T_{reset}$  (given in the 'Protection Characteristics' table of the datasheet). When the device has an automatic restart (with hysteresis), it latches on after the junction temperature falls down to its restart value (typically 158°C). Precautions when Designing for Over-temperature protection:

- OT shutdown is a protection. Do not use it as a functional threshold (whether as a thermal oscillator or otherwise). If used as a threshold, the junction temperature would permanently stay at about 160°C, and significantly (and adversely) affect the IPS's lifetime.

- The Active Clamp (Section 3) overrides the temperature protection. There is no way to interrupt the current in active clamp or reverse bias mode (body diode).

- In certain circumstances (e.g. switching into a hard short-circuit at high frequencies), a thermal runaway could occur. See the Design Tip on High Frequency Operation (DT99-5, Section 3).

### 2-4 Important Considerations when Designing for Over-Current and Over-Temperature Protection

The 'I<sub>ds</sub> vs. Protection Response Time' curve (I<sub>vs</sub>-T curve) provides an overview of the protection features of the IPSs. (Figure 14 in the IPS021 datasheet is an example). The representative I<sub>vs</sub>-T curve in Fig. 4 shows the region where over-current protection dominates, as well as the region where over-temperature protection takes over.

When designing the current path around the load, there are two key points to bear in mind. First, the path's current capa-

bility should always be higher than the curve shown, such that the current path does not burn out before the overcurrent protection kicks in. Second, the load's current capability should always be lower than the curve shown, such that one avoids false triggering of over-current protection.

## 3. ACTIVE CLAMP MODE

### 3-1 Purpose of Active Clamping

Turning off an inductive load requires additional consideration in the energy dissipation capabilities. Essentially the stored energy ( $\frac{1}{2}L.I^2$ ) will have to be dissipated by the power MOSFET. This dissipation is not dependent on the R<sub>ds(on)</sub>, but

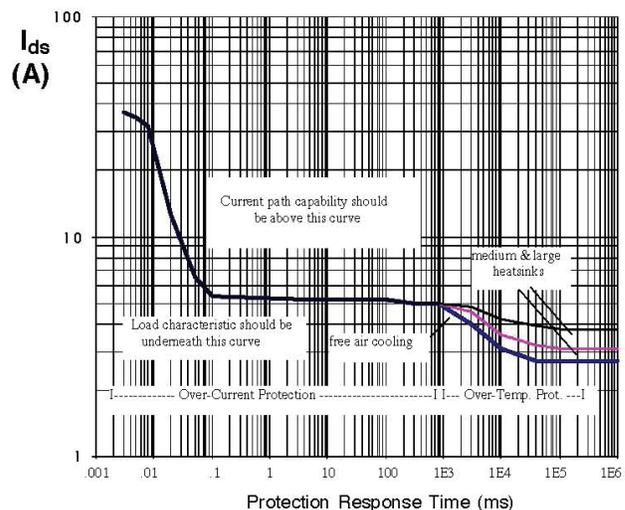


Figure 4: Protection Characteristic of IPS

rather on the energy rating of the die and the scheme of the inductive turn-off clamp. The re-circulation time for the load to be de-energized with the load current going to zero is a function of  $V_{clamp}$ . A higher value of  $V_{clamp}$  will be able to de-energize faster. Compared to conventional methods of dissipating this energy quickly (such as free-wheel diodes, Zener clamps, and MOSFET avalanches), active clamping provides the most efficient means to dissipate the energy stored in the inductor. Consequently, the active clamping feature is integrated into all IPS devices.

### 3-2 Active Clamping Methodology

The active clamp feature is shown in Figure 5. During the off-state, the power MOSFET is turned back on when  $V_{ds} > V_{zener} + V_{f,diode} + V_{threshold,MOSFET}$ . Also, there are two large resistances, the resistor and the MOSFET, within this current path to help dissipate energy. (Note that during the active clamp the FET is in a linear, or high-resistance, mode.) The load demagnetizes quickly during active clamp because the stored energy in the load is dissipated across a large potential  $[V_{cc} - V_{clamp}]$ . The larger the difference, the faster the demagnetization. The energy dissipated by the IPS during the Active Clamp sequence is  $V_{clamp} \times \int I_{ds}(t) dt$ .

The energy stored by the inductance is  $[V_{clamp} - V_{cc}] \times \int I_{ds}(t) dt$ . Thus, it is important to notice that during the active clamp sequence, the device dissipates more power than the load. (The current through the load and the IPS is the same but the voltage across the IPS is higher than the one across the load). The total energy dissipated by the IPS can be calculated using the formula:

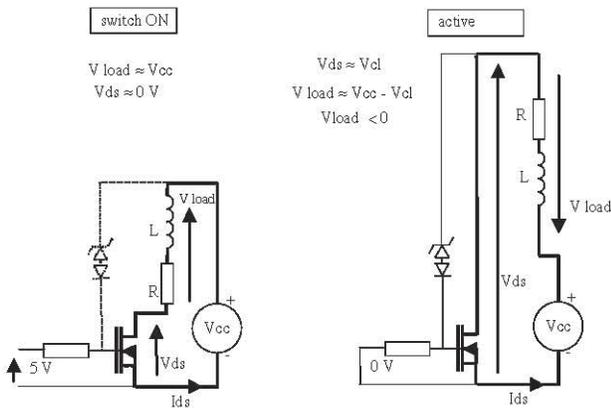
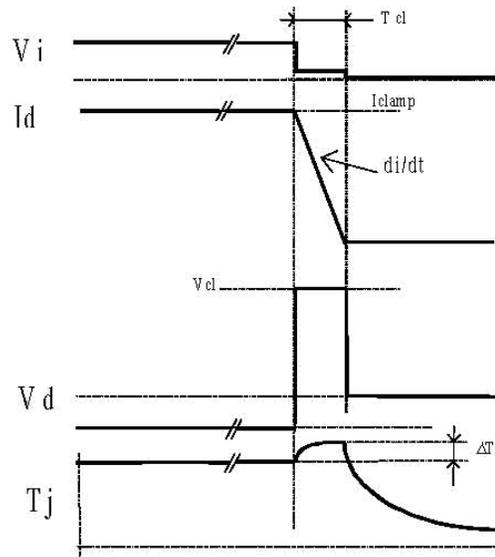


Figure 5: Active Clamp Circuitry



$$E_{IPS} = (\frac{1}{2} \cdot L \cdot I^2) \cdot (V_{clamp} / (V_{clamp} - V_{cc}))$$

The maximum inductive load allowed for each IPS can be estimated from the graph 'Iclamp vs Inductive Load', given in the datasheets (e.g. Figure 15 in the IPS021L datasheet).

### 3-3 Thermal Issues During the Active Clamp Mode

Junction temperature of the MOSFET rises during active clamp because the FET operates in the linear mode. When needed,  $T_j$  can be evaluated as follows:

$$di/dt \text{ of the Demag. current : } di/dt = [V_{cc} - V_{cl}] / L$$

$$\text{Clamping Time : } T_{cl} = I_{clamp} / di/dt$$

$$\text{Clamping average current : } I_{cl \text{ avg}} = I_{clamp} / 2$$

$$\text{Power dissip. during clamping : } P_{cl} = V_{cl} \cdot I_{cl \text{ avg}}$$

$$\text{Junction Temperature rise : } \Delta T_j = P_{cl} \cdot R_{th} \text{ (for } T_{cl})$$

Notes:

Load inductance in (H)

Voltages in (V) and Current in (A)

$R_{th}$  (for  $T_{cl}$ ) is the corresponding transient thermal impedance for  $T_{cl}$  (See 'Transient Thermal Imped. Vs Time' curve in the datasheet)

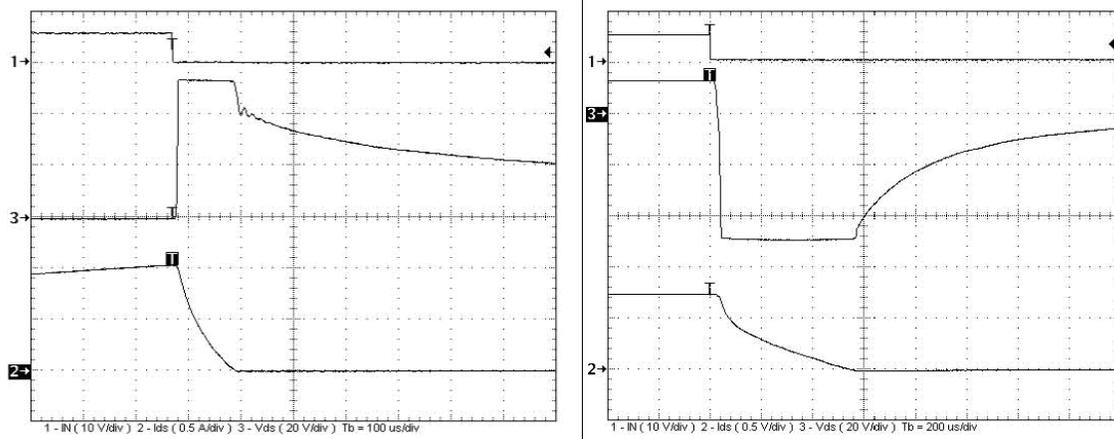


Figure 6: Clamping Waveforms. (a) Low Side Switch (b) High Side Switch

### 3-4 Active Clamping for High and Low side IPSs

The above discussion (and Figure 5) used a low-side switch architecture as the example. High side IPS devices work similarly. As the high-side switch is internally referenced to the Vcc pin, its drain goes below grounded during clamping. Figure 6a and 6b show Active Clamp waveforms for both low and high side switches.

For low side switches, the return path of the clamp includes the input pin. Sink current can be limited by adding a resistor in series with IN pin. IPS products are able to turn the load back on if the input is cycled while clamping.

## 4. PROTECTION CIRCUITRY WITH Vcc REFERENCED INPUT HIGH SIDE IPS

A Vcc referenced Input high side IPS is different from a regular high side IPS in that its input pin is referenced to the Vcc pin. Vcc referenced Input high side IPSs are usually used in the automotive environment, and therefore require the additional protective circuitry shown in Figure 7, whose components consist of:

- (a) A shottky diode (low current rated), to avoid a negative voltage at the microprocessor output under a reverse battery condition.
- (b) A zener diode, to protect the input against voltage peaks, and
- (c) A resistor, Rin, to limit the diode current. The maximum value of this resistor can be calculated as:

$$R_{in} < \frac{V_{cc \text{ min}} - V_{ih} - V_f - V_{ce}}{I_{in \text{ on}}}$$

where Vcc min = minimum operating Vcc voltage (V)

Vih = high level input threshold voltage (V)

Iin on = typical current for the input pin (A)  
(Vcc-Vin = Vih)

Vf = diode forward voltage drop (V)

Vce = open collector voltage (V)

Rin = input resistor (W)

In a Vcc referenced Input high side IPS, a high current flows through the Vcc pin. Any parasitic resistance in series with this pin will significantly modify input threshold because the voltage drop across the parasitic resistor acts as a voltage feedback to the input. One must, therefore, make an effort in board layout, to minimize such parasitic resistance.

## 5. CONCLUSION

This Design Tip is meant to explain only the basic features and protections offered by IPS devices. For further information on the Switching and Diagnostic capabilities of these devices,

