

USING STANDARD CONTROL IC'S TO GENERATE NEGATIVE GATE BIAS FOR MOSFETS AND IGBTs

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INTRODUCTION

Inherently neither the MOSFET nor the IGBT requires negative bias on the gate. Setting the gate voltage to zero at turn-off insures proper operation and virtually provides negative bias relative to the threshold voltage of the device. Negative gate bias does not significantly affect switching speed as opposed to the bipolar transistor. However, there are circumstances when a negative gate drive is necessary:

- The semiconductor manufacturer specifies negative gate bias for the device
- When the gate voltage can not be held safely below the threshold voltage due to noise generated in the circuit.

Although reference will be made to IGBTs, the information contained is equally applicable to power MOSFETs.

DC GATE CHARACTERISTICS

The minimum threshold voltage for most IGBTs is 3V at room temperature. The temperature coefficient of the threshold voltage is always negative; increasing junction temperature results in decreasing threshold voltage. If the junction temperature rises from 25°C to 150°C, and the temperature coefficient is -11 mV/°C,

then the threshold voltage decreases by 1.4V. Thus, a threshold voltage of 1.6V can be expected at high temperature and worst case conditions.

DYNAMIC OPERATION

The problem arises when the voltage increases rapidly between the collector-emitter terminals of the IGBT. During the transient, the gate-collector (Miller) capacitance delivers charge to the gate, increasing the gate voltage. The height and width of the voltage 'blip' at the gate is determined by the ratio of the gate-collector and gate-emitter capacitances, the impedance of the drive circuit connected to the gate, and the applied dV/dt between the collector-emitter terminals.

The internal capacitances are given on the data sheet. Notice the Miller capacitance of the IGBT is smaller than a similarly rated MOSFET, due to the smaller die size.

The impedance to the gate can be minimized by selecting a low impedance Control IC and by minimizing the stray inductance in the drive loop.

The dV/dt can be set to an optimum value (noise versus losses) by selecting the proper value of series gate resistor. The series gate

resistor affects only the turn-on speed of the IGBT, the turn-off speed is largely determined by the IGBT itself. A parallel diode, with the anode towards the gate, across the gate resistor is also recommended. The diode is reverse biased at turn-on but holds the gate down at turn-off, and during the off state.

The Control IC has to have an electrically separated reference pin for the gate drive output. This pin should be connected directly to the emitter terminal of the IGBT, or the Kelvin terminal of the IGBT module. The gate and the emitter voltages are then floating on top of the noise generated by high current ground wiring, but the difference of the two voltages (the effective drive voltage) is free from the noise.

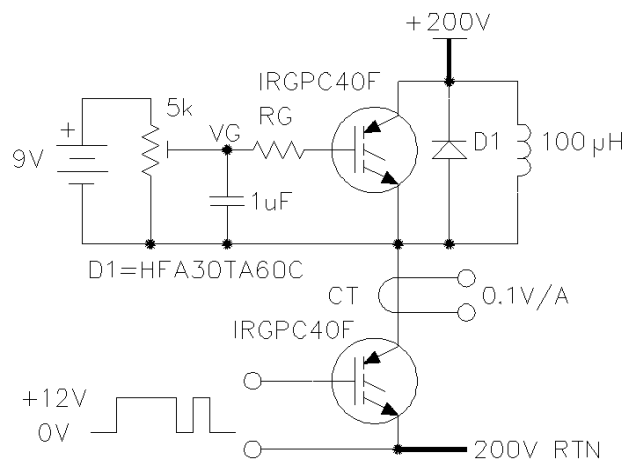


Figure 1
Test Circuit

INTERNATIONAL RECTIFIER's IGBTs DO NOT REQUIRE NEGATIVE BIAS

The IGBTs made by International Rectifier do not require negative bias. The switching times and energy loss values that are published on the data sheets for both discretes and modules were measured at zero gate voltage turn-off. With shorted gate-emitter terminals, the IGBT will withstand the highest dV/dt another similar IGBT can produce in the circuit, without latching or partial turn-on. A common misconception is

identifying the current 'blip' due to charging the output capacitance (C_{oes}) of the IGBT as conduction current. The amplitude of the current 'blip' is approximately 5A for a IRGPC50F IGBT at a dV/dt of 20V/ns. The amplitude of the 'blip' does not change with the applied negative bias.

The following test was conducted to determine the threshold voltage and the effect of the series gate resistance in high dV/dt applications. The test circuit is shown in Figure 1. The positive bias to the upper IGBT was increased until the switching losses in the bottom IGBT indicated excessive shoot-through current. The turn-on loss was measured at 15A inductor current and 6V/ns switching speed. The results are shown in Figure 2. The threshold voltage levels increasing the turn-on losses are 4V, 5V and 5.6V with 47 Ω , 10 Ω , and 0 Ω series gate resistance, respectively. A parallel diode across the series gate resistor (anode toward the gate) helps clamp the gate low, so the series gate resistor can be sized according to the turn-on requirements.

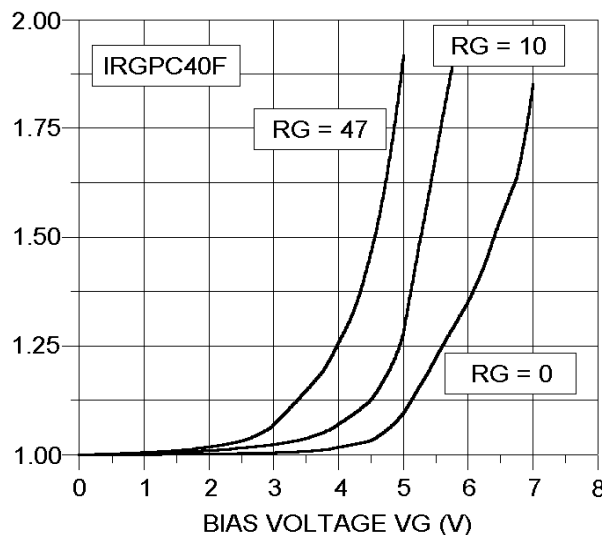


Figure 2
Normalized Turn-On Losses vs. V_G

BUFFER AND NEGATIVE CHARGE PUMP
DRIVING LARGE FLOATING LOADS

The basic buffer circuit and the negative charge pump are shown in Figure 3. The buffer circuit employs two P-channel and two N-channel MOSFETs. Resistor R1 between the gates of Q3 and Q4 slows down the turn-on of the output transistor and limits the shoot-through current in the drivers. D1 reduces the voltage to the gate of Q3 and Q4. D2, C2 and R2 form a level shifter for Q2. C3, C4, D3 and D4 convert the incoming signal to negative DC voltage. After turn-on, the negative voltage settles in a few cycles even at extremely low or high duty cycles (1 - 99%). The settling time and the stiffness of the negative voltage are affected by the output impedance of the signal source.

The circuit is shown in Figure 4 utilizes the high voltage level shifting capability of the IR2110 and the drive capability of the MOS buffer shown in Figure 3. It also generates negative voltage for turn-off. The circuit was tested with an IGBT module part number IRGSI270F06 capable of 270A connected to each output. The gate total charge for the module is 600 nC. The waveforms are shown in Figure 5. The turn-on delay of the circuit is 1 μ s, the turn-off delay is 0.2 μ s. The settling time of the negative bias voltage is about 10 ms at 5 kHz switching frequency at 50% duty cycle. At start-up, the circuit delivers some negative gate voltage even after the first cycle. During power down, the gate voltage remains negative until the reservoir capacitor discharges.

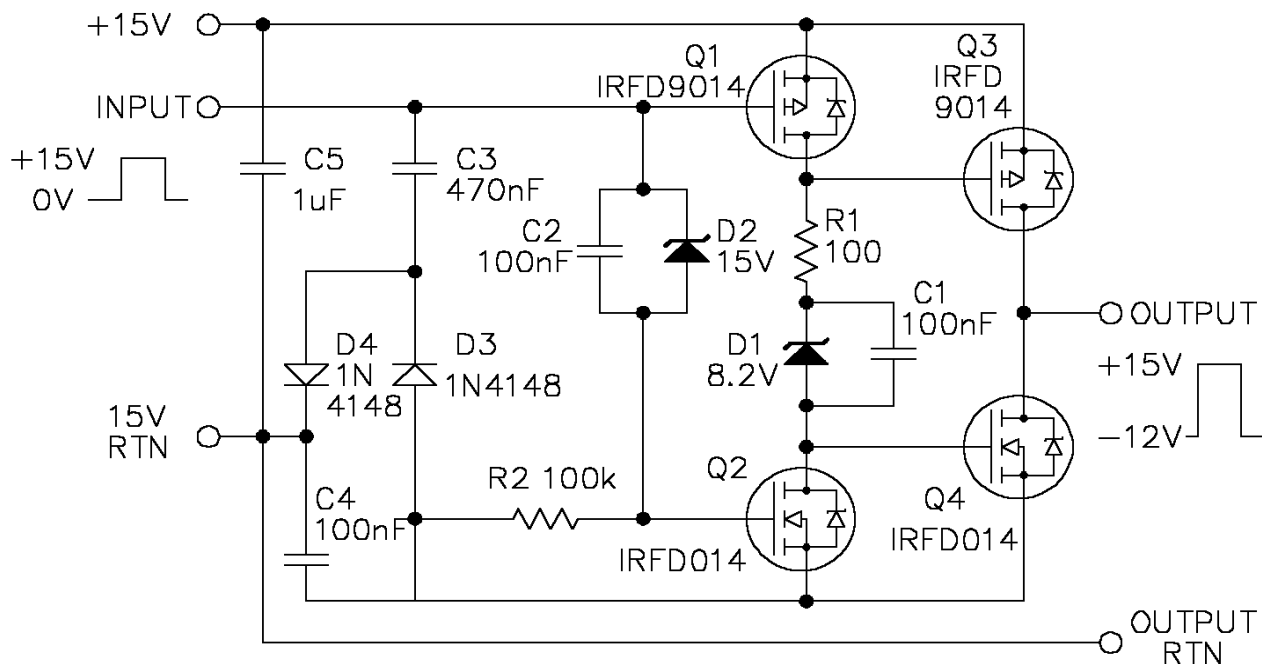


Figure 3
Buffer With Negative Charge Pump

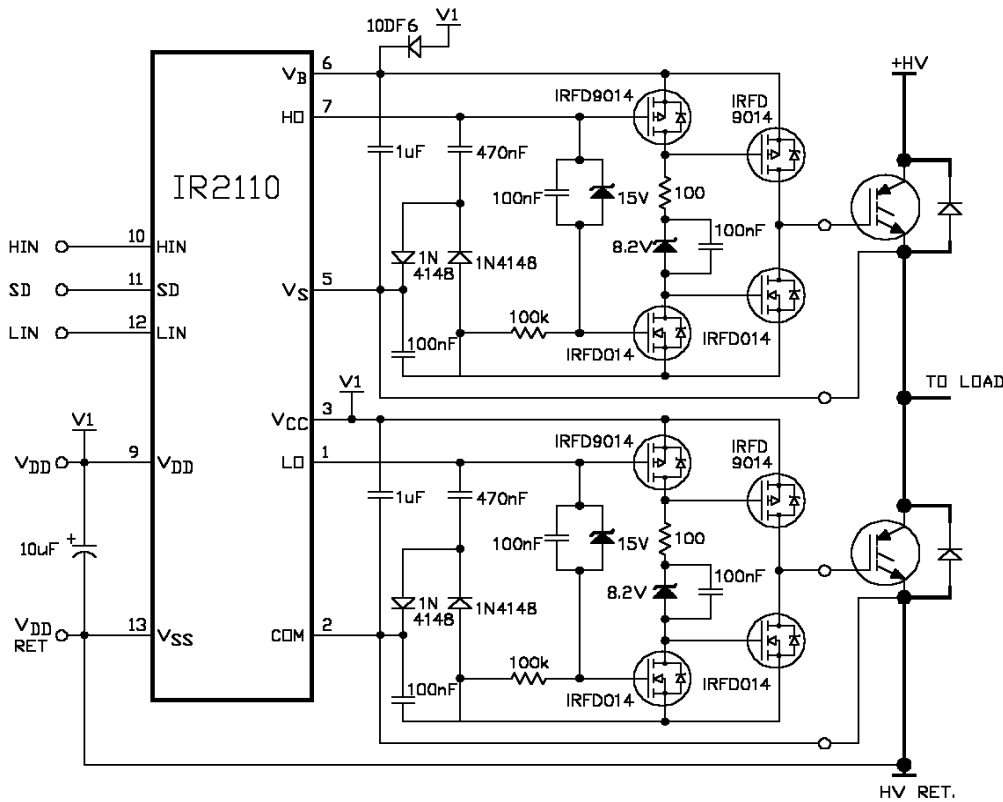


Figure 4
Half-Bridge Drive That Generates Negative Bias

A Simple Control IC with Negative Bias

Though the circuit evolution process usually results in more complication and less reliability, our circuit evolved in a different manner. The buffer and negative charge pump were removed, and the circuit became very simple as shown in Figure 6. Input and output waveforms are shown in Figure 7. The negative voltage is provided by an external power supply, while the negative bias voltage for the high-side is generated by a 100k resistor and a zener diode. The negative gate voltages are limited to the maximum applicable offset voltage between the $V_{SS} - COM$ and $V_{SS} - V_S$ leads. The total power supply voltage to the IR2110 cannot exceed 20V. The 100k resistor is sufficient for $HV = 160V$, 50% duty cycle operation. Different operating conditions may require different resistor values. The average current through the resistor should be at least 1 mA. The power

handling capability and maximum operating voltage of the resistor also have to be considered. Since the operating current of the zener diode is small, the special low current ones are preferable in this application.

CONCLUSION

Both discrete and IGBT modules made by International Rectifier do not require negative bias for proper operation. The Control ICs can be used with minimal amount of external components. However, there are IGBT manufacturers specifying negative bias on their products, and the noise margin can also be improved by applying negative bias to the gate during the off state. The circuit in Figure 4 was intended for high power IGBT module drive applications. The circuit shown in Figure 6 is an economical solution for medium power IGBT applications.

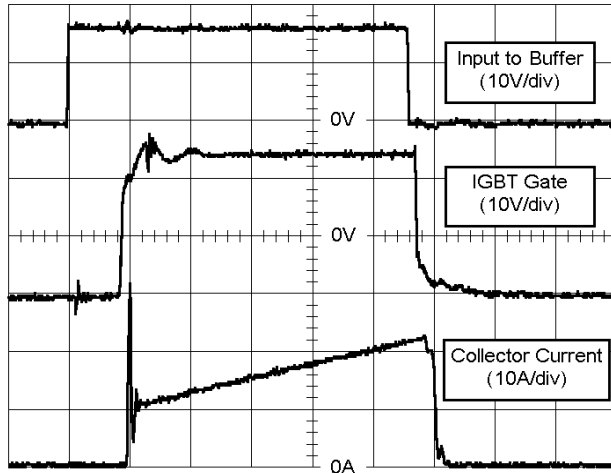


Figure 5
Waveforms From Negative Bias Half-Bridge Driver
(1 μ s/div)

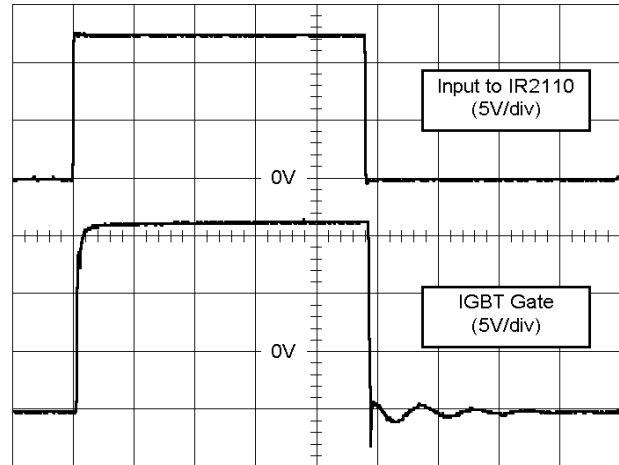


Figure 7
Waveforms From Circuit in Figure 6
(2 μ s/div)

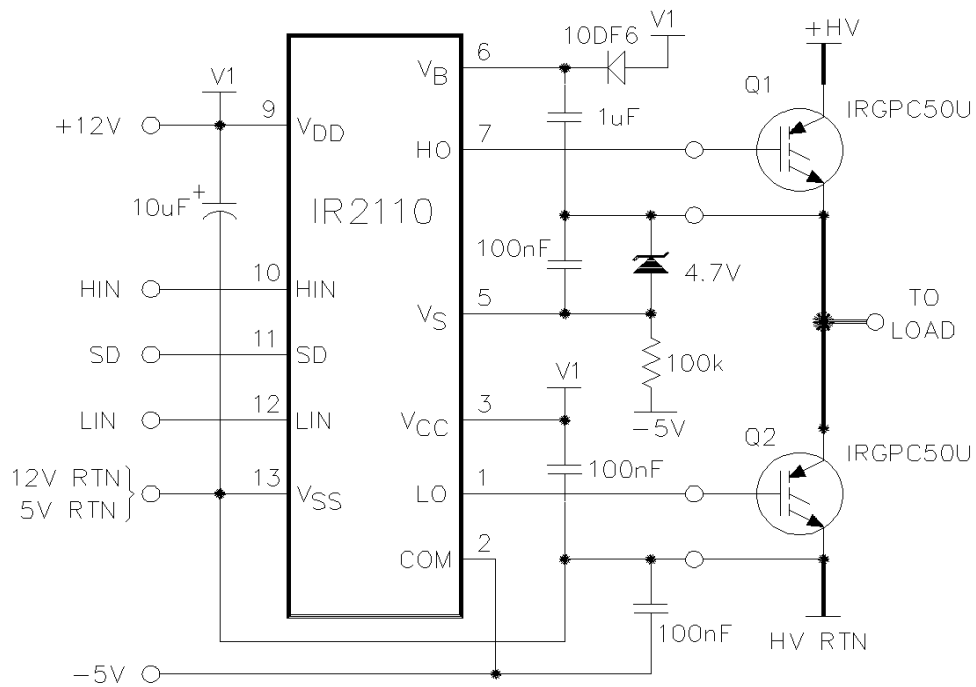


Figure 6
Half-Bridge Driver With External Negative Bias