

Characteristics of HEXFET Gen III Die

(HEXFET is the registered trademark for International Rectifier Power MOSFETs)

Introduction

This application note describes the HEXFET Power MOSFETs in the HEXFET III family available from International Rectifier in die form. These power MOS field effect transistor die feature the same high reliability planar technology used for the IRF series of packaged HEXFETs. The same advanced MOS processing techniques, silicon gate structure, and efficient hexagonal source pattern are available in die form for hybrid assembly. Use of a silicon-gate design and state-of-the-art MOS processing techniques result in an extremely reliable device which is highly reproducible in various die sizes. Hybrid packaging of such die results in substantial savings in weight and volume compared to standard packaging.

HEXFET III

The evolution of the HEXFET has given rise to three HEXFET families, each based on a distinct die design philosophy. The HEXFET III process is distinguished by increased avalanche capability, a diode-recovery dv/dt rating, an increase in maximum allowable die temperature for devices of 100V and below, and a number of other significant technological advances. Full details of these improvements are given in Application Note AN-966 (Reference 1).

HEXFET III devices have electrical characteristics that are equal or superior to their HEXFET I and HEXFET II counterparts so that they are able to use the same part numbers. Data sheets referring to HEXFET III devices are identified as such on the front page and packaged devices are marked in a way which identifies them as HEXFET III devices (See AN-966 for full details.)

Table I lists HEXFET III wafer probe values while Figures 1 through 38 show the die dimensions. Table II explains the nomenclature code.

HEXSense™

International Rectifier has a family of HEXFETs incorporating current sensing. This is the HEXSense family of devices, based on the HEXFET III process. They are available in the usual voltage and current ranges and may therefore be used in place of conventional HEXFETs. Current sensing is achieved by isolating a few of the HEXFET cells from the main source metallization and providing them with a separate bonding pad. The drain current divides between the sense cells and the main body of cells in a manner determined by the ratio of the number of sense cells to the total number of cells on the die. Since the ratio which the current divides is known, the drain current can be determined by measuring only the sense current. As the sense current is in the order of a few milliamps, the value of the drain current can be determined without incurring significant power losses.

The HEXSense die has two extra bonding pads, besides the gate and source pads. These are the current sense pad and the Kelvin-source pad. The current sense pad is connected to the sensing cells. The Kelvin-source pad connects to the main source metallization and is used as a return path for the sense current. A separate return path for the sense current is required to prevent voltage drops due to parasitic resistance in the main source path being included in the sense current path.

Details of the HEXSense family are included in Table I.

Table I. HEXFET III Die

HEX Size	Part Number	VDS	RDS(on) Max.	Figure	Recomm. Source Bonding Wire		Data Sheet
					mils	mm	
Z	IRFC1Z0	100	2.400	1	3	0.08	PD-9.438
1	IRFC014	60	0.200	2	5	0.13	PD-9.507
1	IRFC110	100	0.540	3	5	0.13	PD-9.325
1	IRFC210	200	1.500	4	5	0.13	PD-9.326
1	IRFC214	250	2.000	4	5	0.13	PD-9.475
1	IRFC310	400	3.600	5	5	0.13	PD-9.327
2	IRFC024	60	0.100	6	10	0.25	PD-9.594
2	IRFC120	100	0.270	8	8	0.20	PD-9.313
2	IRFC220	200	0.800	9	8	0.20	PD-9.317
2	IRFC224	250	1.100	9	8	0.20	PD-9.472
2	IRFC320	400	1.800	10	8	0.20	PD-9.315
2	IRFC420	500	3.000	10	8	0.20	PD-9.324
2	IRFCC20	600	4.400	10	8	0.20	PD-9.623
2	IRFCE20	800	6.500	11	5	0.13	PD-9.610
2	IRFCF20	900	8.000	11	5	0.13	PD-9.607
2	IRFCG20	1000	11.500	11	5	0.13	PD-9.604
3	IRFC034	60	0.050	12	15	0.38	PD-9.509
3	IRFC130	100	0.160	14	10	0.25	PD-9.307
3	IRFC230	200	0.400	16	8	0.20	PD-9.309
3	IRFC234	250	0.450	16	8	0.20	PD-9.476
3	IRFC330	400	1.000	17	8	0.20	PD-9.308
3	IRFC430	500	1.500	17	8	0.20	PD-9.311
3	IRFCC30	600	2.200	17	8	0.20	PD-9.482
3	IRFCE30	800	3.200	18	10	0.25	PD-9.613
3	IRFCF30	900	4.000	18	10	0.25	PD-9.616
3	IRFCG30	1000	5.600	18	10	0.25	PD-9.620
4	IRFC044	60	0.028	19	20	0.51	PD-9.510
4	IRFC140	100	0.077	21	15	0.38	PD-9.373
4	IRFC240	200	0.180	23	15	0.38	PD-9.374
4	IRFC244	250	0.280	23	15	0.38	PD-9.527
4	IRFC340	400	0.550	24	12	0.30	PD-9.375
4	IRFC440	500	0.850	24	12	0.30	PD-9.376
4.5	IRFC448	500	0.600	25	12	0.30	PD-9.595
4	IRFCC40	600	1.200	24	12	0.30	PD-9.506
4	IRFCE40	800	2.000	26	10	0.25	PD-9.578
4	IRFCF40	900	2.500	26	10	0.25	PD-9.580
4	IRFCG40	1000	3.500	26	10	0.25	PD-9.576
5	IRFC054	60	0.014	27	25	0.64	PD-9.544
5	IRFC150	100	0.055	29	20	0.51	PD-9.441
5	IRFC250	200	0.085	29	20	0.51	PD-9.443
5	IRFC254	250	0.140	29	20	0.51	PD-9.540
5	IRFC350	400	0.300	31	20	0.51	PD-9.445
5	IRFC450	500	0.400	31	20	0.51	PD-9.458
5	IRFCC50	600	0.600	31	20	0.51	PD-9.656
5	IRFCE50	800	1.200	32	10	0.25	PD-9.573
5	IRFCF50	900	1.600	32	10	0.25	PD-9.542
5	IRFCG50	1000	2.000	32	10	0.25	PD-9.543
6	IRFC260	200	(.060)	33	25	0.64	—
6	IRFC360	400	0.200	33	25	0.64	PD-9.518
6	IRFC460	500	0.270	33	25	0.64	PD-9.465

Table I. HEXFET III Die (Continued)

HEX Size	Part Number	VDS	RDS(on) Max.	Figure	Recomm. Source Bonding Wire		Data Sheet
					mils	mm	
P-CHANNEL HEXFETs							
1	IRFC9014	-60	0.500	2	5	0.13	PD-9.654
1	IRFC9110	-100	1.200	34	5	0.13	PD-9.390
1	IRFC9210*	-200	3.000	35	5	0.13	PD-9.350
2	IRFC9024	-60	0.280	6	10	0.25	PD-9.647
2	IRFC9120	-100	0.600	36	8	0.20	PD-9.319
2	IRFC9220*	-200	1.500	37	8	0.20	PD-9.351
3	IRFC9034	-60	0.140	12	12	0.30	PD-9.648
3	IRFC9130	-100	0.300	38	10	0.25	PD-9.320
3	IRFC9230	-200	0.800	16	8	0.20	PD-9.352
4	IRFC9044	-60	—	19	20	0.51	—
4	IRFC9140	-100	0.200	21	15	0.38	PD-9.421
4	IRFC9240	-200	0.500	23	15	0.38	PD-9.422
LOGIC LEVEL DIE							
1	IRLC014	60	0.200	2	5	0.13	PD-9.556
1	IRLC110	100	0.540	3	5	0.13	PD-9.560
2	IRLC024	60	0.100	6	10	0.25	PD-9.557
2	IRLC120	100	0.270	8	8	0.20	PD-9.561
3	IRLC034	60	0.050	12	15	0.38	PD-9.558
3	IRLC130	100	0.160	14	10	0.25	PD-9.562
4	IRLC044	60	0.028	19	20	0.51	PD-9.559
4	IRLC140	100	0.077	21	15	0.38	PD-9.563

HEX Size	Part Number	VDS	RDS(on) Max.	Nominal Sense Ratio	Figure	Recomm. Source Bonding Wire		Data Sheet
						mils	mm	
HEXSense DIE								
2	IRCC024	60	0.100	780	7	10	0.25	PD-9.615
3	IRCC034	60	0.050	1410	13	15	0.38	PD-9.590
3	IRCC130	100	0.160	1430	15	10	0.25	PD-9.454
3	IRCC230	200	0.400	1490	15	8	0.20	PD-9.565
3	IRCC234	250	0.450	1490	15	8	0.20	PD-9.566
3	IRCC330	400	1.000	1525	15	8	0.20	PD-9.567
3	IRCC430	500	1.500	1520	15	8	0.20	PD-9.455
4	IRCC044	60	0.028	2590	20	20	0.51	PD-9.529
4	IRCC140	100	0.077	2680	22	15	0.38	PD-9.592
4	IRCC240	200	0.180	2740	22	15	0.38	PD-9.568
4	IRCC244	250	0.280	2770	22	15	0.38	PD-9.569
4	IRCC340	400	0.550	2800	22	12	0.30	PD-9.570
4	IRCC440	500	0.850	2780	22	12	0.30	PD-9.593
5	IRCC054	60	0.014	2200	28	25	0.64	—
5	IRCC150	100	0.055	(5440)	30	20	0.51	—
5	IRCC250	200	0.085	(5680)	30	20	0.51	—
5	IRCC254	250	0.140	(5440)	30	20	0.51	—
5	IRCC350	400	0.300	(5440)	30	20	0.51	—
5	IRCC450	500	0.400	(5440)	30	20	0.51	—

*GEN I design

Numbers in parenthesis are preliminary.

For more detailed information, please refer to the most current data sheet.

Common characteristics:

$I_{DSS} @ V_{DS}$: 250 μA

I_{GSS} : 500 nA

$V_{GS(th)}$: Standard HEXFETs min 2V, max 4V with $V_{DS} = V_{GS}$, $I_D = 250 \mu A$

$V_{GS(th)}$: Logic level HEXFETs min 1V, max 2V with $V_{DS} = V_{GS}$, $I_D = 250 \mu A$

$R_{DS(on)}$: Measured with $V_{GS} = 10V$ on standard HEXFETs and 5V on logic level HEXFETs

Recommended wire size for Gate, Kelvin and Current Sense Connections: 3 to 5 mils (0.076 to 0.127 mm)

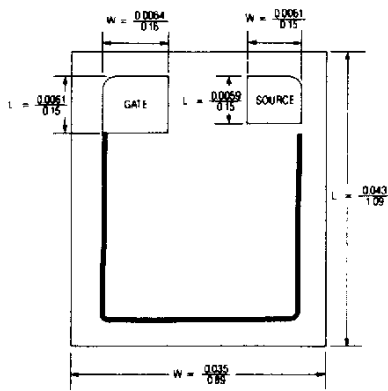


Figure 1. HEX-Z: 100V, N-Channel

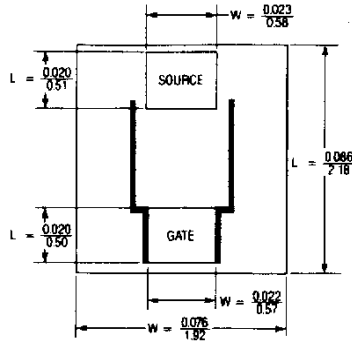


Figure 2. HEX-1: 60V, N- and P-Channel

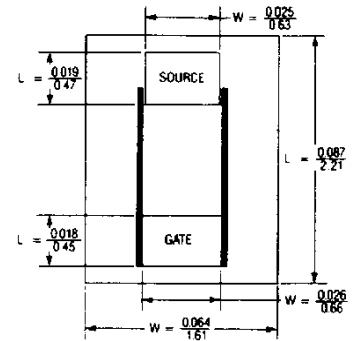


Figure 3. HEX-1: 100V, N-Channel

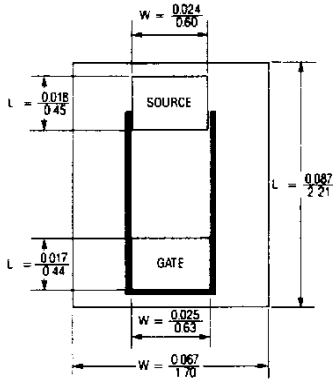


Figure 4. HEX-1: 200V & 250V, N-Channel

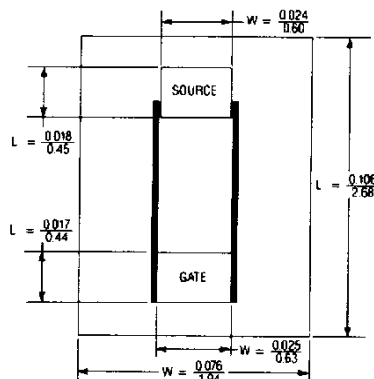


Figure 5. HEX-1: 400V, N-Channel

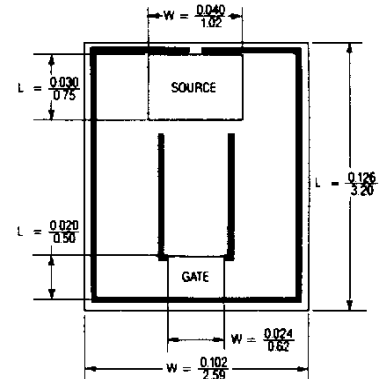


Figure 6. HEX-2: 60V, N- and P-Channel

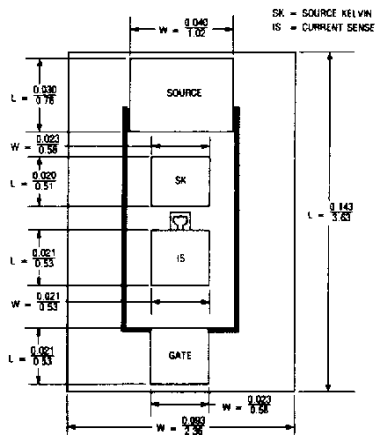


Figure 7. HEXSense-2: 60V, N-Channel

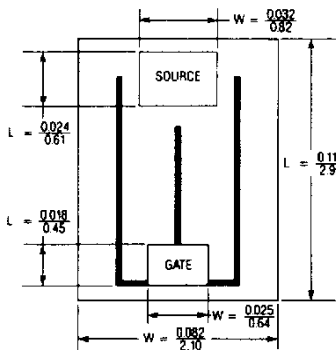


Figure 8. HEX-2: 100V, N-Channel

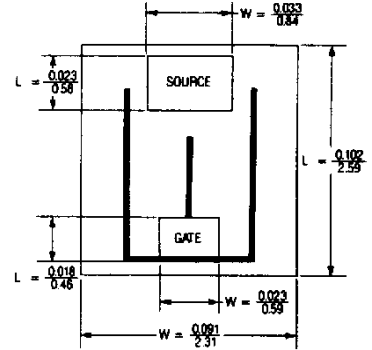


Figure 9. HEX-2: 200V & 250V, N-Channel

All dimensions shown in inches/mm
Die dimensions are from centerline to centerline of scribe alleys

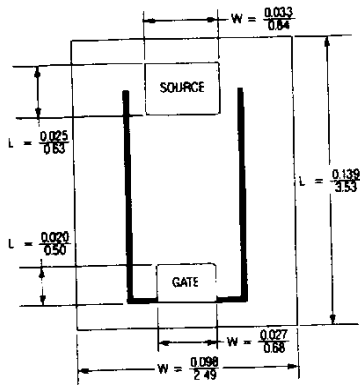


Figure 10. HEX-2: 400V, 500V, & 600V, N-Channel

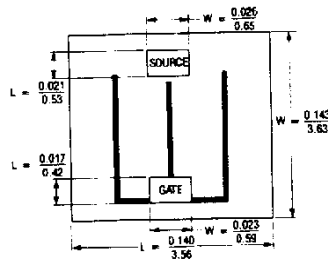


Figure 11. HEX-2: 800V, 900V, & 1000V, N-Channel

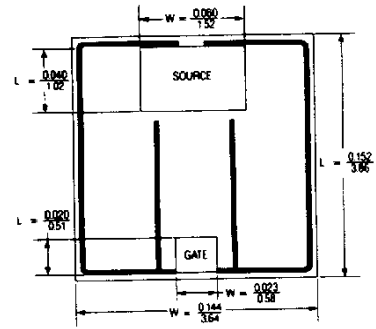


Figure 12. HEX-3: 60V, N- and P-Channel

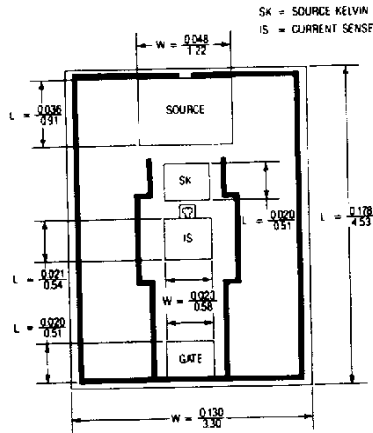


Figure 13. HEXSense-3: 60V, N-Channel

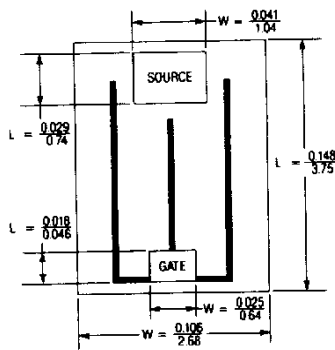


Figure 14. HEX-3: 100V, N-Channel

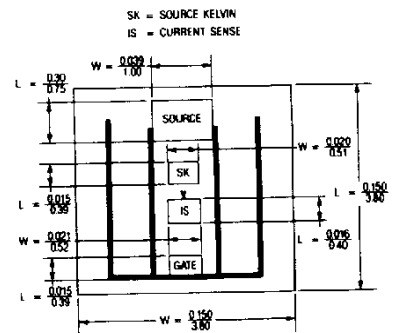


Figure 15. HEXSense-3: 100V to 500V, N-Channel

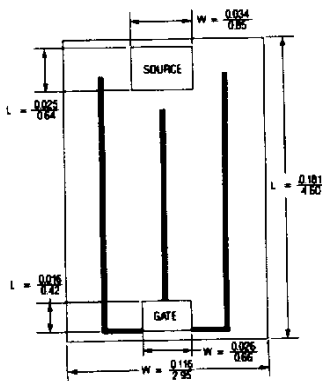


Figure 16. HEX-3: 200V & 250V, N- and P-Channel

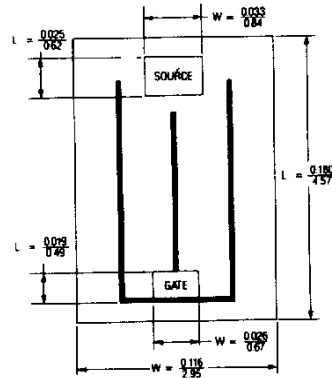


Figure 17. HEX-3: 400V, 500V, & 600V, N-Channel

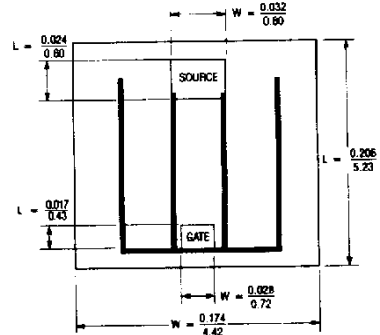


Figure 18. HEX-3: 800V, 900V, & 1000V, N-Channel

All dimensions shown in inches/mm
Die dimensions are from centerline to centerline of scribe alleys

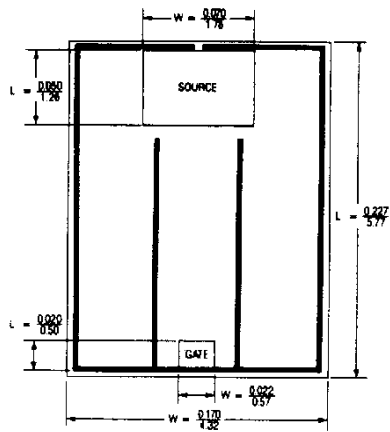


Figure 19. HEX-4: 60V, N- and P-Channel

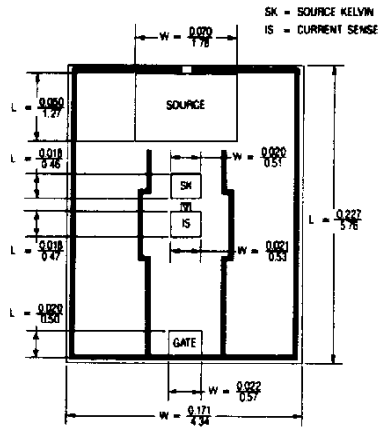


Figure 20. HEX-4: 60V, N-Channel

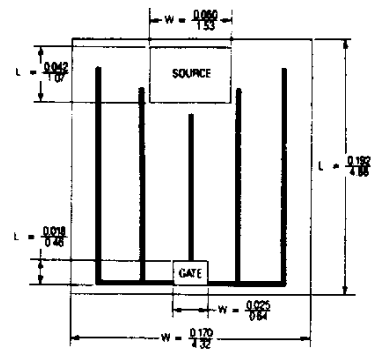


Figure 21. HEX-4: 100V, N- and P-Channel

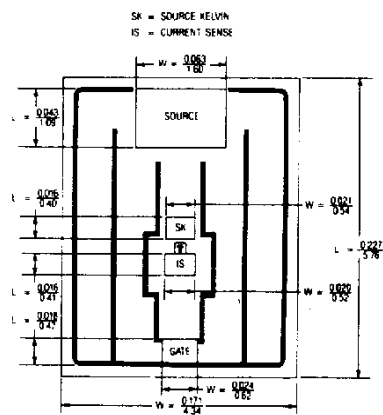


Figure 22. HEX-4: 100V to 500V, N-Channel

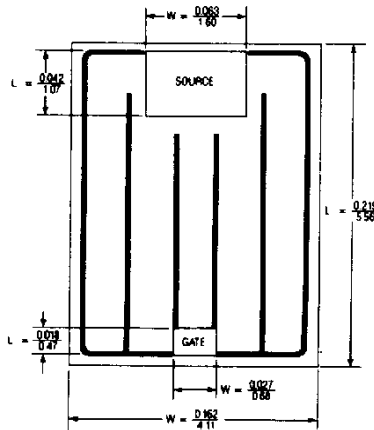


Figure 23. HEX-4: 200V & 250V, N- and P-Channel

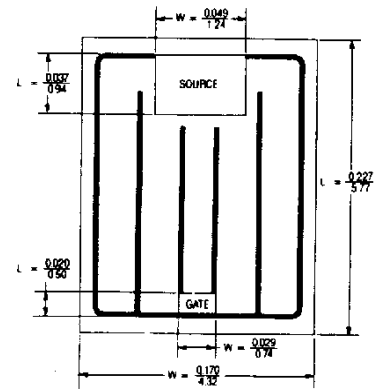


Figure 24. HEX-4: 400V, 500V, & 600V, N-Channel

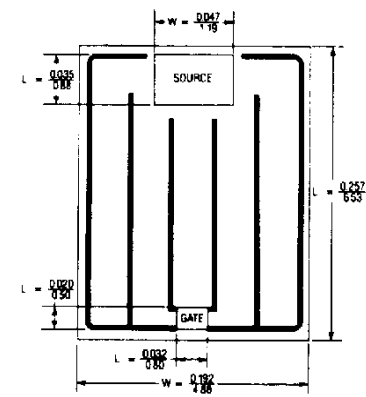


Figure 25. HEX-4.5: 500V, N-Channel

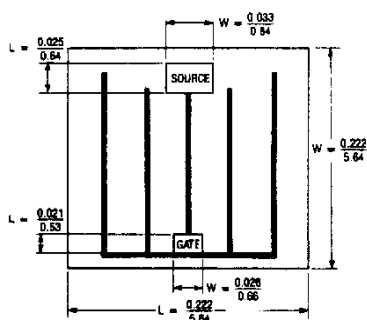


Figure 26. HEX-4: 800V, 900V, & 1000V, N-Channel

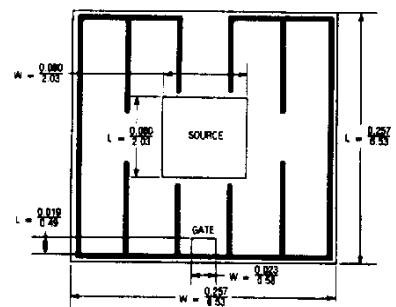


Figure 27. HEX-5: 60V, N-Channel

All dimensions shown in inches/mm
Die dimensions are from centerline to centerline of scribe alleys

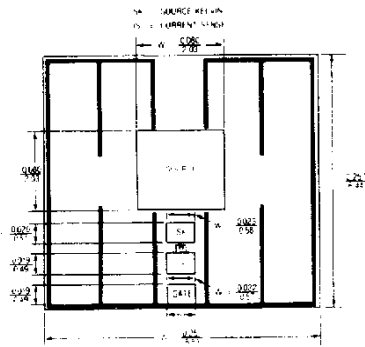


Figure 28. HEXSense-5: 60V, N-Channel

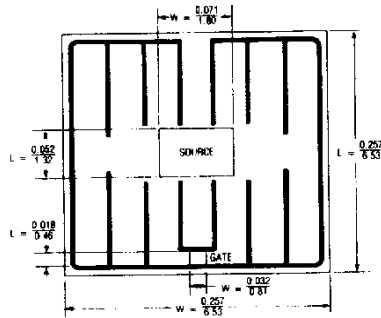


Figure 29. HEX-5: 100V, 200V, & 250V, N-Channel

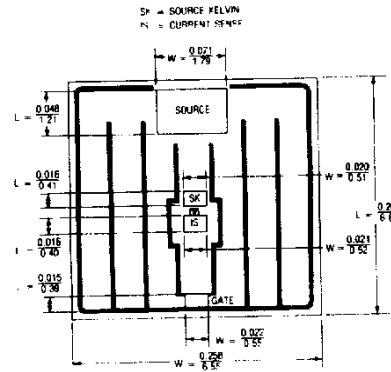


Figure 30. HEXSense-5: 100V to 500V, N-Channel

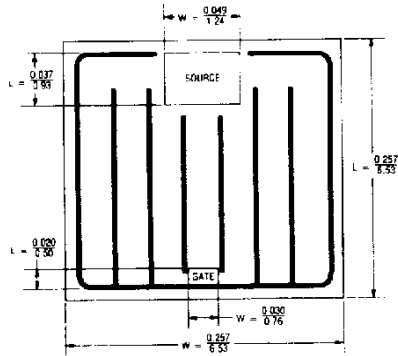


Figure 31. HEX-5: 400V, 500V, & 600V, N-Channel

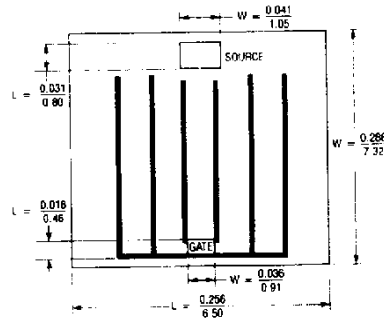


Figure 32. HEX-5: 800V, 900V, & 1000V, N-Channel

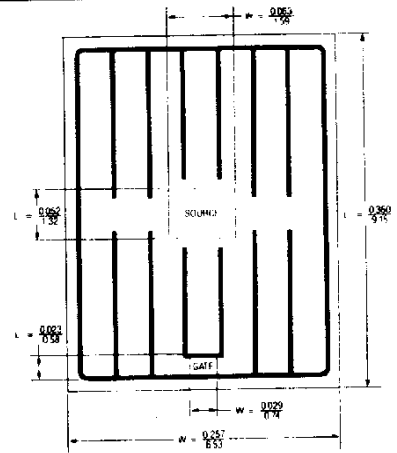


Figure 33. HEX-6: 200V, 400V & 500V, N-Channel

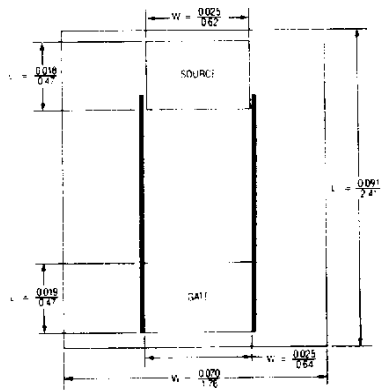


Figure 34. HEX-1: -100V, P-Channel

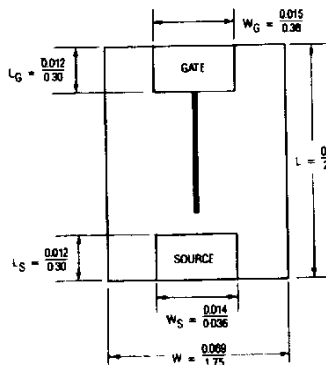


Figure 35. HEX-1: -200V, P-Channel Gen I

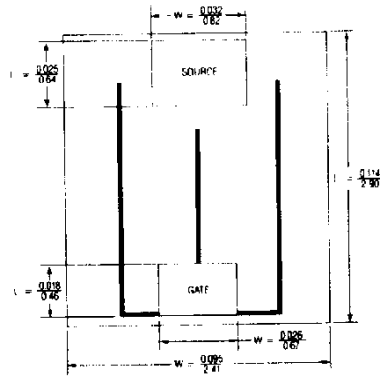


Figure 36. HEX-2: -100V, P-Channel

All dimensions shown in inches/mm
Die dimensions are from centerline to centerline of scribe alleys

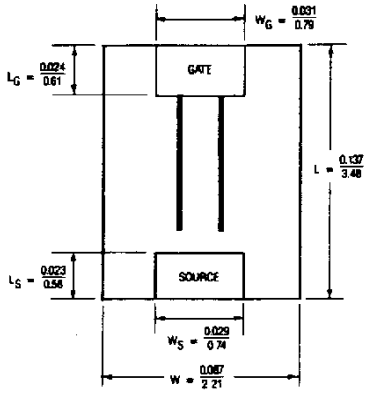


Figure 37. HEX-2: -200V,
P-Channel Gen I

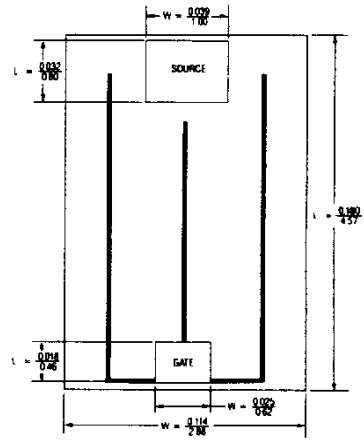


Figure 38. HEX-3: -100V,
P-Channel

All dimensions shown in inches/mm
Die dimensions are from centerline to centerline of scribe alleys

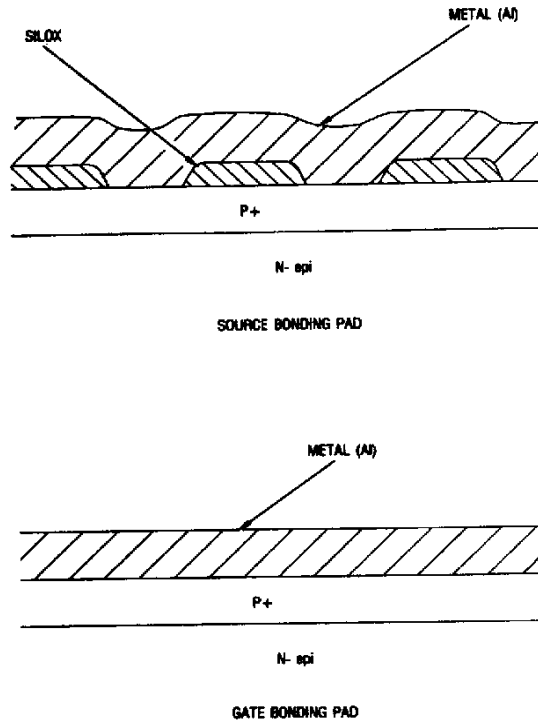


Figure 39. Cross Section of Source and Gate Bonding Pads

Chip Tray Capacity by Die Size

HEXFET DIE	HEX-Z	HEX-1	HEX-2	HEX-3	HEX-4	HEX-5	HEX-6
Chip Tray Capacity	400	140	96	45	35	16	15

Please note that chips are only sold in multiples of the trays shown above.

Dimensional Tolerances

Bonding Pad L or W:

<0.025 in., Tolerance = ± 0.0005 in.
 >0.025 in., Tolerance = ± 0.001 in.

Overall Die L or W:

<0.050 in., Tolerance = ± 0.004 in.
 >0.050 in., Tolerance = ± 0.008 in.

Die Thickness: Ranges from 15.5 mils ± 1 for 60V devices to 19 mils ± 1 for 1000V devices.

Logic Level HEXFETs

A family of third generation logic level HEXFETs rated at 60 and 100V with guaranteed on-resistance at gate voltages of 4 and 5V is also listed in Table I. With the exception of drive requirements and gate threshold, these devices are identical to their standard counterparts.

Electrical Characteristics

Each HEXFET die is individually probed at ambient temperature to the electrical specifications shown in Table I.

Because of electrical limitations when electrically probing in wafer form, some of the generic specifications of the equivalent packaged device cannot be tested and guaranteed in die form. These are power dissipation (P_d), safe operating area (SOA), thermal resistance ($R_{th(jc)}$), on-resistance at rated current ($R_{ds(on)}$), inductive current (ILM) and unclamped inductive current (IL). These parameters are dependent upon the user's assembly technique. On-resistance at $I_D = 1A$ is tested and guaranteed according to Table I. However, the following characteristics are guaranteed by design to meet the specifications of the equivalent part: g_{fs} , Q_g , Q_{gs} , Q_{gd} , dv/dt and T_{Jmax} . For these values consult the appropriate data sheet listed in Table I.

Following electrical probing, the die are inked for identification and scribed. The die are mechanically separated, and packed for shipment.

Handling and Shipping

HEXFET die from International Rectifier are shipped in anti-static chip trays and sealed electrostatic shielding bags for protection during shipment. Once opened, the die must be stored in a dry, inert atmosphere, such as nitrogen, prior to assembly. Die should be handled with DuPont Teflon-tipped vacuum pencils to prevent mechanical damage. Any non-conformance to the electrical or visual inspection specifications in this brochure must be reported in writing to International Rectifier within 30 days after shipment of the lot by International Rectifier. International Rectifier assumes no responsibilities for die which have been subjected to further processing such as mount-down, wire bonding, or encapsulation. In the interest of product improvement, the right is reserved to make design or processing changes without notification.

The anti-static chip trays are designed to avoid the build-up of static charge. ESD control procedures should be observed during handling and assembly to prevent exceeding the 20V maximum gate-source voltage, as indicated in References 2 and 3. The chip tray capacities are shown on the appropriate page of drawings.

Visual Inspection of Die

International Rectifier HEXFET die are designed to meet the visual inspection criteria of Mil-Standard 750C, Method 2072. HEXFET die are visually screened to a 1.0% AQL level.

Die Mounting

The HEXFET die have a chromium-nickel-silver drain metallization which is suitable for solder preform mounting using solders such as 95/5 PbSn or 92.5/2.5/5 PbAgIn solder.

Gold backing may be available as an alternate possibility. Please contact the factory or an IR representative for more information.

Any of the commonly used header or substrate materials such as copper, nickel-plated copper, and gold-plated molybdenum, beryllia, and alumina are acceptable. The substrate must be freed of oxides prior to assembly either by chemical cleaning or hydrogen pre-firing techniques. The HEXFET die should be cleaned prior to mount-down in deionized water cascade (one minute) followed by isopropyl alcohol agitated bath (twice, one minute each) and then 70°C nitrogen chamber drying. Mounting is generally accomplished in a profiled belt furnace. The furnace zone settings will depend upon hybrid mass density, jiggling, and belt speed. The HEXFET die temperature must not exceed 400°C, nor be in the range of 350 to 400°C for greater than one minute. A clean furnace of hydrogen atmosphere is recommended, although an atmosphere of nitrogen or forming gas (nitrogen-hydrogen, 85% – 15%) is acceptable.

A variety of conductive plastics have been utilized as alternate means of bonding the HEXFET die to a variety of substrates.

Wire Bonding

Electrical connection to the gate and source aluminum bonding pads is by ultrasonic bonding with Al wire having an elongation of 10%. The recommended wire diameters are given in Table I. Caution must be exercised during wire bonding to ensure that the bonding footprint remains within the bonding pad area; otherwise, device failure can result. Likewise, wire bonding equipment settings should be optimized and a wire pull test performed (e.g., see Method 2037, Mil-Standard 750C) to monitor wire bond strength uniformity. Destructive sample testing and 100% non-destructive testing is recommended. Rebonding of wire bond rejects can be performed although decreased yield can be expected from such reworks. Using process controls as described above, final assembly yields of 80% to 95% can be achieved. In devices rated at 60V, the source is bonded to active area. Figure 39 shows the cross section at the bonding pads for a standard device.

Encapsulation

Prior to encapsulation, the die or assembly must be kept in a moisture-free environment, since I_{gss} and I_{dss} particularly are sensitive to surface moisture. If the final package is non-hermetic, a high grade semiconductor coating may be applied. Cleaning of the die in a degreaser prior to coating is recommended. Immediately prior to encapsulation, a 150°C, two-hour bake should be performed to remove any surface moisture. Capping of hermetic packages should be performed in a dry-nitrogen atmosphere.

References

- (1) International Rectifier Application Note AN-966. "HEXFET III — A new Generation of Power MOSFETs."

Conclusion

The use of power MOSFET die for hybrid assemblies can result in significant reduction in overall package size. In addition, the high gain characteristics of the HEXFET can allow further miniaturization by eliminating complex drive circuitry. Several HEXFET die can readily be mounted on the same heatsink to form circuit configurations or to parallel devices. The HEXFET operational advantages, thereby, can be realized in very compact, custom package configurations. □

- (2) International Rectifier Application Note AN-955. "Protecting Power MOSFETs from ESD."
- (3) International Rectifier Application Note AN-986. "ESD Testing of MOS-Gated Power Transistors."

Table II. Nomenclature Code for HEXFET Die

