Design Considerations for using IGBT modules in Inverters and Drives

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Introduction

This work is designed to assist the IGBT module selection process as well as offer guidance through the inverter/motor drive design and evaluation process. To build a successful inverter or drive requires an understanding of not only the power switches, but that of the load, line, associated transients, switching frequencies and power loss budget. With these as the cornerstones or top level concerns, there is a clear need to understand the parasitic interactions of the IGBT module with the bus and the load and the actual losses beyond the theoretical calculations. This is a practical guide that will go through device selection, measurement techniques, loss calculations and measurements, gate drive and related design issues.

1.) Module construction

Why not just go discrete?

The fact of the matter is that the module is a smaller solution than a comparably rated discrete solution with the individual IGBTs and copack diodes. The dielectric gel filling allows for closer spacing between high voltage differences, like perhaps the top and bottom switches in a half bridge. The closer spacing gives rise to much lower interconnect inductances between the die compared to what would be buss bars—a clear advantage in terms of switching losses. The module allows the use of a Direct Bond Copper (DBC) substrate. The dies are attached to the DBC and the die connections are done with multiple bondwires of appropriate cross section. The power terminals are connected to the DBC to provide the rugged mechanical connection that is seen. The backside of the DBC is then soldered to a baseplate which is ultimately bolted to the thermal management system to provide necessary cooling. A good view of the module construction is shown below in figure 1. This depicts a half bridge module although it is easy enough to see how the DBC isolates the collectors of the IGBTs from the baseplate and how this could be expanded to full three phase inverters, with as much as a brake and a bridge rectifier integrated in one package.

Our new modules are offered in 600V and 1200V ratings to accommodate DC link voltages in the area of 300 and 700V respectively. The modules are rated for -55 degC to +125 degC case temperatures with a 150 degC maximum junction temperature. The modules are available in half bridge, triple half bridge and single device configurations in standard packages.

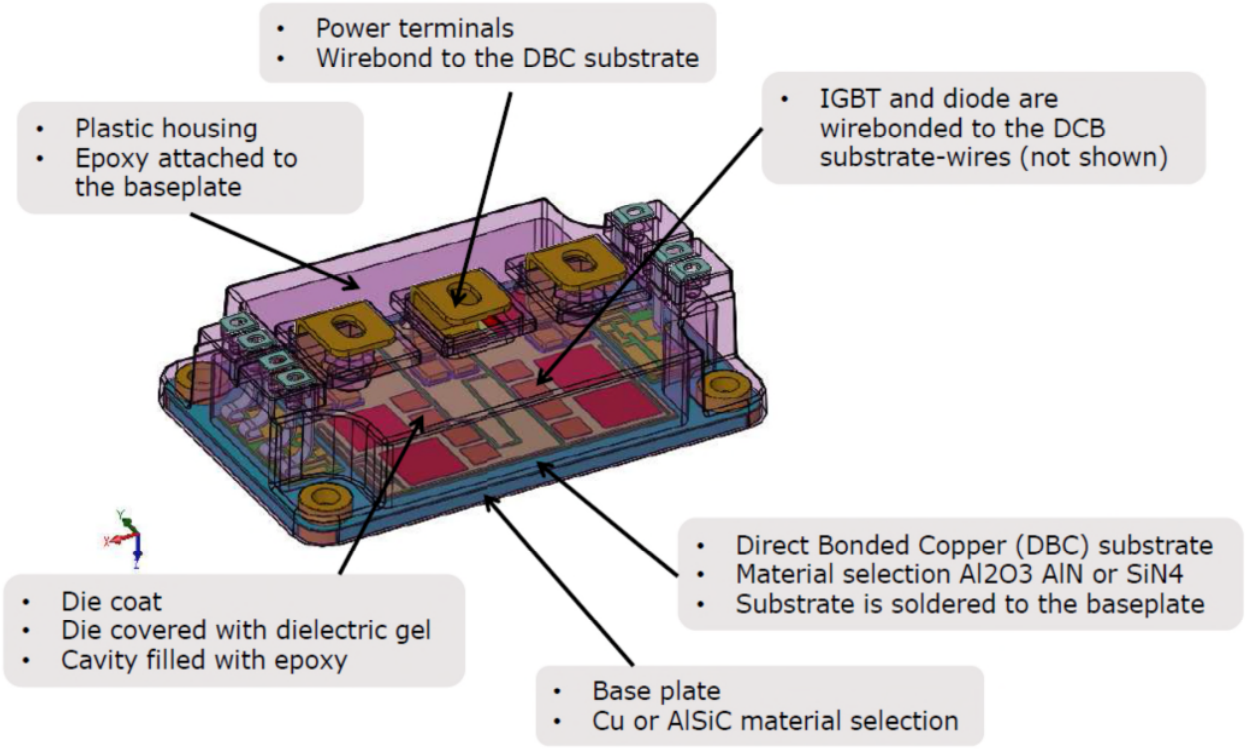

Figure 1. Module construction

2.) Device Selection

It's an age old question: Which device should I use in my application? The steps below and explanations will make the device selection process as simple as possible.

Module Selection Checklist

This preliminary information can be collected into a simple set of questions at the onset of the drive or inverter design (the headings are expanded on below):

1.) Short circuit current
2.) Short circuit timing budget
3.) Maximum phase current to the machine
4.) Maximum DC link voltage
5.) Maximum Switching frequency
6.) Maximum junction temperature
7.) Maximum ambient or boundary temperature
8.) Module Package
9.) Qualification Level

With these parameters the current rating of the IGBT can be chosen, the appropriate voltage rating, and the proper device family. Our package offering includes most standard size module packages including the 34mm, 62mm, EconoPACK2, EconoPACK3, EconoPACK4, EconoPACK+ and EconoDUAL.

Short circuit rating

Larger inverters often have lesser output filtering and may offer and IGBT half bridge output to the outside world. These applications require short circuit rated devices.

For inverters this is often not considered at all. The inverter usually has an inductor in series with the output and likely filter capacitors to AC quiet ground to filter off the high frequency switching components. This inductor limits the di/dt that the IGBT's can source from the DC link capacitors.

The inductor is internal and the user cannot bypass it at the output terminals. With this in play the 5 or 10us short circuit rating in the IGBT is not required. There is no way the end user can cause peak currents beyond what the filter inductors will allow by manipulating the outputs. The impedance of the inductor is chosen such that it is quite low at the fundamental output frequency, usually less than 1% PU and high enough to offer fairly low ripple current at the switching frequency at some given minimum load.

For motor drives, the output of the half bridge conversion stage is often directly available to the end user. It is then possible to have the end user short one of the half bridge stages to some other terminal. Perhaps the earthing terminal, another phase terminal, a DC link terminal or any of the control terminals. In these circumstances, the drive must fail safely. This often requires the short circuit current to be sensed and acted upon thereby shutting down the appropriate power switches. The sensing event takes time. The output current needs to be sensed, the motion control engine needs to respond to the overcurrent threshold, the gate drive needs to shut down the IGBT. If the turn off delay of a large IGBT is perhaps 1500ns at max temperature, with a propagation delay through the galvanically isolated gate drive circuit of 500ns worst case, with a worst case motion control engine interrupt of 2000ns and a current transducer settling time of 1us, the IGBT in the circuit must then be able to withstand a short circuit for at least 5us before shutdown can ensue. In larger drives, the short circuit interrupt event can take up to 7us or so by conventional design and motion control methodologies. In these cases, devices with a 10us short circuit withstand rating are required.

There is an alternative to this for smaller machines and applications. The inverters in these machines are often built into the end bell housing of the machine and wired directly to the stator. In this configuration it is not physically possible to have the end user short an output to anything without massive disassembly effort. In these circumstances, the short circuit withstand requirement is not required.

Maximum Current Rating and NOT Power rating

Without knowing the machine or application, it is difficult to select devices for the drive from nameplate power ratings alone. Looking at power ratings alone may lead you down a path similar to “If the machine produces a given amount of power, and the DC link voltage is known, I can then choose a device that will safely source the required current to make that power”, but this path is faulty.

The machine isn’t arbitrary. For a high saliency ratio PM machine with strong Kt and Ke the stall currents can be very high. An offroad construction vehicle may use this sort of machine into, out of and at stall conditions. This drive will have to source surprisingly large amount of current at these conditions. That current will determine the current requirement of the IGBT’s in the drive.

Squirrel cage machine’s current profiles aren’t as dramatic, however the maximum load current needs to be understood. The IGBTs in the drive are again chosen for these current levels and not the power output of the machine.

From a different vantage point it is easy to reinforce why this would be so. If the IGBT has a fairly constant Vce sat, device loss is then proportional to the current flow through the Vce sat. The device will have a thermal limit, thereby a maximum device current. The maximum machine or load current has to fall well within that limit. Whether examined from the device side of the drive or the load/machine side, the worst case current determines what size devices are required.

Consider the temperature when selecting an IGBT module

All IGBTs are specified over temperature. As a convenient point of reference, the datasheets include the maximum continuous collector current at 80 degC case temperature. This is a good starting point for choosing the right module given the maximum RMS phase current of the machine. It’s not the whole answer as switching

losses and switching frequency still need to be considered, but for initial device selection, it's a good starting point.

DC Link Voltage

As a responsible designer, designing on best effort and merits, it is necessary to understand the input source to the inverter. The input often comes from a rotating machine and rectifier stack. The DC link voltage then varies as shaft speed and Ke of the source machine.

But this may not be universally true. Given the changing landscape of power systems and the drive to make them more efficient, it is entirely possible that the DC link to the inverter being designed may be the output of a PFC preregulator. A preregulator forces sinusoidal phase currents in phase with the phase voltages thereby improving the power factor seen by the input source. This may afford added stability, however the limits of the preregulator need to be understood. In a boost type circuit, when the input rises above the output and the control shuts down the converter, the DC link voltage will rise due to the freewheel diode being forward biased and the overvoltage will be passed on to the DC link.

For example, if the DC link voltage is coming from an APU or turbine, driving a PM machine the overspeed condition is directly tied to DC link voltage. If the turbine can double shaft speed from nominal, the dc link can double proportionally assuming the stator isn't in saturation. There are a lot of techniques to limit this including using brushless field control and pilot rotor/stators in place of the PM machines. These machines offer the ability to fold back the main field current proportional to overspeed and directly control the Ke and thereby DC link voltage. But this is not a fast control methodology. The fold back event is proportional to the time that it takes the main rotor pole flux to change. This can be a several hundred millisecond event due to the retentivity of the pole metal. In the automotive arena, this is called load dump induced overvoltage. It is directly caused by open circuiting the positive terminal of the battery and having the alternator sense the open circuit and fold back rotor current. Even if the foldback event is fast, the claw poles in the rotor are quite well magnetized and their retentivity takes time to drop to the lesser DC flux value. Typical load dump event is slightly less than 200ms. There is no common term for this in mil vehicles or aviation, but it is captured in various standards including DO160 and MIL-STD-1275 for various mains voltages and end equipment.

In essence, the maximum voltage rating of the module must exceed the maximum voltage expected from the DC link with some margin or the module will be damaged.

Brief Avalanche Discussion

Out of this, regardless of derating, it is NEVER advisable to run an IGBT in avalanche mode for any amount of time. This is primarily due to the current path having much smaller cross section. The intrinsic MOSFET channel is off during an avalanche condition, thereby avalanche current can only flow from the intrinsic PNP collector to the periphery of the emitter structure on the surface of the device. This is often a very small cross section compared to forward biased mode, and an ill-advised power path.

Switching frequency and output frequency range

Most drives will use a PWM input of much higher switching frequency than the output fundamental. The switching or carrier frequency allows the PWM to modulate the duty cycle and create clean sinusoidal current waveforms from the output poles. For these applications, the maximum switching frequency or carrier frequency needs to be understood. This will be better explained in other sections, but switching loss scales with frequency. The higher the switching frequency the higher the switching loss.

There are exceptions to this. Some machines and drives are trapezoidal or self-commutated. In other words the switching occurs at the electrical commutation frequency of the machine. Switching loss in these machines is much less, however

they don't have the luxury of sinusoidal current waveforms. Torque ripple is often higher due to this drawback.

Desaturation

It is possible to draw a large enough collector current to push the IGBT into linear mode. Linear mode is highly dissipative. The device has a high voltage across the CE terminals and a high collector current. This can be catastrophic if the condition is present for too long.

This happens when the intrinsic PNP runs out of gain and falls from saturated mode with lower Vce to a more lossy, linear mode of operation with higher Vce referred to as "desaturation".

Vce is a secondary means to sense overcurrent. The current has to be high enough to force desaturation and detectable "desat" voltage across Vce.

Most gate drive circuits offer some form of desat protection, usually accomplished with switching diodes and a flying capacitor that samples Vce in the "ON" condition and blocks the high voltage in the off state. The small capacitor then stores Vce for a brief period where it is compared to a reference. Once the voltage is exceeded a fast interrupt occurs and in some cases it is followed with a flag to the central microprocessor and a lockout interval to allow cool down. The Dunipace work described later in this application note can be used in the gate drive circuit to accurately measure saturation voltage and make accurate, thermally compensated decisions on that voltage, but the effectiveness of this, or any other desat sense means is debatable.

There are two diametrically opposed schools of thought on desat sensing…..both with significant experience. One side said "desat sensing is an acceptable overcurrent protection mechanism" and the other said "desat sensing takes too long. By the time the desat condition is sensed as excessive Vce, the high fault current and resulting high temperature has damaged the device or bonding". The expense that the desat sensing opponent went through to measure current and quickly interrupt gate drive was extensive, although they often bragged about being able to "throw a tire iron" across the output and have the circuitry remain safe. Alternatively the current can be sensed by a traditional external current sense device. Clearly both sides agree on the ultimate necessity of overcurrent protection, but the paths differ from sensing fault current directly to sensing the resultant Vce Desaturation event.

3.) DC Bus Design and Capacitor Selection

DC Bus Design

The DC bus must offer the lowest possible inductance between the capacitor bank and the module to protect the device from transients. Additionally as discussed above, the main ripple current to the poles should be sourced from a low ESR, low ESL capacitor located at the IGBT terminals.

Beyond this, there is the matter of current carrying capability. If guidance on this is needed, the following work might be considered:

http://electronicdesign.com/boards/efficient-tool-sizes-high-current-pcb-traces

This article discussed current carrying capability and guidelines for PCB which is easily extended to busswork. Good starting guidelines for current density are in the 500CM/A range.

Capacitor Selection

In most off the shelf drives, there is a ½ line cycle hold over requirement. In other words, if the input power is interrupted for one half of a cycle (10ms in EU, 8.3ms in US), the drive has to keep operating. This gives rise to the enormous capacitor banks used in these drives, but that's not the only criteria in play. Note: 400Hz aircraft power busses need much less hold over storage due to the faster refresh rate.

In addition to storing enough energy to keep the drive operating at full load during a short power disruption, the capacitor bank must source the current to the inverter poles to run the machine at the switching frequency of each pole. By this, the capacitor bank must store enough energy for the holdover requirements and have low enough ESR and ESL to source the peak currents without excessive dissipation. To minimize stray inductance and the nuisance energy stored therein, it is strongly recommended that the primary DC bus capacitor be located right at the IGBT terminals. Larger holdup capacitors can be located some distance away on the buss bars, but the low ESR capacitor that sources the ripple current to the inverter must be as near the IGBT as possible. Selecting the proper DC link capacitor can make a big difference. Contact your capacitor vendor for a recommendation on the appropriate solution for your application

4.) Conduction and Switching Loss Calculations

The inverter design, like most any other power electronics design effort has to stay within the maximum junction temperature specifications of the IGBT. IGBTs have a maximum junction temperature specification in the datasheet, and most applications derate that even further based on the project specifications as well as house rules and procedures. To stay within this temperature specification you have to know the maximum ambient or boundary temperature, the maximum junction temperature, the thermal impedances and the losses in the device. Loss calculation is difficult for three phase inverters. Most are left to Mathcad™ routines or programs that capture each vector state and the switching losses between them as rms quantities.

Any loss calculation should be correlated with real, measured case temperatures in situ. Section 8 will cover applicable measurement methods.

The calculation below is based on Graovac and Purshel's work (References:[6]). It is much simpler than the sophisticated simulation programs. The basis of the calculation is to use the rms output current (Iout), the device voltage drops and resistances (Vce, rce, Vf, rd), the modulation index (m), the displacement power factor (PF) and the switching frequency (fsw) to deliver approximate conduction and switching losses.

The parameters of the test module used are:

Vce	1.80V
Vf	1.40V
Eon	5.8mJ
Eoff	17.2mJ
Err	13mJ
RthetaJC_IGBT	0.077 degC/W
RthetaJC_FRED	0.348 degC/W

Table 1.) Test module parameters

The junction resistances can be calculated by:

Eq1: $rce = approximate\ slope\ of\ Ic\ vs\ Vce\ curve\ at \max temp\ near\ typical\ Vce\ value$

For the test module used in this work:

$$rce = \frac{(2.80V - 1.15V)}{(800A - 0A)} = 2.1m\Omega$$

Eq2: $rd = approximate\ slop\ of\ If\ vs\ Vf\ curve\ at \max temp\ near\ typical\ Vf\ value$

For the test module used in this work:

$$rd = \frac{(1.80V - 1.00V)}{(800A - 0A)} = 1.0m\Omega$$

The conduction and switching losses can be calculated by:

Eq3: $Pcondloss_{IGBT} = (Vce * Iout) * \left(\frac{1}{2*\pi} + \frac{m*PF}{8}\right) + (rce * Iout^2) * \left(\frac{1}{8} + \frac{m*PF}{3*\pi}\right)$

Eq4: $Pcondloss_{FRED} = (Vf * Iout) * \left(\frac{1}{2*\pi} + \frac{m*PF}{8}\right) + (rd * Iout^2) * \left(\frac{1}{8} + \frac{m*PF}{3*\pi}\right)$

Eq5: $Pswloss_{IGBT} = fsw * (E_{on} + E_{off})$

Eq6: $Pswloss_{FRED} = fsw * E_{rr}$

For an initial starting point, the datasheet values for Eon, Eoff, Err and Vcesat at temperature must be used in the loss calculations. The phase current of course is based on the worst case load. As the design solidifies, iterate this calculation with measured values in situ. Use the measured Vcesat and Vf values as measured with the Dunipace circuit described below, as well as the Eoff and Eon values determined by in situ double pulse testing. There has been a lot of work done on scaling Eoff and Eon between the test currents used in the datasheet and the phase currents seen in situ. The best approach is to simply measure Eoff, Eon and Err rather than scale it. The scaling factor varies with device technology and is often misleading. There's no uncertainty in using the actual measured numbers.

5.) Thermal Design

Once the maximum conduction and switching losses are known, the thermal design is ready to begin. The thermal design has a very simple goal. The heatsink and thermal transfer must be sufficient to keep the devices below the maximum allowed junction temperature, but therein lies the problem. In a finished module, we can't measure the junction temperature. We can measure the case temperature and possibly the value of a thermistor located near the dice.

The datasheet gives Rthjc for the individual IGBT's and FRED dice in the module. The maximum ambient temperature is known by this point and the in house design rules that give maximum junction temperature guidelines are in play.

The switching and conduction losses can be calculated (and later iterated upon with more exact values from section 8 in this work).

All that remains is the means to get the heat away from the module and the interface between the module and the heatsink.

This is best brought together with an example. Let's say we are using the test module mentioned above. The inverter is switching at 4kHz, delivering 200A rms per phase with a machine PF of 0.8 and a modulation index of 0.85.

1.) We calculate the following losses per IGBT and FRED given the 4kHz switching frequency and the worst case load current of 200A rms per phase.
Per EQ3: IGBT Conduction Loss=104.4W per switch
Per EQ4: FRED Conduction Loss=76.2W per switch
Per EQ5: IGBT Switching Loss=92W per switch
Per EQ6: FRED Switching Loss=5.2W per switch

2.) From the table 1 we have RthetaJC values:
- RthetaJC_IGBT=0.077 degC/W
- RthetaJC_FRED=0.348 degC/W

3.) The thermal constraints for the design are:

- Tjmax=150 degC
- Tambient_max=50 degC

4.) If we apply RthetaJC, from the max allowed junction temp (assuming included margin), we get:

- IGBT Temp rise (Junction to case)=196.4W*0.077degC/W=15.1 degC
- FRED Temp rise (Junction to case)=81.4W*0.348 degC/W=28.3 degC

What this means is that the case temp MUST BE HELD at approximately 120 degC to meet the maximum junction temperature requirements.

5.) From this we can specify the heatsink. There are two IGBTs and two FREDs in this module package, thereby there is 555.6W of heat to be removed.

6.) RthetaCS combined with RthetaSA then has to be:
RthetaCA=(120 degC case temp-50 degC max ambient)/555.6W =0.126 degC/W

7.) The thermal compound has an RthetaCS of 0.05 degC/W. If by chance, the calculations in 6.) came out to less than this number, the module is too small for the application.

8.) The heatsink then needs to have RthetaSA of 0.126 degC/W-0.05 degC/W or 0.076 degC/W. A good heatsink with proper airflow can accomplish this. Heatsink and coldplate vendors have this information on their various extrusions and cold plates varying over air or coolant flow rates.

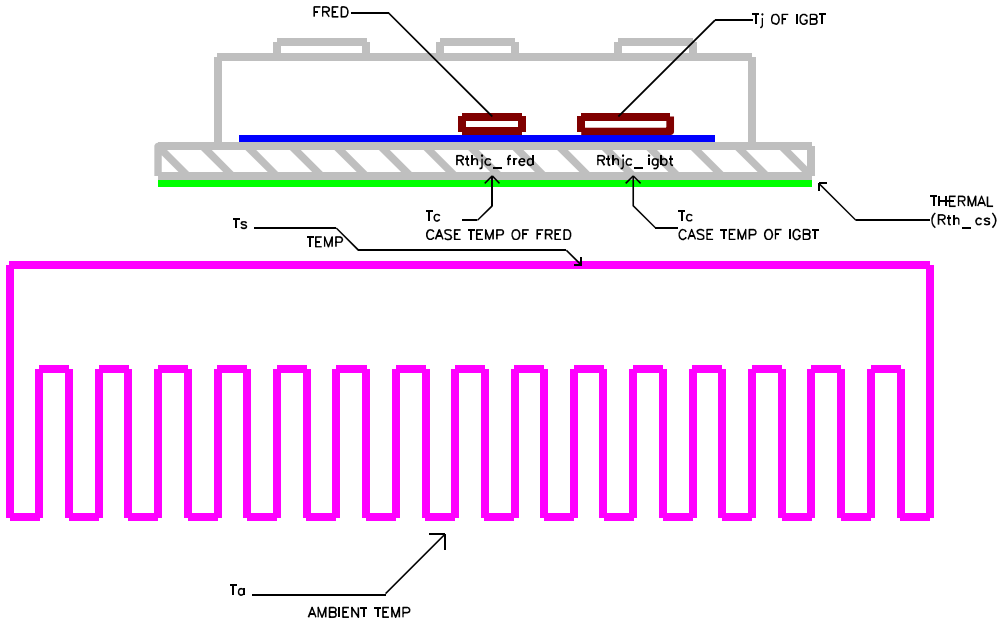

Figure 2: Thermal stackup. Note Rthjc is for individual die.

6.) Gate Drive

This is often the most difficult part of the design. From a power standpoint, the gain between the gate drive circuitry and the output devices is absolutely astonishing.

Fundamentally the gate drive circuitry applies a positive voltage, +15V to the GE terminals of the IGBT to turn it on, It then applies a slightly negative voltage to turn the device off. Most IGBT's have a threshold of 5V or so which tells us that 15V is certainly saturated ON condition and 0V is certainly off. So the question arises: "why pull the device negative in the off state". The answer is pretty simple if we consider the device capacitances and how the IGBT half bridge or pole commutates.

If we have a half bridge as depicted in figure 4, when we turn on the high side switch the lowside switch has to go from nearly 0V or VCEsat to roughly the DC link voltage quickly. The faster the high side switch turns on, the faster the lowside switch capacitances have to charge up (the inverse is perfectly true for turning on the low side switch and charging the high side capacitances). The low side switch has non-negligible Coes, Cres, and Cies as does the high side switch. As the high side is turning on, the low side Coes is charging from about 2V VCEsat up to the full DC link voltage. This fast charging is also applied to the Cres and Cies capacitors in series of the low side switch. Cres is always much smaller than Ciss, but if the voltage change is fast enough, and the driver off state impedance is high enough, Cres can couple enough charge into Ciss to bring the low side switch into an on condition. This is a highly dissipative mode because the high side switch is on at this time. If severe enough it becomes a shoot through condition. This is known as Cdv/dt turn on. It is possible in both the high and low side switch of the output pole.

On the bench, this is seen as a positive voltage excursion across Vge of the IGBT in the off state that occurs at the falling edge of Vce of the switch that is going into the on state just after the FRED reverse recovery pulse. Bulletproofing to avoid this mode of operation includes choosing a low impedance totem pole output in the gate driver, a low series gate resistance (referred to in this work as Ron) in the off state, and pulling the device to a negative voltage to turn it off. Using -5V for the off state with modern devices is a safe design practice. With a good driver there should be no Cdv/dt turn on problem.

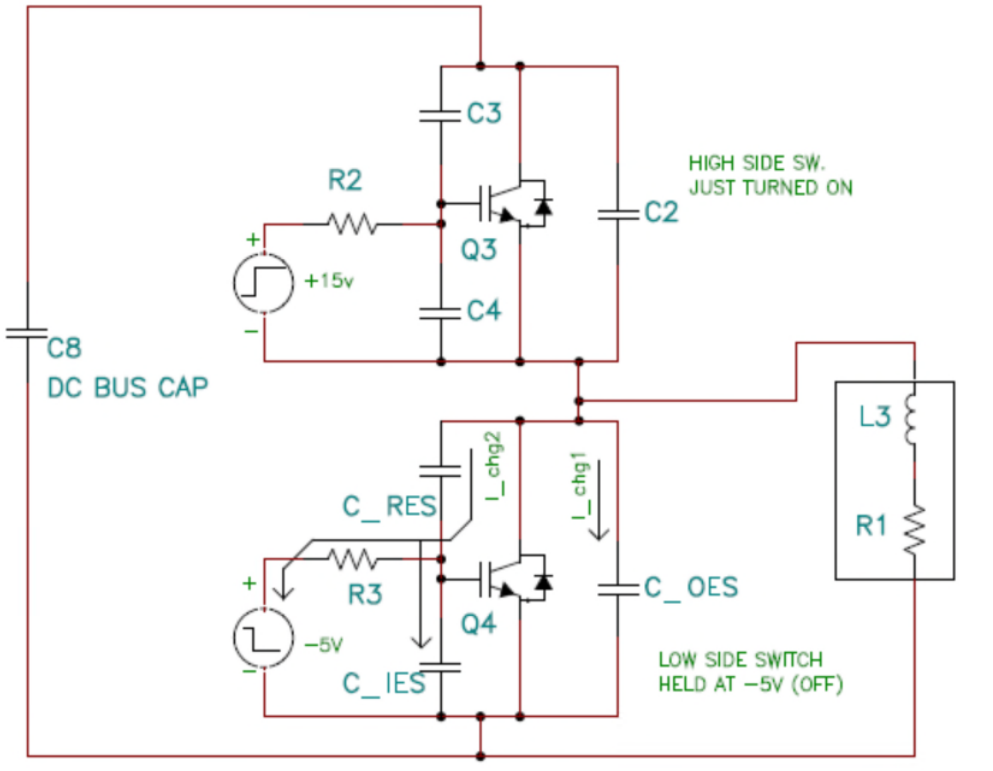

Figure 3. Half bridge illustrating Coss, Ciss, C*dv/dt turn on, Crss

7.) Mechanical Assembly

Mechanical Connections

Most modules are built on traditional base plates. The baseplates are then bolted to the thermal management system with appropriate interface material. To think through it, no module baseplate that goes through that much processing can come out perfectly flat without a post process grind and an anneal. The grind would be expensive and the anneal would be destructive to die attach reliability, thereby these things are impractical

and not done. Instead of this, the module baseplate is designed and manufactured to be slightly convex at the end of the process. (see figure 4). This is then corrected with a proper torqueing sequence after the thermal interface material is applied. The torqueing sequence and resultant holding force correcting the convex nature of the baseplate is in no way detrimental to the module.

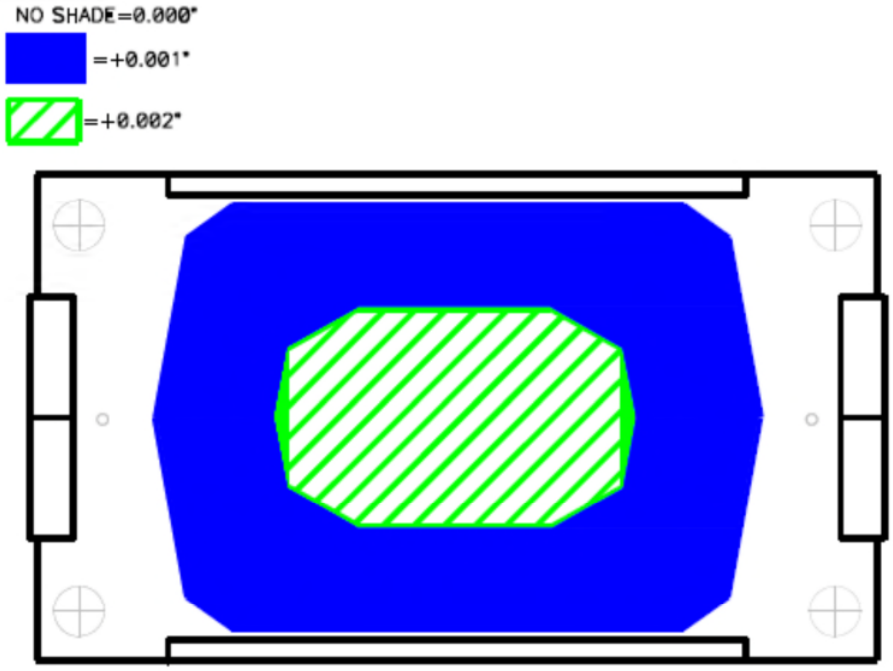

Figure 4. Inspection block measurements of module showing slight convexity, bottom side facing up.

To look at the other extreme, if the module baseplate were concave, no amount of torque or holding force on the corners could correct that. There would be an air void or excessive thermal compound thickness under the middle of the module and the thermal impedance would suffer accordingly.

As for the thermal interface material, a thin, uniformly applied paste material similar to Wakefield type 120 is recommended with good application technique and no excess.

The recommended screw to attach the module to the heatsink is an M6 x 1.0mm or M5 x 0.8mm.

Thread depth should be 2-3 screw diameters deep and the threads should be drilled and tapped to provide class 2B fit or better. The recommended maximum torque for the screws is 6.0Nm or 53 inch pounds as per the module datasheet. In an aluminum heatsink, perhaps 6061 material, most any machine shop reference will show that the threads can easily withstand 5 to 5.5 Nm or roughly 44 to 49 inch pounds of torque respectively with the above fit and thread depth.

The torque limiting device should then be set for 5 Nm or 44 inch pounds (see figure 5 and figure 6). This will provide plenty of force to flatten the module and engage the Belleville washer. The torque sequence should go from corner to corner with one intermediate setting. If the holes in the module were numbered in a clockwise fashion, 1, 2, 3, 4, the torque sequence should be: Step 1 (20 inch pound limit setting) 1-3-2-4. Step 2 (44 inch pound limit) 1-3-2-4. This will provide a great thermal interface and even loading.

Figure 5. Proper torque limiting device, can also be in wrench form or preset on a pneumatic or electric production tool

Figure 6. NOT A TORQUE LIMITING DEVICE!!! DO NOT USE THIS FOR TORQUING DOWN MODULES!!

For the hardware and bolts that hold the module to the heatsink, most any grade screw will work. In a harsh environment, a stainless steel screw should be considered. Belleville washers are recommended immediately under the bolt head to offer a little mechanical compliance once proper torque is applied (see figure 7 and 8). Under the Belleville washer, an appropriate size flat washer is recommended to spread the holding force as much as possible. On the screw threads, a ***dried patch*** of Loctite 242

thread locking compound or similar is recommended. Wetcompound may interfere with the thermal compound and weaken one or the other, so it is to be avoided. The combination of these things gives every screw mechanical compliance, force distribution and anti-rotational properties in addition to proper holding force in the module.

Figure 7. Belleville washer

Figure 8. Belleville washers on module (immediately under screw head, just above flat washer).

The backside nuts are for illustration purposes only. Normally this is a tapped hole in the heatsinlk.

Electrical Connections
The electrical connections should be torqued down in a similar fashion as the mechanical assembly. The torque limits in the datasheet should be used. The electrical connection may also use Bellville washers and anti-rotational hardware, but the bussbar to terminal contact needs to be kept clean and free from any debris. Use of liquid threadlocker or films is discouraged for the electrical connections. If excess material gets between the terminal and the bussbar interface the contact impedance will be excessively high. There is no torque sequence needed or intermediate torque step for these connections as there is no seating of thermal compound.

8.) In Situ Measurements

Measurement Techniques
For a large inverter design, measurement is difficult. There will be nearfield magnetic noise that will couple into any and all measurement loops. Take your best effort to keep all of the line, load and measurement leads well twisted to cancel induced voltage, shielded to avoid electrostatic coupling and as short as possible to keep the radiating/receiving loops and surfaces to a minimum. If you have the time, take a look at Michel Mardiguian and Henry Ott's books [2] and [3] on Electromagnetic interference and mitigation. The books hold no magic secrets, but they do reinforce these fundamentals in better detail than can be had herein.

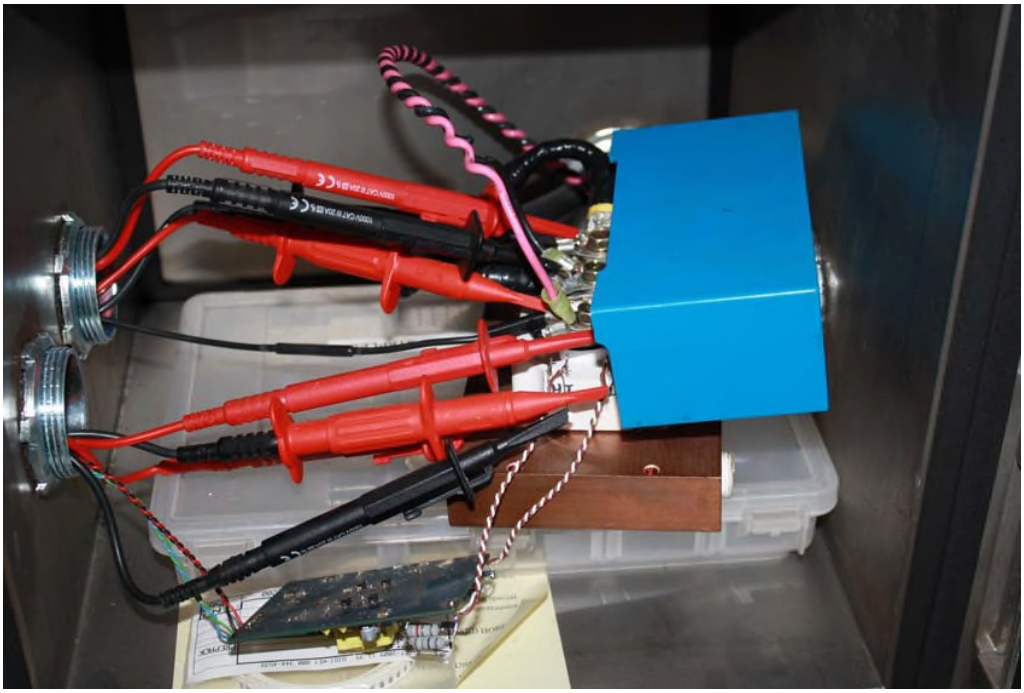

Figure 9. Incoming power leads are twisted, as are gate drive leads and measurement leads. Everything kept as short as possible. (Incoming conductors not sized for continuous operation, bus cap supplies double pulse power). The bus cap is directly on the IGBT module, Load line to inductor exiting box right, cooling lines for cold plate exiting box rear.

Conduction Loss Measurement
As a part of the design validation task, it is advisable to take a look at the conduction waveforms of the IGBT's. Unfortunately this is not an easy task. If the device is blocking perhaps 400 or 800V and we are trying to see a 2V drop during saturation, this measurement is impossible with conventional instrumentation and probes. Even if

the vertical gain of the oscilloscope is increased to resolve the 2V saturation, the clipped blocking voltage will saturate the vertical amplifier. Saturation recovery will distort the Vce sat waveform displayed.

And this is where Dr. Richard Dunipace made a wonderful contribution [1] that is cited with his permission. He designed a small amplifier circuit that uses an ultrafast, high voltage diode to block the high voltage and measure the Vce thereby keeping the oscilloscope out of saturation. The circuit can be found at:

http://powerelectronics.com/discrete-power-semis/test-saturation-voltage-achieve-high-efficiency-2

Inverter Commutation

Most inverters use a centered PWM approach. If the load current is continuous in this scheme, the diode of one switch in a pole will be hard commutated by the turn on of the opposite switch in the pole.

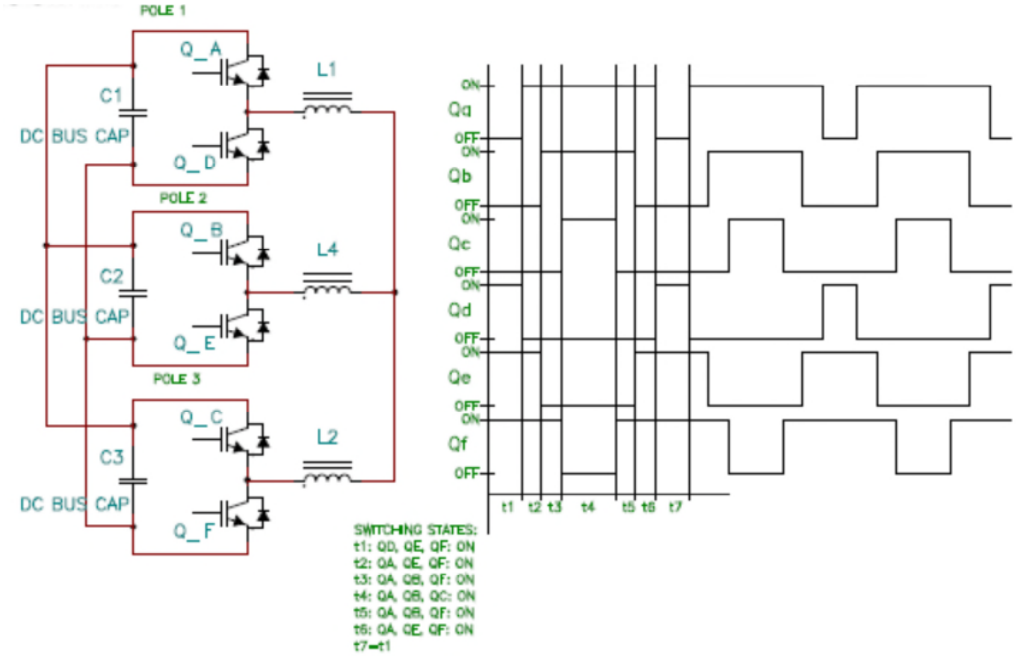

Figure 10. Looking at the switching states, with an inductive load it becomes clear that the FREDs are hard switched most of the time.

Hard commutation in the inverter closely resembles the double pulse tester measurement that is used to determine Eoff, Eon, and Qrr of the IGBTs and respective FREDs. Double pulse tests can be done with substantially lower average power levels to validate the gate drive, DC link capacitor, Busswork and stray inductances.

Double Pulse Tester (Used for switching loss measurement)

The schematic for the double pulse tester can be seen in figure 11 below. The first pulse is known as the soak time for the load inductor (see figure 14 and 15, t1). This ramps up the current.

Timing for this is a reasonable pulse, usually something in the 20 to 50us range with the inductor sized accordingly to ramp to proper current value in that time.

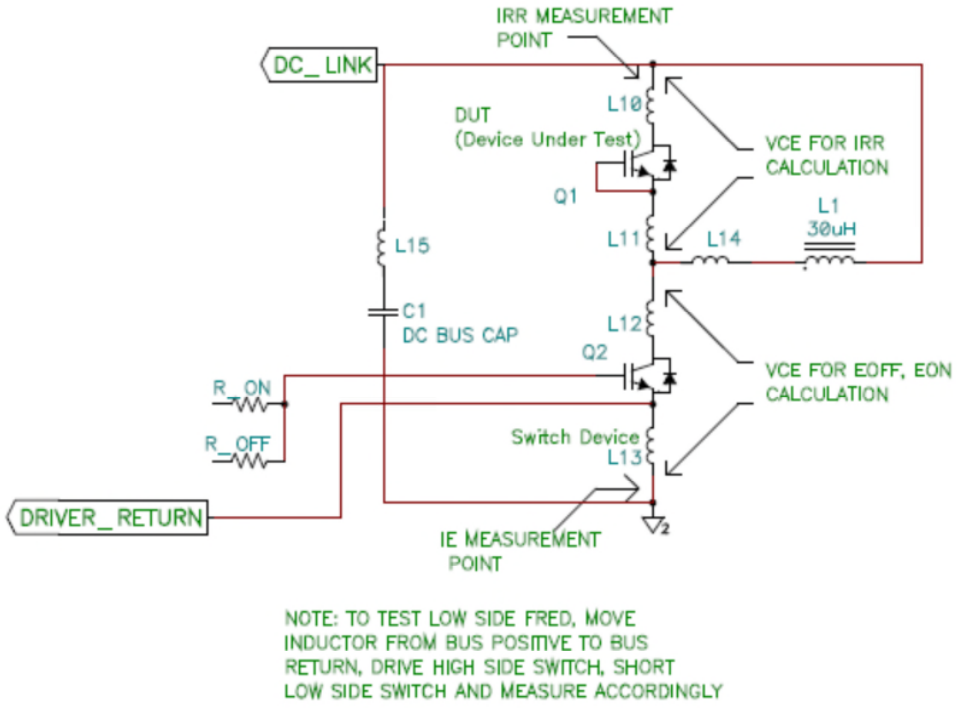

Figure 11. The double pulse tester with stray IGBT inductances illustrated.

The deadtime between the pulses is usually small, on the order of 5 to 10us to keep the current from decaying too badly (see figure 14 and 15, t2). During this deadtime, the pole commutates such that the opposite FRED is freewheeling (figure 12 and 13, t3). On the beginning of the second pulse, the FRED is hard switched by the opposite switch applying full DC bus voltage across it (figure 12 and 13, t4). This represents the fastest reverse recovery event. If the voltage across the switching IGBT is measured along with the current, the Eon loss includes the reverse recovery loss in the opposite FRED. Additionally FRED current and voltage are multiplied and integrated for Err, the current is integrated for Qrr, and ta, tb, Irr and associated di/dt values can be measured. This test determines the diode data. This test is to be done in situ on the inverter being designed once all of the bus capacitors are known, the buss work is complete and the load connections are defined. This can then determine the Eon, Eoff, and Qrr specific to the stray inductances in the circuit.

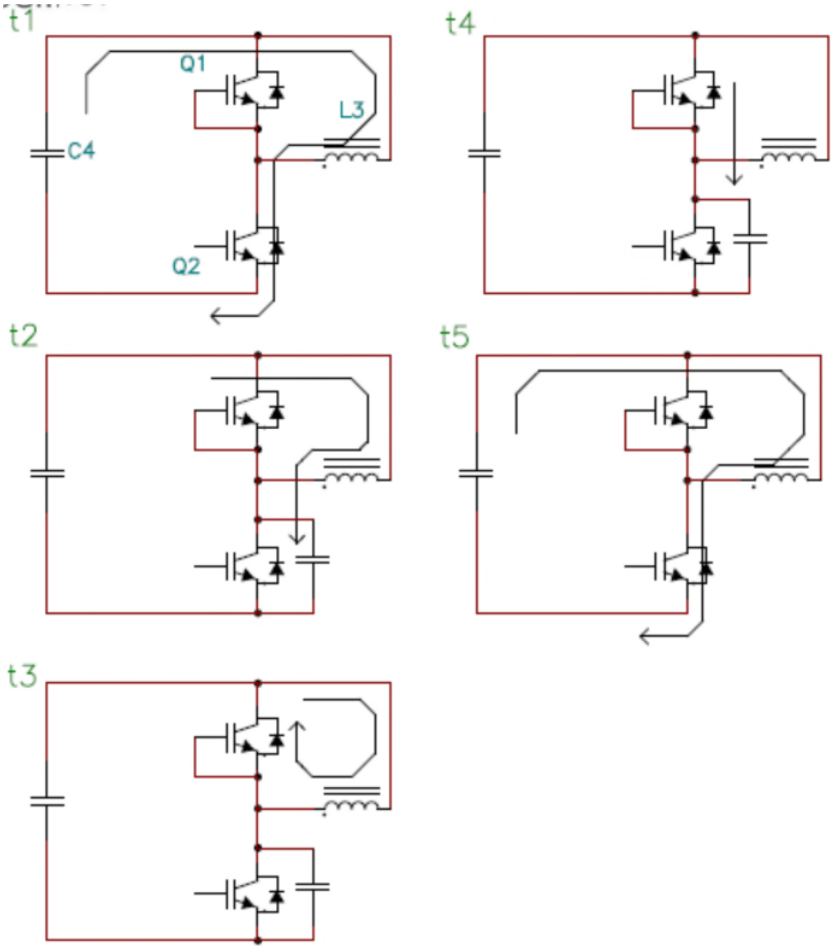

Figure 12. Double pulse tester switch states and current paths for low side device Eoff, Eon measurements

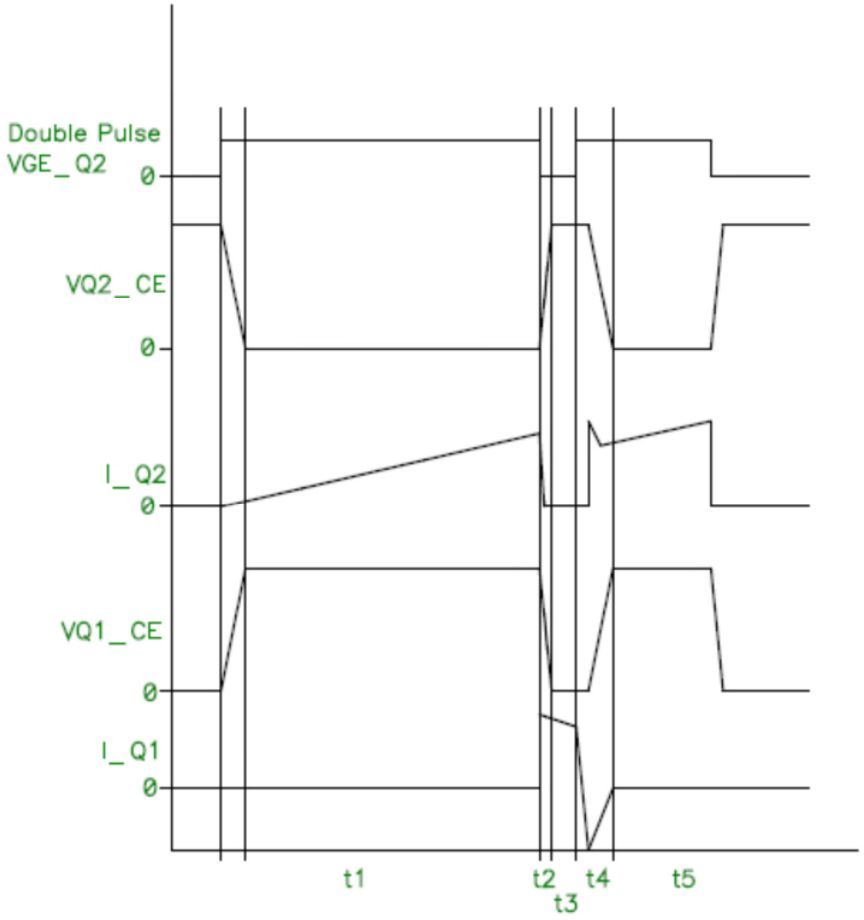

Figure 13. Double pulse tester waveform illustration

Once the specific diode characteristics are known under hard commutation, it may be necessary to adjust the di/dt on the turn on edge by tuning Ron (recall this generates the di/dt that forces FRED commutation). For example if there is excessive ringing during hard commutation, this will likely show itself later as a nearfield EMI problem. To mitigate this may require slowing down the di/dt at turn on by increasing Ron. It may also require adding snubbers from the output of the pole to bus return.

Most IGBT datasheets will give a Qrr specification for the FRED—the value of the Irr integral. By this, a snappy diode with fast tb and large Irr can compare similarly to a soft diode with longer tb and softer Irr. The specific data is illustrated in figure 14. It's often not given due to the large set of possibilities for gate drive resistance and the varying diode characteristics over these di/dt ranges. It's not an oversight or a secret that is held back from the IGBT vendor, rather something that needs to be measured and addressed for each application. For a snappy diode with large Irr and fast tb, it may be necessary to slow down the turn on of the IGBT with larger Ron in the gate drive path. It may also be necessary to add snubbers to each half bridge output to damp any parasitic ringing from this snappy event. Snubbers are detailed in section 9 below.

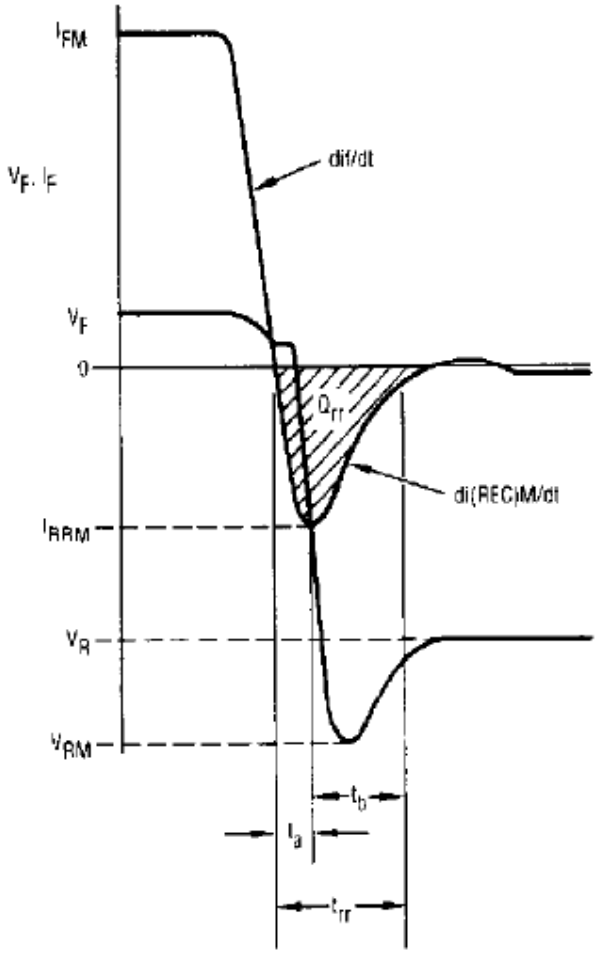

Figure 14. Diode reverse recovery waveform.

Once the preliminary calculations are complete and the prototype inverter and thermal management system is ready for preliminary evaluation effort, it is necessary to measure the Eon, Eoff, Qrr and the diode parameters in situ. This is done with the double pulse tester that was described in figure 11 above. It will require the addition of a load inductor, often air core, located well away from the work area.

To measure Turn On loss, both pulses are needed from the double pulser. The switch current and voltage are multiplied and integrated. Turn on loss includes the forced recovery of the opposite FRED. A turn on loss measurement for the test module is included in figure 16 below.

To measure turn off loss only a single pulse is needed and the turn off measurements are multiplied and integrated. A turn off loss measurement for the test module is included in figure 18 below.

Reverse recovery is measured much the same as turn on loss, only with the measurements taken on the opposite switch (the FRED that is hard commutated). A reverse recovery measurement for the test module is included in figure 17 below.

Note, the double pulser doesn't have to be a $5000 instrument and three days of coding on Labview ™. I opened a CD4000 logic databook, found a CD4098, breadboarded, shielded, and put a Schmitt trigger buffer in front of it to square the trigger pulse. It took about two hours to design, build and setup with 20 turn pots for soak, dead and second pulse times and it has worked fine for years (figure 15)

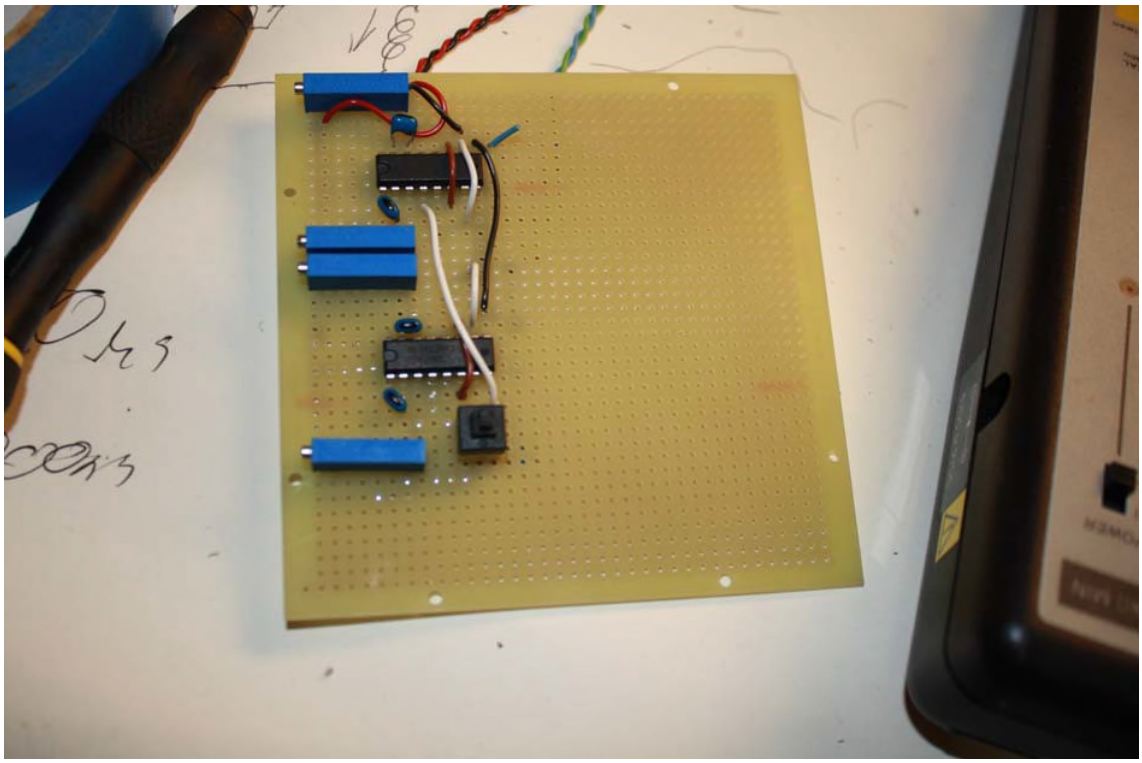

Figure 15. Home brew double pulse board. Two CD4098 IC's daisy chained with diode OR'ed together, the schematic comes straight from the datasheet.

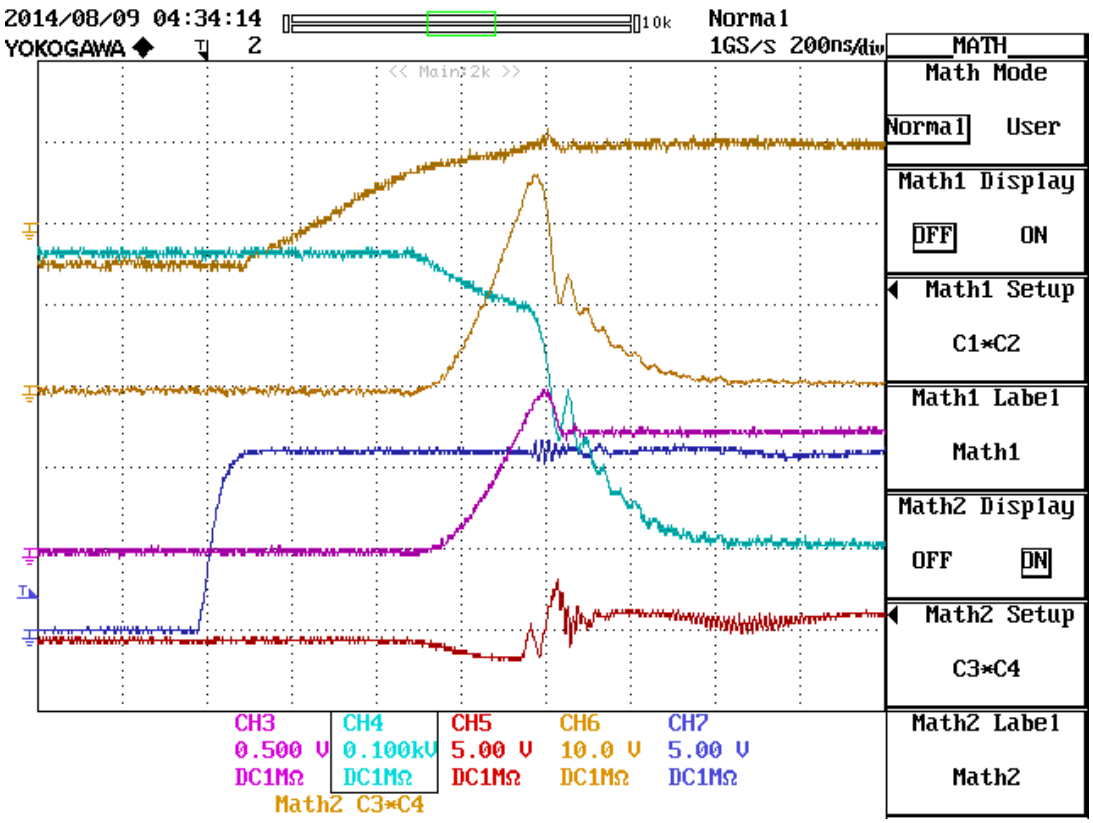

Figure 16. Eon measurement for test module, Ron=18 Ohm, Roff=6 Ohm. Ch3=Ic 100A/div, Ch4=Vce 100V/div, Ch5=Vge, Ch6=Vge, Ch7=pulser output. Math=50kW/div. Eon=32.5mJ

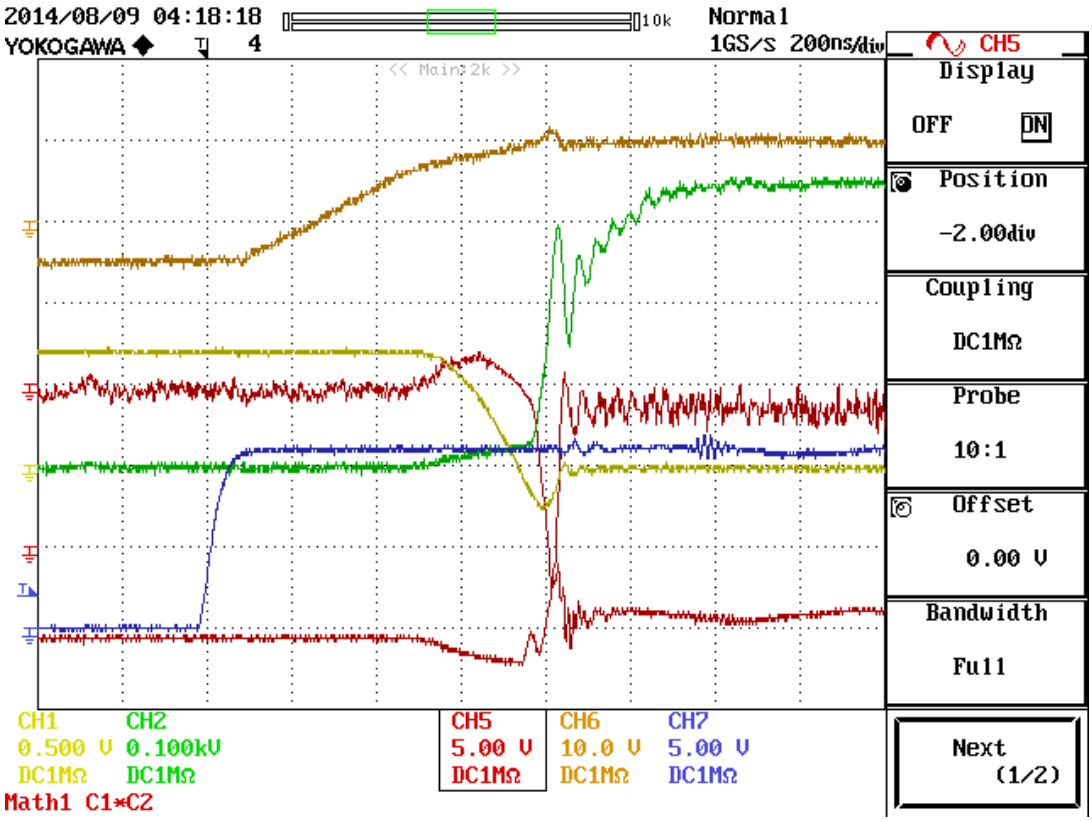

Figure 17. Qrr measurement for test module. Ron=18 Ohm. Roff=6 Ohm. Ch1=Ic, 250A/div. CH2=Vce, 100V/div. CH5=Vge, 5V/div. CH6=Vge, 10V/div. Ch7=Pulse. Qrr=10uC, di/dta=2400A/us, di/dtb=2500A/us, ta=60ns, tb=50ns, Irr=125A

While the 18 Ohm Ron exibits very minor oscillation, it represents a good tradeoff between turn on speed and snappy FRED reverse recovery. The Qrr waveform can be seen in figure 17.

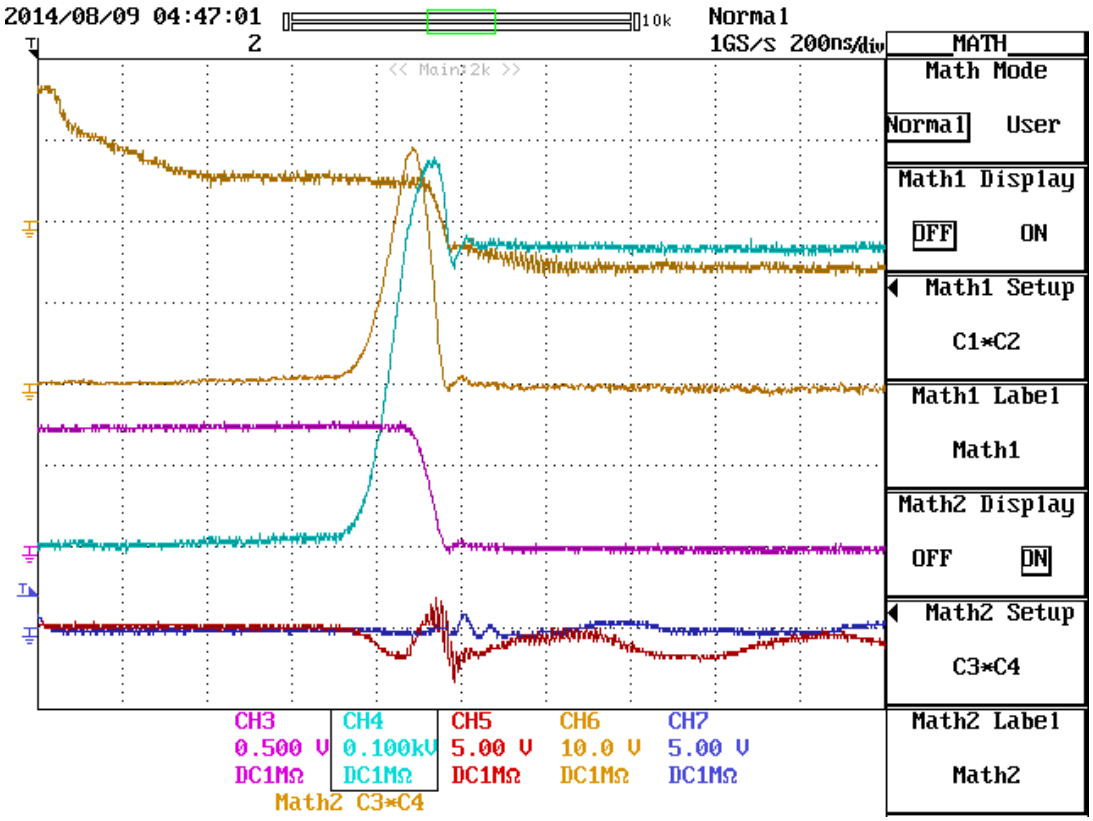

Figure 18. Turn off loss measurement for test module. Ron=18 Ohm, Roff=6 Ohm. CH3=Ic, 250A/div. CH4=Vce, 100V/div. Ch5=Vge, 5V/div. Ch6=Vge, 10V/div. Ch7=Pulse.
Math=50kW/div. Eoff=18mJ

While the double pulser is hardly indicative of real life commutation and steady state operating conditions, it does provide an excellent means to duplicate the peak pulse power levels and to see and tune the turn on and turn off losses by adjusting Ron and Roff. Further it provides direct examination of any ringing on the reverse recovery event.

Tuning Ron

It is possible to decrease Ron to reduce turn on loss in the IGBT. The impact of this on turn on loss can be seen in figure 19 below. If Ron is decreased to the Roff value, note the excessive ringing in the waveform.

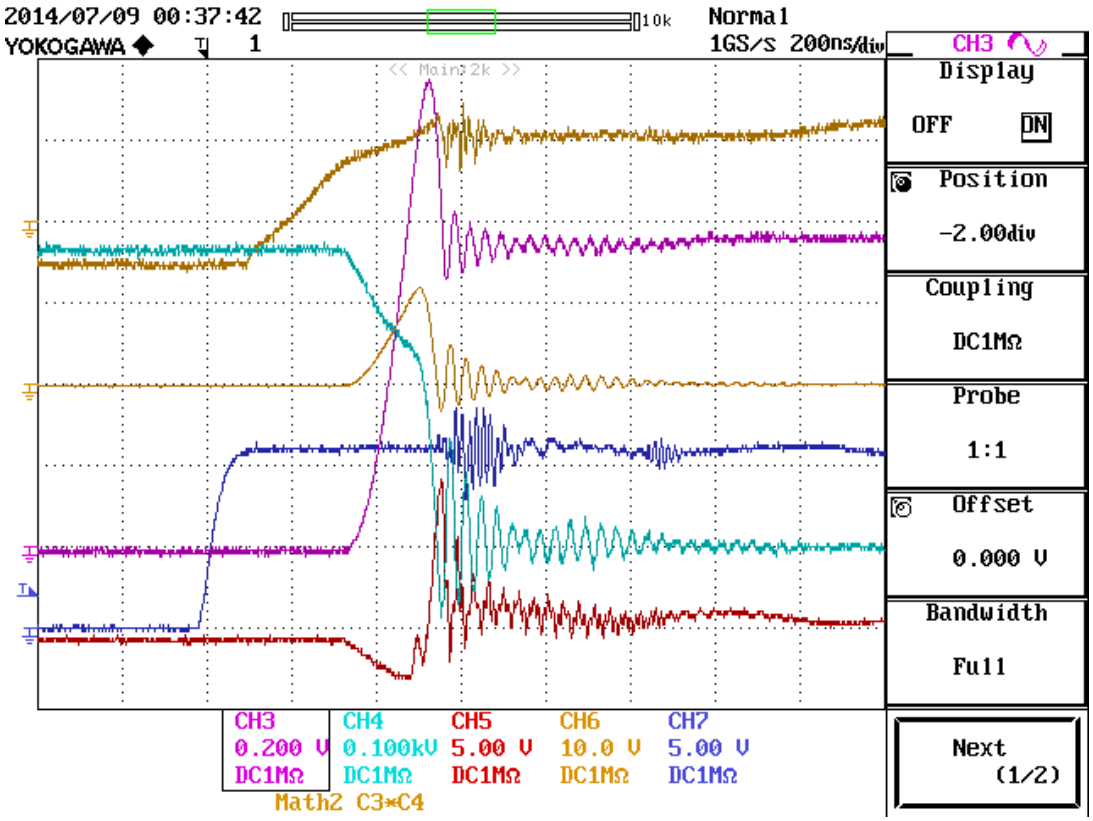

Figure 19. Eon measurement for test module Ron, Roff=6 Ohm. Ch3=Ic 100A/div, Ch4=Vce 100V/div, Ch5=Vge, Ch6=Vge, Ch7=pulser output. Math=100kW/div. Eon=13mJ

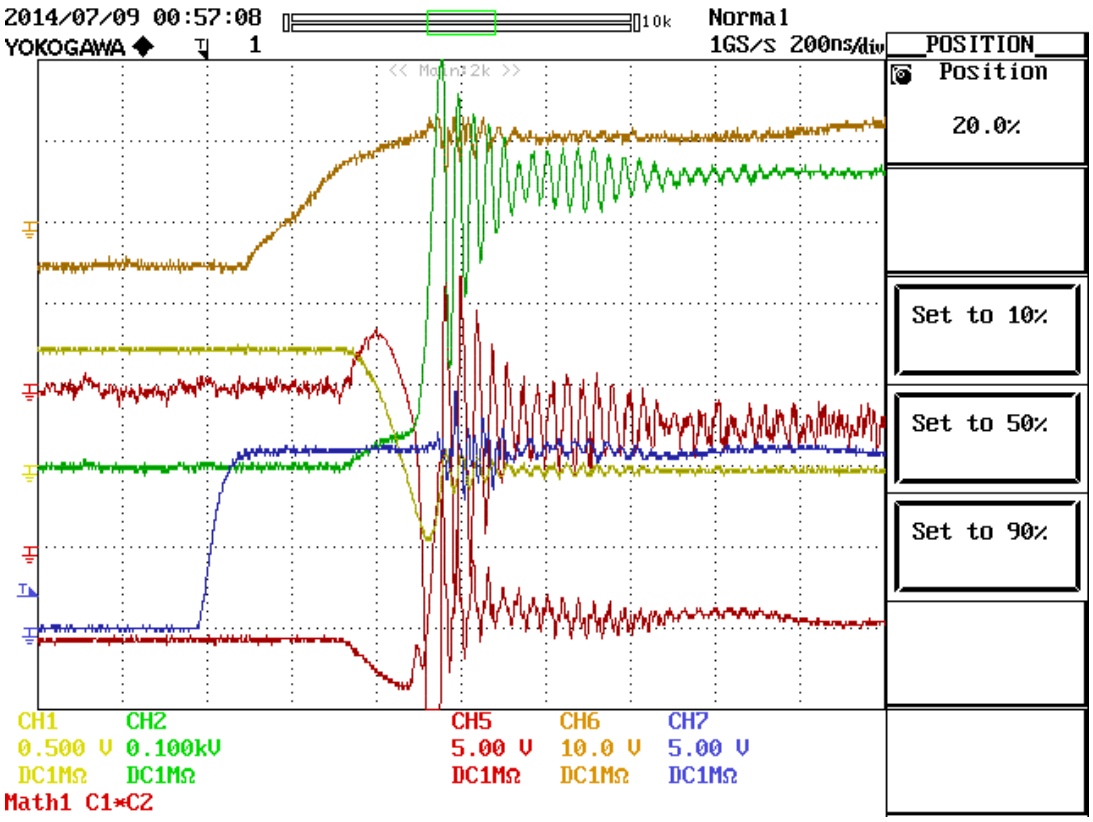

Figure 20. Qrr measurement for test module. Ron, Roff=6 Ohm. Ch1=Ic, 250A/div. CH2=Vce, 100V/div. CH5=Vge, 5V/div. CH6=Vge, 10V/div. Ch7=Pulse. Qrr=18uC, di/dta=3800A/us, di/dtb=6200A/us, ta=60ns, tb=50ns, Irr=225A

The turn off resistor in these tests was kept the same at 6 Ohms. It can be seen in figure 21 that the turn off losses are essentially the same.

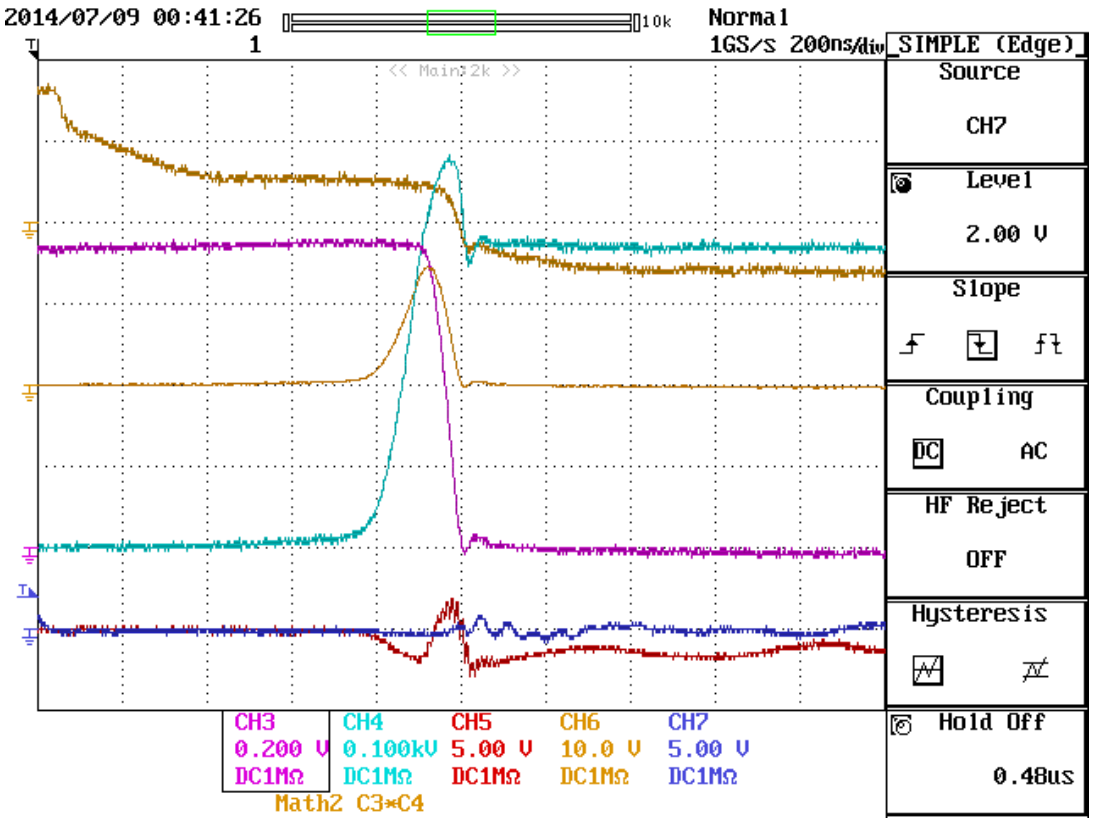

Figure 21. Turn off loss measurement for test module. Ron, Roff=6 Ohm. CH3=Ic, 100A/div. CH4=Vce, 100V/div. Ch5=Vge, 5V/div. Ch6=Vge, 10V/div. Ch7=Pulse. Math=100kW/div. Eoff=18mJ

Switching Loss Summary:

Eon, Eoff, Qrr data	Ron (Ohm)	Roff (Ohm	Eon (mJ)	Eoff (mJ)	Qrr (uC)	Irr (A)	ta (ns)	t (ns)	di/dta (A/us)	di/dtb (A/us)
Good turn on loss, no turn on ring (fig 16, 17, 18): 6 Ohm RG in turn off path, 18 Ohm Rg in turn on path	18	6	32.5	17.5	10	125	60	50	2400	2500
Roff=Ron, Great turn on loss, 28MHz oscillation : 6 Ohm Rg in both turn on and turn off path	6	6	13	18	18	225	60	50	3800	6200

Table 2. Switching loss data

Note that decreasing Ron had no impact on turn off energy. The slower di/dt on the slower turn on edge stopped the 28MHz oscillation. It also reduced Qrr of the FRED, as well as Irr, and di/dta, di/dtb. The turn on energy was higher with slower switching, at the tradeoff of having no ring.

9.) Snubber Design

In a practical design, the right answer for Ron might be somewhere between 18 and 6 ohms with a snubber circuit from midpoint to bus return to damp the oscillation from the stray inductance and the IGBT capacitances. The snubber would take the form of an RC network and there would be added losses with this addition (see figure 22).

To properly design the snubber circuit requires an understanding of the local inductances and capacitances in play. The section below on stray inductance deals with the lumped aggregate of the stray inductances in the module. The inductance causing the ringing is a smaller portion of that aggregate sum.

The best way to compute the parasitic values in play is to first accurately measure the ring frequency. From this point add a little capacitance (perhaps Coes/2) from the pole output to bus return as near the module as possible with shortest leads possible. See if the frequency changes at all. It should drop slightly. From this, we can calculate the lumped parasitic values in play because we have two equations in two unknowns:

Eq7: Fres=1/(2*pi*sqrt(LpCp))

Eq8: Fres'=1/(2*pi*sqrt(Lp(Cp+Cadd)))

If we solve for Lp and Cp, we get:

Eq9: Lp=(Fres^2-Fres'^2)/(4*pi^2*Fres^2*Fres'^2*Cadd)

Eq10: Cp=(Fres'^2*Cadd)/(Fres^2-Fres'^2)

With this solution we can then choose a snubber capacitor such that the resonant frequency is shifted down an octave:

Eq11: Csnubber=3*Cp

The resistance required to overdamp the circuit is then approximated by:

Eq12: Rsnubber>2*sqrt(Lp/4Cp)

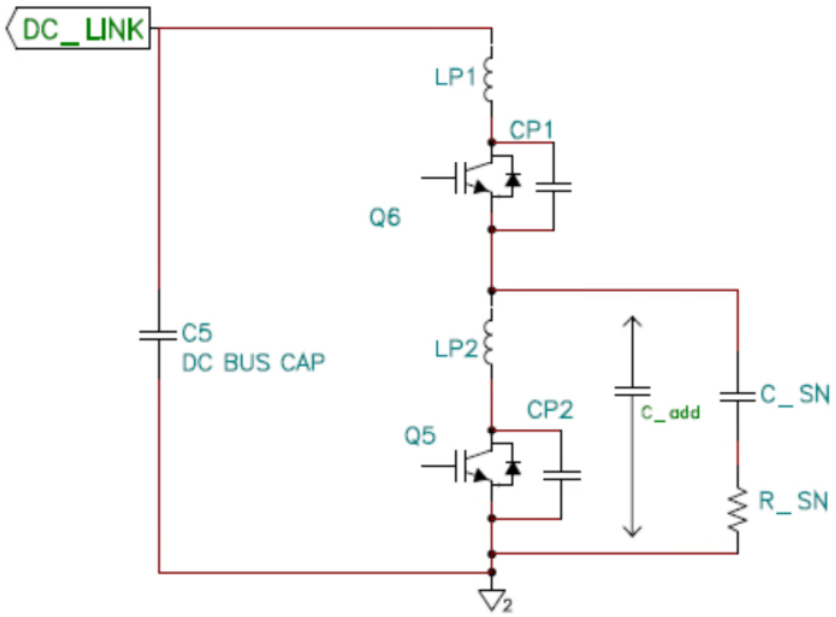

Figure 22. Schematic of snubber circuit

10.) Stray Inductance

The stray inductance is illustrated by the series inductances LP1 and LP2 associated with the switches capacitor and DC bus in figure 2. It can be backed out mathematically from the Eoff waveform. Initially, when Vce is first rising, there is an overshoot on the Vce waveform. The voltage overshoot is the voltage across the stray inductance. For figure 21, this voltage is about 100V. This voltage occurs as the current through the switch is rapidly decaying to the off state. Note that the load inductance is not included in this current path. The di/dt of this edge can be used in conjunction with the voltage overshoot to calculate stray inductance. The di/dt of this edge in figure 21 is approximately 5000A/us. This stray inductance is the sum of the DC bus cap ESL, the internal module inductance, the termination inductances from the module to the DC bus and the riser inductance from the module substrate to the terminations.

From V=-Ldi/dt, we have 100V=L*5000A/us. By this, Lstray=20nH.

Stray inductance is a good thing to watch. The application engineers can tell you the module internal inductances, so it is easy to see how much inductance is in the DC bus cap and DC bus. If stray inductance is too large, the stored energy in the stray inductance will negatively impact switching losses as it has to be commutated on every cycle.

11.) Safety Considerations

In a development cycle there are measurements, tests and failure points that need to be found. This often involves working on live equipment at or beyond maximum power levels. Clearly this work can only be done by qualified personnel. The Occupation Safety Hazards Administration does a good job outlining safety procedures under 29 CFR Part 1910.333. Live equipment likely falls under 1910.333(c2), which does not specifically spell out procedures, techniques, tools and Personal Protective Equipment (PPE).

In keeping with the good nature of the standard, ***safety throughout a high power inverter development, design and testing cycle IS the responsibility of the tasked engineer(s).*** They are to have all proper training, tools, PPE and related safety

equipment. Don't underestimate or cut corners on safety gear and protective equipment. Listed below are a few suggestions that may help in the safety process.

1.) Understand and identify the shock hazards. Use appropriate procedure and PPE. Set up the measurement properly with everything de-energized, then apply power and ramp up voltages slowly.
2.) Understand the CV^2/2 energy stored in the capacitor bank as well as the ESR of said bank. This is often enough energy to destroy modules. Further understand that the line fuse or breaker in the system feeds this rectifier/capacitor bank. Meaning, the capacitor
bank will have to substantially discharge before the line current can rise high enough to trip a thermo-magnetic breaker or exceed the I^2*t value of the fusing.
3.) Understand the LI^2/2 energy stored in the stray inductances as well as the machine and how they interact. Add pairs of protective contactors in series with the input mains and or load. Have the contactors easily opened, perhaps by means of a E-stop button or a
safety switch ran from an isolated low voltage source to drive the contactors. Inrush might have to be considered and accounted for, but this gives the user an isolated, independent switch to shut things down
4.) Consider and FPGA in the engineering development cycle between the motion control engine and the gate drive circuitry. The FPGA should be set up to look at all of the PWM pulses coming in and disallow switchthrough events, instantaneous reversals, and events where the deadtime is too short. The propagation path for FPGA inhibit output needs to be the fastest possible. Typically this is done via fast optoisolator to the gate driver output. Interrupts in this fashion can be as fast as 200ns. The FPGA is often removed once the motion control code is solidified and proven.
5.) Set up all measurements and validate waveforms and operation at a lower voltage before ramping to full power. This gives time to get the instrumentation setup and understand any nuisance nearfield magnetic noise in those waveforms.
6.) Make use of a shield or barrier for high energy measurements. We can pretend it doesn't happen, but on occasion, whether intentionally or unintentionally, a device will be faulted and the capacitor bank will dump into the fault to clear it. This often causes a rapid decomposition event. Shielding is mandatory.
7.) Use isolated probes. Current Probes, Rogowski probes, isolated HV differential voltage probes……this all allows the oscilloscope to be bonded to earth and maximally safe. The alternative is to float the oscilloscope. This ill advised shock hazard adds additional stress to even the most seasoned bench veterans.
8.) Use PPE. Although not specifically rated, you may find it advantageous to have a pair of class II lineman's gloves, a resistor and a relay or solid state switch to quickly discharge the capacitor bank on power off or interrupt, a pair of ear muffs to keep the secondary
reaction from a rapid decomposition event to a minimum, a welding jacket and face shield as secondary protection beyond the shield or guard. Again, in most any safety forum, the responsibility to keep safe resides with the individual doing the work. These are merely suggestions based on extensive experience with these things spanning both the theoretical and hands on.
9.) Save the data to a thumb drive, download it later. Or use a blue tooth link or something other than a wired connection from PC to oscilloscope. Why add the additional ground loop when it's not needed?
10.) Keep a CO2 fire extinguisher handy. Seldom to never needed, but it makes the development bench that much more robust. Safe work is good work.
11.) Have good ventilation over and around the bench and machine.
12.) Use the buddy system. Never work on high voltage, high energy circuitry alone. Yes, there will be measurements and procedures that will be carried out by one individual. Have the other, perhaps working on lower energy circuitry nearby watch over and have clear access to an inhibit switch and a cap bank discharge mechanism.
13.) If you treat this work as a lineman would treat their work in 13kV mains, use shielding, inhibit switches, cap bank discharge switches, fusing and breakers to your advantage, and use proper PPE as a lineman would---the work isn't easier or faster, but it is maximally safe.

14.) Make certain OFF is OFF. Capacitors should be discharged, test fixture unplugged, LOTO installed and properly labeled on hard wired fixtures.

Disclaimer: the list above is my no means exhaustive. Please consult with your specific procedures, standards and directives on safe inverter design practices.

Conclusions

This work should provide useful guidance to selecting the appropriate module and designing the inverter or motor drive. Only after the complete design (including software and firmware) is validated under worst case conditions with the machine, line, temperature environment and dynamometer should the design be released to production. Keep loop area to a minimum by twisting leads tightly and or shielding. This will minimize noise transmission and noise pickup by measurement equipment.

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