Application Note AN-1185

A guide to the SBP5AS: A Radiation hardened DC to DC converter module

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Introduction
This Application Note should serve as a map for the use and application of the SBP converter module. It contains all of the critical parameters associated with each pin and some guidance as to how to set them up in the circuit.

Basic Topology
The SBP DC to DC converter is comprised of a voltage-mode control IC. Direct paralleling is not possible.

The converter is a synchronous buck converter capable of starting into a pre-bias condition. This is accomplished by a diode emulation mode built into the integrated controller that is active only during the startup condition. When a pre-bias startup condition is sensed, the controller turns off the lowside MOSFET thereby allowing the body diode of the device to block that current and not pull down the output voltage. Diode Emulation mode is not used at light, steady state loads in the SBP DC to DC converter in order to maintain the best possible transient response.
Output Adjust Pin:
The output voltage of the converter is settable between 0.8 and 3.3V. The resistor that sets this voltage, $R_{\text{Adjust}}$, can be calculated by one of two equations depending on whether or not remote sense is tied to the load or to the module output:

With Remote Sense pin tied directly to converter output:

$$R_{\text{Adjust}} = \frac{191.686}{31.600 \times \text{Vout} - 25.026} - 1210$$

With Remote Sense pin tied to the load:

$$R_{\text{Adjust}} = \frac{189.600}{31.600 \times \text{Vout} - 24.960} - 1210$$

If a final trim is used on the end equipment, $R_{\text{Adjust}}$ should be calculated from $1.035 \times \text{Vout}$ (output voltage is initially set 3.5% higher).

Note: For static load, output voltage can be 85% of the input voltage. For high load current variations the output voltage shall be limited to 75% of the input voltage. This is to obtain the dynamic performance without saturating the internal PWM controller.
**Regulation:**

Typical regulation for the SBP converter can be seen in figure 2.) below.

![3.3V, High input voltage](image1)

Figure 2a) Typical Regulation, Vin=9V

![3.3V, Low input voltage](image2)

Figure 2b) Typical Regulation, Vin=4.7V

**Output Voltage Ripple:**

Output ripple is caused by the ripple current in the output inductor flowing through the output capacitor and its Equivalent Series Resistance (ESR) and Inductance (ESL). The output ripple voltage without any external filter is approximately 10mV RMS.

The peak to peak ripple voltage is 38.7mV P-P with a 25MHz BW applied to the waveform. With an added LC filter of 20nH and 470uF with an ESR of 0.005Ω the ripple voltage drops to 15.7mV P-P with a 25 MHz filter applied.
Figure 3.) Output ripple with no external filter

Figure 4.) Output ripple with 20nH and 470uF, 0.005Ω external filter
Internal and External Compensation:

In terms of compensation, the internal inductor and capacitor contribute a double pole at roughly 5.63 kHz. The internal output capacitor has a zero at roughly 67.7 kHz. The error amplifier is compensated in a Type III compensation scheme with dominant poles at 0Hz and 225 kHz and zeros at roughly 0.5 kHz and 6.8 kHz. Combined with the gain of the internal error amplifier, this combination offers a 0dB crossover frequency of approximately 40 kHz. At this crossover frequency, the converter has between 70 and 90 degrees of phase margin depending on line, load and output voltage conditions.

The SBP DC to DC converter was designed with the unique ability to not only add optional capacitance to the converter and have it remain stable, but to add an additional low frequency gain to the converter and further improve the transient response with the added output capacitance. While the internal output capacitance in the SBP converter is sufficient for most applications, there are clearly instances where a lot of local capacitance is needed for locally bypassing high transient loads.

To compensate for additional output capacitance, a small external capacitor can be connected between the Sense and Output Adjust pins that will place an additional zero at low frequency and raise the gain of the control loop slightly to compensate for additional added output capacitance. The calculation of this added capacitance is included under the SENSE PIN heading.

Sense Pin

The SENSE PIN can be used to reduce the drop in the positive conductor that connects the converter to the load. In applications with a positive conductor longer than a few inches or contributing more than 1% I*R drop at maximum current, the sense pin should be connected as close to the load as possible. In applications with minimal conductor drop the sense pin should be connected to the output of the converter or it can be simply left open. The sense pin should NOT be shorted to return on the POL converter.

The compensation of the converter is designed for minimal perturbation by added parasitic components. However when filter capacitance is added to the output the loop performance can be improved slightly by the use of C adjust (Cadj), as described below. The addition of this component from the SENSE to the ADJUST pin adds a low frequency zero to the control loop offering slightly more gain in the feedback loop.

The maximum value of Cadj is determined by the external capacitance compared with the internal capacitance, and the external ESR compared with the internal ESR.

\[
C_{adj} \leq \frac{1.5nF}{k} \leq \frac{C_{out}}{470uF} \quad \text{and} \quad k \leq \frac{ESR_{out}}{5m\Omega}
\]
Load step performance
The Lout (40nH and 0.005Ω) of stray series inductance and DCR showed 32mV in voltage deviation on the filter output Cout (470μF and 0.005Ω). This corresponds to 10.6mΩ in output impedance. Cadj is 1.5nF.

Figure 6.) 3A load step, 1: V external filter, 2: V SBP output

Input Voltage Hysteresis
The input voltage hysteresis can be adjusted by and resistor placed from the Vin to Enable.

The resistor value can be found:

\[ R_{hys} = \frac{83.33k\Omega \cdot V_{hys}}{1 - 1.796 \cdot V_{hys}} \]

Where \( V_{hys} \) is the desired input voltage hysteresis.
The hysteresis is 0.557V with Rhys open circuit. \( V_{hys} \) can only be lowered by adding finite value of Rhys.

Input Start/Stop Voltage
A resistor connected from the ENABLE to GND sets the UVLO turn-off threshold voltage.
The resistor value can be found by:

\[ R_{stop} = \frac{V_{hys} \cdot 50k}{V_{stop} - 0.6V - 6.06 \cdot V_{hys}} \]

The UVLO turn-on threshold voltage is the UVLO turn-off threshold voltage plus the hysteresis \( V_{start} = V_{stop} + V_{hys} \)
The minimum UVLO turn-off threshold voltage is 3V
Input ripple current

The POL converter is designed to accommodate a wide variety of input conductors and wire harnesses for maximum design flexibility.

Calculation of the input ripple current is shown with an inductive harness. The input ripple current is the Thevenin voltage (22mVrms) divided by the harness impedance at the switching frequency. This gives the following with a 100nH to 2.5uH variation:

- 68 mArms which is 97dBuA for 100nH
- 14 mArms which is 83dBuA for 500nH
- 3 mArms which is 69dBuA for 2500nH

Sync Pin

Several POL converters can be connected to the same input supply. If several inputs are connected to an inductive source, mixing of the different switching frequencies will occur, creating a very low sub harmonic ripple on the output.

This can be prevented by adding a small inductance in series with the inputs and a capacitor in the common point. Further, one should pay close attention to resonances in the input wiring harness and capacitors.

Another way to prevent the intermodulation is to synchronize the converter to a common clock. This is accomplished by driving the SYNC PIN from an external clock. The synchronization frequency range is 425 KHz to 575 KHz. The synchronization signal source must be able to source the current of 1.0mA with the voltage level of minimum 2.0V at high and maximum 0.8V at low. The rise and fall times of the synchronizing waveform should be 0.2us or less respectively.

Parallel Enables

The Enable inputs of several SBPs can be paralleled. This can be done directly if there are no requirements for timing between the outputs. The only difference is that the Rstart / Rstop resistance is divided by 2 (number of paralleled SBPs).

Alternatively, timing can be altered by adding some resistance between the ENABLE pins and the combined Rstop resistor. This is done to stop the controlling converter first, to insure timing.

Soft start

The Soft start period can be modified by adding a capacitor from the TRACK pin to GND. The internal and external output capacitance needs to be charged during the soft start event. This charge current is added to the load current during start up, and the sum needs to be within the maximum current rating.

\[
t_{ss} = \frac{(C_{out, int} + C_{out, ext}) \cdot V_{out}}{I_{charge}}
\]

\[
C_{ext} = 39nF \cdot t_{ss} - 82nF
\]

tss is the soft start time in [ms].

The internal capacitance is 470uF.
**Power Good Pin to Sequence Multiple SBP modules**

Tracking is important in applications with different processor and or I/O voltages. The manufacturers will often recommend a startup sequence in these cases to mitigate any data contention. For repeatable operation, it is preferable to use the POWER GOOD pin as outlined below.

To rely on the Soft Start capacitance for tracking is not a recommended design practice. This is due to the tolerance of the soft start capacitor combined with the tolerance in the soft start circuit in the PWM controller in the SBP. The combination of these tolerances can result in worse than expected tracking performance.

**Sequence Type: Vout1 before Vout2**

The power good pin of the first output is connected to the enable of the second output. The second output will start to rise when the first output releases the power good, which approximately is 1.5 times the Soft start time. R200 controls the start/stop voltage, where R201 is more of a protection at very low input voltages (if converter 1 stops functioning before converter 2 – below 3V).
Sequence type: Ratiometric Tracking

Ratiometric tracking is when the outputs have the same percentage of their final output voltage during turn ON. Ratiometric tracking can be accomplished by connecting a voltage divider from the highest output voltage to the soft start pin of the lowest output voltage. The voltage divider shall be 0.6V / Vout1. The low side of the voltage divider must be connected to the power good of output 1.

\[ R_{207} = \frac{V_{out1}}{V_{ref}} \cdot 1k + 0.5k \]

\[ R_{206} = \frac{V_{ref}}{V_{out1} - V_{ref}} \cdot R_{207} \]

Figure 8.) Ratiometric Tracking Diagram

Vref is 0.6V.
Sequencing Type: Simultaneous tracking

Simultaneous tracking is when the output voltages rise at the same actual level. This can be accomplished by connecting a voltage divider from the highest output voltage to the soft start pin of the lowest output voltage.

The voltage divider shall be \( \frac{0.6V}{V_{out2}} \)

\[
R_{207} = \frac{V_{out2}}{V_{ref}} \cdot 1k + 0.5k
\]

\[
\Delta V_{out} = \frac{V_{out1}}{V_{out2}} \cdot I_{ss} \cdot R_{207}
\]

\[
R_{206} = \frac{V_{ref} + \Delta V_{out}}{V_{out2}} \cdot \frac{V_{ref} - \Delta V_{out}}{R_{207}}
\]

Vref is 0.6V. Iss is 23uA.
Efficiency

The measured data below shows the efficiency of the POL converter under best and worst case conditions. The efficiency curves are taken at -55, 22 and 115°C.

![Efficiency vs. Load Current for Vin=4.7V, Vout=3.3V](image1)

![Efficiency vs. Load Current for Vin=7V, Vout=1.2V](image2)

**Discussion of Losses:**

**Internal Switches:**

The temperature plots illustrate the Rs dependency of the MOSFETs in the regulator IC. At lower temperatures, the Rs of the MOSFETs is appreciably lower than at higher temperatures. At higher temperatures, the charge and discharge current to the output inductor cause more losses in the respective high and low side switches as a result of this higher resistance.
Assuming fixed input voltage, the lower voltage output requires a proportionally lower duty cycle on the high side switch. This means that the lowside switch is on for a proportionally longer duration and the freewheel currents cause more losses in this switch.

As the input voltage is raised, this condition gets worse in two ways. The lowside switch is clearly on for a longer duration with rising input voltage and the switching losses in the high side switch are exponentially greater as they are associated with the various CV2/2 energies in the switch capacitances.

**Output inductor:**

At narrow duty cycles (thereby lower output voltages), the AC losses in the output inductor are much worse than at larger duty cycles. This is due to the higher frequency energy associated with the narrow pulse causing additional eddy current losses in the core material and copper windings. The core material was chosen with this in mind as well as the rugged applications, temperature ranges and environments that the inductor will see.

**Input and Output Capacitor**

The primary loss mechanism in the capacitors stems from the RMS value of the AC ripple current flowing through the ESR of the capacitors. These losses are minimal in the SBP module.

**PCB traces**

The losses in the PCB traces are fairly straightforward. At 500 KHz the depth of penetration in copper is approximately 0.0042” or 4.2 mils. The copper on the PCB is slightly thinner than this so any additional AC losses beyond the I*R drop in a given trace is minimal. The PCB was well routed with plenty of cross section in the power path conductors to keep the DC losses to a minimum.

**Thermal Plot**

The thermal plot shows the hot spots in the module. The control IC is mounted on the top of the PCB with the output inductor mounted under the control IC on the bottom of the PCB. These are the major heat sources in the SBP module. The module is contained in an Aluminum housing assembled over the top and bottom of the PCB which helps conduct heat away from the control IC. The ambient temperature for the plot is 20°C.

![Module drawing](image)
Figure 13.) FEA based simulation of module thermals

**Mounting**

The POL must be mounted to a thermally conductive plate or chassis with four screws. Proposed screw size is M2 or UNC 1-72 and 12 mm (0.47") in length. A recommended torque is 0.25nm (35OzIn). The host chassis should be mechanically rigid and thermally conductive enough to support the mass and power loss. Typical power loss at full load is 3.5W, but can be smaller at a lighter load.

**Wiring**

The positive and negative conductors into and out of the module should have a cross section of at least 2500 circular mils. If Wire is to be used, use 16AWG or larger cross section wire. Twisted pair is strongly recommended.

**Conclusion**

This document should serve as an application resource for the use of the SBP POL Converter. We have tried to address every aspect of the application of the POL converter as well as the use of combined POL converters. Please refer to the datasheet for specific values and dimensions that may not be covered herein.