

Application Note AN-1132

Power Quad Flat Pack No-Leads (PQFN) Board Mounting Application Note

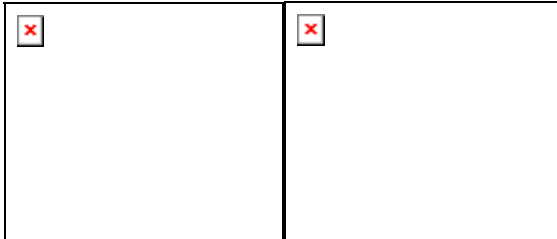
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The Power QFN is an efficient device with a wide range of input voltage in a small 5x6mm QFN package. This package is offered only as Lead-Free (PbF), identified by a PbF suffix after the part number (for example, IR3800PbF). The main text of this application note contains guidance applicable to Power QFN package. In Appendix A, there are device outlines, substrate layouts and stencil designs for Power QFN MCM. To simplify board mounting and improve reliability, International Rectifier manufactures Power QFN devices to exacting standards. These high standards have evolved through evaluating many different materials and designs. Although such evaluations have yielded good results, the recommendations in this application note may need to be adjusted to suit specific production environments.

Introduction

Power QFN[®] is a surface mount semiconductor technology designed primarily for board-mounted power applications. It eliminates unnecessary elements of packaging that contribute to higher inductance and resistance, both thermal and electrical, so that its power capabilities exceed those of comparably sized packages.



The main text of this application note contains guidance applicable to Power QFN MCM PbF. Then, in Appendix A, substrate layouts and stencil designs.

To simplify board mounting and improve reliability, International Rectifier manufactures Power QFN devices to exacting standards. These high standards have evolved through evaluating many different materials and designs. Although such evaluations have yielded good results, the recommendations in this application note may need to be adjusted to suit specific production environments.

Device construction

Power QFN devices are surface mount package type. This technology uses the current plastic molding technique with wire bond interconnects (*Figure 1*).

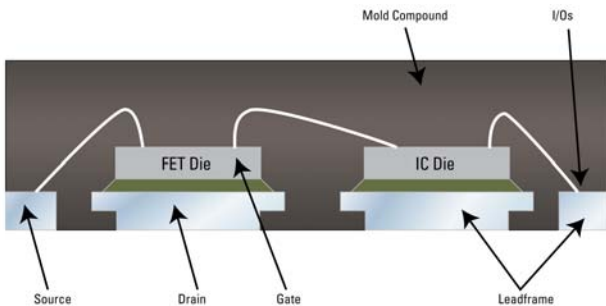


Figure 1 Sectional view

Figure 2 shows the contact configuration of the Power QFN MCM device. Specific pad assignments are shown in the data sheet for each product.

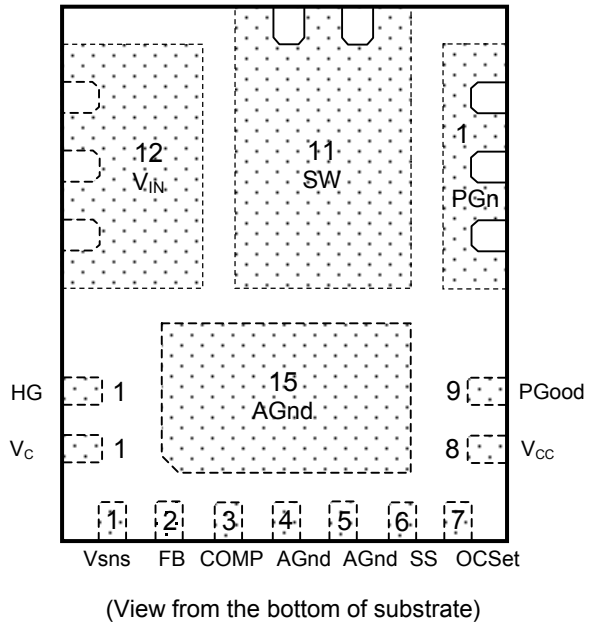


Figure 2 Power QFN MCM contact configuration

Figure 3 shows how Power QFN devices are labeled. Pin one is identified by the small dot. Part number, batch number and date code are provided to support product traceability.

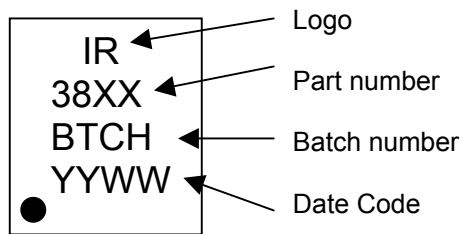


Figure 3 Device markings

Design considerations

Substrates

The Power QFN was originally developed and evaluated for use with epoxy glass-woven substrates (FR-4). The test substrates were finished in Organic Solderability Preservative (OSP), but any of the numerous surface finishes available are suitable.

The substrate finish can affect the amount of energy required to make solder joints; this can in turn be a factor in solder quality issues such as solder balling, tombstoning (or tilt) and the formation of voids.

Substrate designs

To achieve low-loss track layouts, Power QFN devices were designed for use with layouts that are solder-mask-defined (SMD) for the pad lands (Appendix A, Substrate/PCB Layout) and non-solder-mask-defined (NSMD) for the lead lands (Appendix A, Substrate/PCB Layout). The devices were also evaluated with entirely NSMD layouts. The outline of Power QFN devices and the use of solder-mask-defined pads contribute to efficient substrate design. Large-area tracks optimize electrical and thermal performance.

If pad numbering is required to produce a component outline within the library of a CAD system, International Rectifier recommends that the conventions shown in **Figure 4** and **Table 1** are adopted. This makes it easier to discuss any issues that may arise during design and assembly.

Power QFN devices can be placed in parallel using simple layouts (**Figure 4**). International Rectifier recommends a minimum separation of 0.500mm (0.020"). The separation can be adjusted to reflect local process capabilities but should allow for rework. Micro-screen design and desoldering tool type may affect how closely devices are placed to each other and to other components.

Refer to Appendix A for device outlines, substrate layouts and stencil designs for each package size and device outline in the Power QFN range.

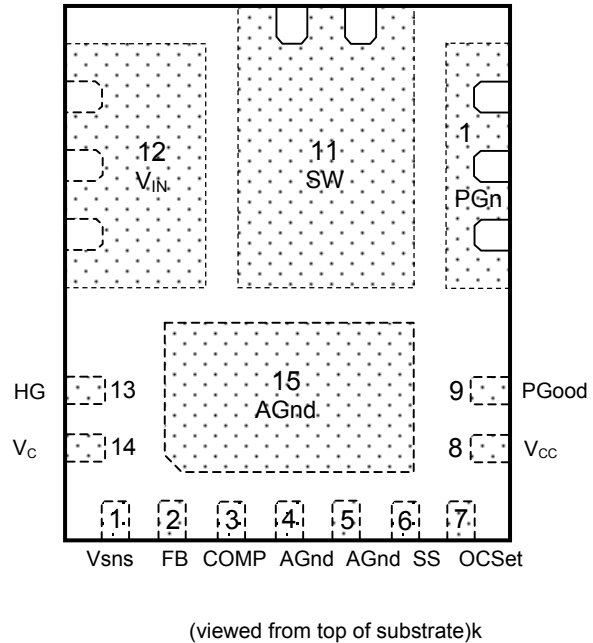


Figure 4 Recommended pad numbering

Pin	Name	Pin	Name
1	Vsns	9	Fb
2	Fb	10	PGnd
3	Comp	11	SW
4	AGnd	12	V _{in}
5	AGnd	13	HG
6	SS/SD	14	V _c
7	OCSet	15	AGnd
8	V _{cc}		

Table 1 Names of Pins on Power QFN

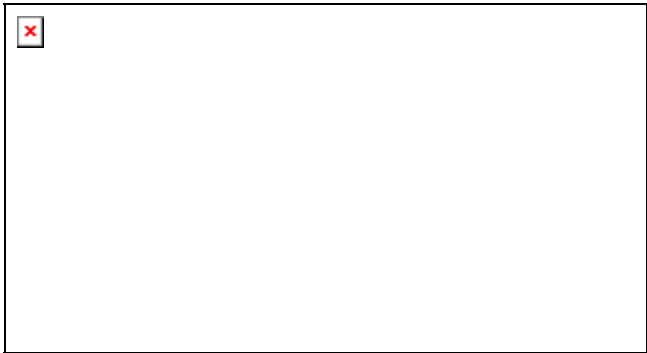


Figure 5 Placing PQFN Devices in parallel

2nd Level Assembly Considerations

International Rectifier designed Power QFN devices to be as easy as possible to assemble using standard surface mounting techniques. However, procedures and conditions can have a profound influence on assembly quality. It is therefore necessary to develop an effective process based on the individual requirements for the application.

Packaging

Power QFN devices are supplied in tape and reel format (*Appendix B*).

Storage requirements

Power QFN devices on tape and reel are packed in sealed, nitrogen-purged, antistatic bags. The sealed bags provide adequate protection against normal light levels but it is prudent to avoid prolonged exposure to bright light sources. The bags also provide protection from the ambient atmosphere. Devices in sealed, unopened bags have a shelf life of 1 year. Once a bag has been opened, its contents should be treated as Moisture Sensitivity Level 2 devices, as shown on the packaging labeling, to guarantee good solderability.

International Rectifier recommends that, when not in use, reels of devices should be resealed into the protective bags in which they were supplied.

Solder pastes

International Rectifier evaluated different types of solder paste from various manufacturers. The properties of pastes vary from manufacturer to manufacturer, meaning that some perform better than

others. In general, high slumping pastes tend to suffer more from solder balling than slump-resistant pastes; solder balling is discussed in the next section on stencil design. In addition, some pastes appear to be more prone to voiding than others.

Solder alloys, metal contents and flux constituents all influence the rheology of the solder paste. This in turn influences how the paste reacts during processing. The assembly and board-level reliability of the Power QFN package have only been evaluated using lead-free pastes (Sn96.5 Ag3.0 Cu0.5). [c1]

Evaluations of lead-free devices used a reflow profile that conforms to IPC/JEDEC standard J-STD-020C (July 2004 revision). As devices may be subjected to multiple reflows when PCBs are double-sided or reworked, the evaluations used up to three reflows. International Rectifier recommends that customers should conform to J-STD-020C in setting reflow profiles and should not exceed three reflows.

Stencil design

The stencil design is instrumental in controlling the quality of the solder joint. Appendix A shows stencil designs that have given good results with the recommended substrate outlines. These are based on reductions of 25% for the pad lands (Appendix A, Substrate/PCB Layout) and 20% for the lead lands (Appendix A, Substrate/PCB Layout) equivalent to printing 75% and 80% of the area respectively using a stencil thickness of 0.125mm (0.005"). The design should be revised for other stencil thicknesses.

Stencils for Power QFN can be used with thicknesses of 0.100-0.250mm (0.004-0.010"). Stencils thinner than 0.100mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125mm-0.200mm (0.005-0.008"), with suitable reductions, give the best results.

Post-reflow evaluations can help to assess how a stencil is performing within a given process. Two main problem areas can be addressed by improving stencil design:

- **Solder balling around the perimeter of the die.** This can be caused by too much solder paste, in which case the stencil might need to be reduced by more than 25%. The reduction can be symmetrical but biasing it unevenly may help to prevent solder balling; the stencil designs in Appendix A have apertures moved further from the die edge for this reason. Solder balling can result from other external factors, such as the moisture content of the board and incorrect ramp rates or insufficient soak times in the reflow profile. Leadless packages like Power QFN can sometime accentuate existing deficiencies within a process.
- **Misshapen joints.** If the joints are smaller or seem to be only partially made, this might suggest that there is insufficient solder to make the joint. If, however, the joints have what appear to be additional areas extending from their edges, they are usually the result of too much solder; this almost certainly the case if solder balls are also present. Insufficient solder can also cause voiding but this is more likely to arise from other factors, including surface finish, solder paste and substrate condition.

Device placement

Inaccurate placement may result in poor solder joints or in devices being tilted and/or misaligned. Ideally, the Power QFN should be placed to an accuracy of 0.050mm on both X and Y axes but, during evaluations, devices centered themselves from placement inaccuracies of more than 0.300mm.[c2] Self centering behavior is very solder and process dependant and experiments should be run to confirm the limits of self centering on specific processes.

Reflow equipment

Power QFN devices are suitable for assembly using surface mount technology reflowing equipment and are recommended for use with convection, vapor phase and infrared equipment. PbF qualified devices have a good resistance to short-term exposure to high temperatures, making them suitable for reflow profiles of up to 260°C (measured by attaching a thermocouple to a Power QFN device).

There are no special requirements for successful assembly, but all reflow processes used in evaluation and qualification complied with the recommendations of solder paste suppliers. Using incorrect reflow profiles can cause solder quality issues such as solder balling, tombstoning (or tilt) and the formation of voids;

if such problems arise, the reflow profile should be checked.

The Power QFN package is designed to have superior thermal resistance properties. For this reason, it is essential that the core of the substrate reaches thermal equilibrium during the pre-heating stage of the reflow profile to ensure that adequate thermal energy reaches the solder joint.

Inspection

For comprehensive information on inspecting board-mounted Power QFN devices, refer to the Power QFN Inspection Application Note (AN-1133).

As with all QFN packaging, the best way to inspect devices after reflow is through a combination of visual inspection of the peripheral solder joints and X-ray imaging of the connections directly under the package.

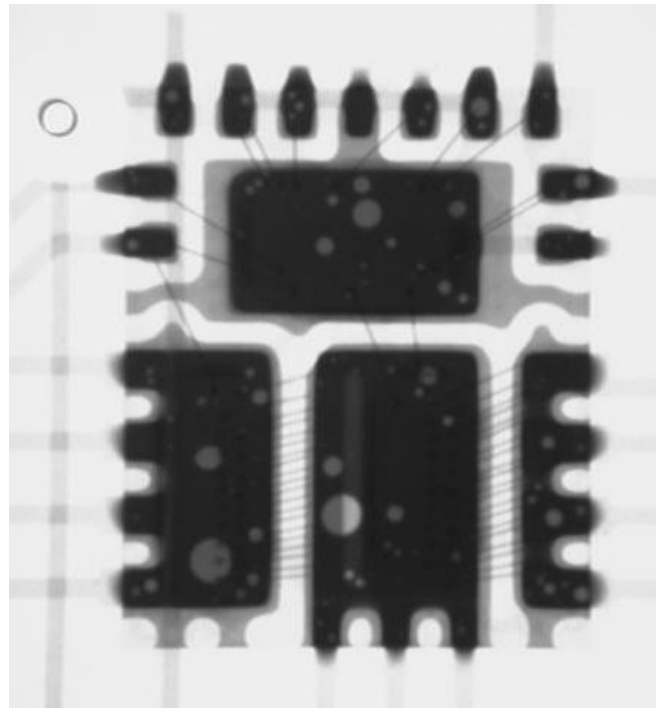


Figure 8 X-rays of Power QFN

Figure 8 shows an X-ray image of a board-mounted Power QFN device shows solder joints, alignment, and voids. The amount of voids in *Figure 8* is acceptable.

Rework guidelines

Modern rework stations for ball grid array and leadless packages often use two heating stages. The first heats the substrate, either with a conventional hot-plate or a hot-air system. The second stage uses a hot-air system for localized heating, often with the option of unheated air for faster cooling of the solder interconnections on the replaced device; this improves the solder grain structure.

The device placement mechanism or arm usually has a hot-air de-soldering gun as part of the pick head, equipped with a vacuum cup and thermocouple. Once the solder reflow temperature has been reached, the vacuum is automatically engaged to allow the device to be removed from the substrate. This reduces the risk of causing damage by premature removal.

The objective of rework is to remove a non-functional part and replace with a good part. International Rectifier does not recommend reusing devices removed from a substrate. When pulling out the Power QFN, take care to not compromise the existing failure in order to allow subsequent failure analysis.

To replace a Power QFN device:

Note: If you usually bake to remove residual moisture before rework, insert your normal procedure here.

1. Heat the site to approximately 100°C using the substrate heating stage. This reduces the amount of heating required from the hot-air de-soldering tool, which in turn reduces the risk of damaging either the substrate or surrounding components.
2. Lower the placement arm to bring the de-soldering tool into contact with the device. When the device and the solder interconnects reach reflow temperature, lift the placement arm to remove the device from the substrate.
3. Clear residual solder and flux from the site with a blade-type de-soldering tool and de-soldering braid. Take care in cleaning the site: damage to the solder-resist may produce undesirable results. When the site is ready, apply new solder paste with a micro-screen and squeegee.
4. Heat the site to approximately 100°C using the substrate heating stage. Position the new device with the placement arm and then use the de-soldering tool to heat both device and solder interconnects to reflow temperature. Retract the arm, leaving the device in place. Cool as quickly as possible to achieve good grain structure in the new joint.

Mechanical test results

International Rectifier has subjected board-mounted Power QFN devices to extensive mechanical tests, conducted in accordance with industry standards and practices. The package tested were 5x6mm Power QFN MCM. Given that all Power QFN devices are made in the same way, other Power QFN MCM devices should perform to the same high standard.

This section contains summarized results for bend tests, drop tests and vibration tests. Full reports are available on request.

Bend tests

Method

Cycling bend testing was carried out in accordance with JEDEC JESD22B113, Board Level Cyclic Bend Test Method for Interconnect Reliability Characterization of Components for Handheld Electronic Products.

Boards were designed as specified in JESD22B113 with nine Power QFN parts per board. Board thickness was maintained to 0.030" (0.75 mm). The span of the support anvils was 110mm and the span of the load anvils was 75mm. The sinusoidal load was cycled at 3Hz with a 2mm displacement. Boards were cycled for 200,000 cycles.

Results

The results from cyclic bend testing are displayed in *Figure 12*. It is important to note that no qualification requirements are imposed in JESD22B113. As stated in the specification, "The test duration of 200,000 cycles should not be construed as an expectation of reliability; it is only a recommendation to get enough component failures to generate a valid probability failure plot or to limit the duration of testing. The reliability requirements should be separately determined between the supplier and customer." In some respects, the Power QFN can be considered relatively robust as fewer than 60% of the components, as called out in JESDB113, failed before the test limitation of 200,000 cycles.

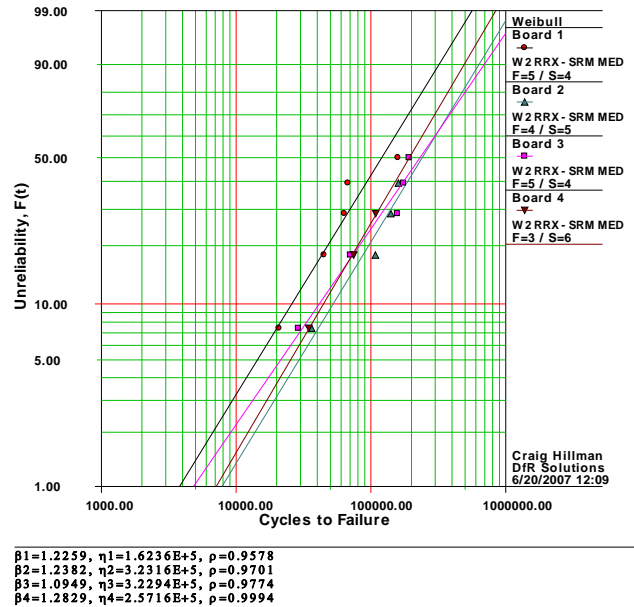


Figure 12 Results from bend cycling of Power QFN

Drop tests

Method

Drop testing was carried out in accordance with JEDEC JESD22B111, Board Level Drop Test Method of Components for Handheld Electronic Products.

Boards were designed as specified in JESD22B111 with fifteen Power QFN parts per board. Board thickness was maintained to 0.030" (0.75 mm). The populated assemblies weighed 22 g. The calibrated acceleration was 1500Gs, 0.5 millisecond duration, half-sine pulse which resulted from a 15.5" drop onto a steel block. *Figure 12* shows the shock pulse. Each drop was measured with an accelerometer. Each board was dropped 30 times.

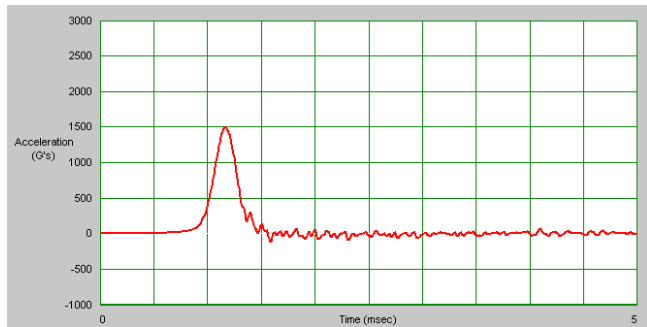


Figure 13 Shock pulse for shock test

Results

There were no failures on the 60 tested Power QFN parts.

Vibration tests

Method

Vibration testing was carried out as per MIL-STD-810F (Method 514, Proc I, Cat. 20 – composite wheeled vehicle). The board design used in vibration testing was equivalent to the design specified in JEDEC JESD22B111, with fifteen Power QFN parts per board. A total of four boards were subjected to vibration testing.

The Power QFN boards were subjected for four hours to random vibration from 5Hz to 500Hz, experiencing

1.9g_{rms} (18.6ms⁻²_{rms}) with an acceleration spectral density value of 0.005g²Hz⁻¹ ([0.48ms⁻²]²Hz⁻¹). *Figure 13* shows the bandpass filter frequency chart.

Based on experience with the interconnect failure behavior of similar packages, the devices were only subjected to out-of-plane loading (Z-direction). The test is a pass-fail test and the Power QFN devices were tested after the vibration was completed.

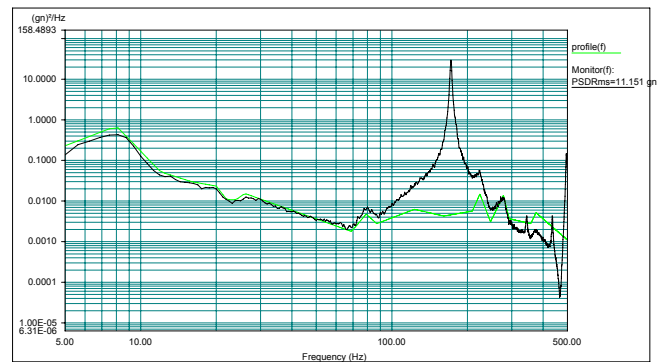


Figure 14 Bandpass filter frequency chart

Results

60 devices were tested and there were no failures.

Acknowledgements

International Rectifier would like to thank:
DfR Solutions for providing the required studies needed to develop
the substrate/PCB layout, solder resist and stencil designs.

Standards

MIL-STD-810F Method 514 Proc. 1.Random Vibration
JEDEC JESD22B111 Board Level Drop Test
JEDEC JESD22B113 Board Level Cyclic Bend Test

Appendix A

Model-specific data

This appendix contains the following information about 5x6mm Power QFN MCM and device outline currently available:

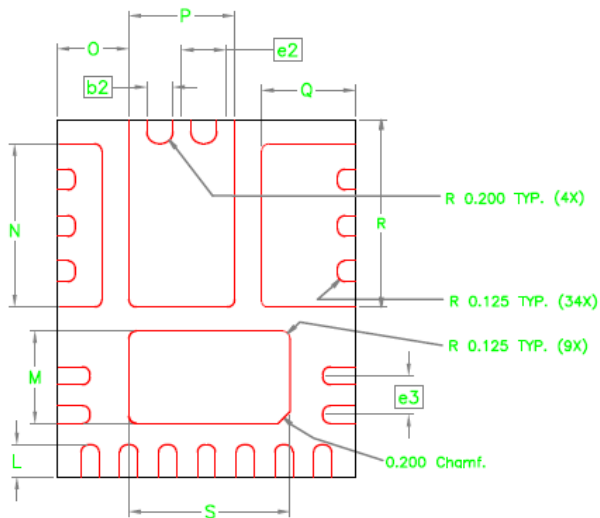
- Device outline drawing
- Recommended substrate/PCB layout
- Suggested designs for stencils of 0.125mm (0.005") thickness

For more details about individual devices, and to find out their size and outline, refer to the relevant product data sheet.

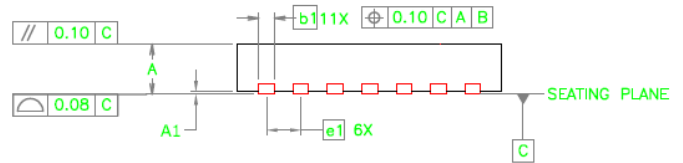
Appendix A.1 5.6mm PQFN MCM-outline

Package outline

Figure A.1.1 shows the package outline for Power QFN MCM device. The relative pad positions are controlled to an accuracy of $\pm 0.050\text{mm}$. For full dimensions and tolerances of each device, and to find out its size and outline, refer to the relevant product data sheet and package outline drawing.



(dimensions in mm)



Outline PQFN 5x6 D				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.000	.0315	.0394
A1	0.000	0.050	.0000	.0020
b	0.375	0.475	.0148	.0187
b1	0.250	0.350	.0098	.0138
b2	0.388	0.488	.0153	.0192
c	0.203	REF.	.0080	REF.
D	5.000	BASIC	.1969	BASIC
E	6.000	BASIC	.2362	BASIC
e	0.775	BASIC	.0305	BASIC
e1	0.650	BASIC	.0256	BASIC
e2	0.738	BASIC	.0291	BASIC
e3	0.650	BASIC	.0256	BASIC
L	0.500	0.600	.0197	.0236
M	1.500	1.600	.0591	.0630
N	2.700	2.800	.1063	.1102
O	1.150	1.250	.0453	.0492
P	1.725	1.825	.0679	.0719
Q	1.525	1.625	.0600	.0640
R	3.100	3.200	.1220	.1260
S	2.650	2.750	.1043	.1083

Figure A.1.1 PQFN MCM-outline package outline

Substrate/PCB layout

Lead lands (the 11 IC pins) width should be equal to nominal part lead width. The minimum lead to lead spacing should be $\geq 0.2\text{mm}$ to minimize shorting.

Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large and inspectable toe fillet.

Pad lands (the 4 big pads other than the 11 IC pins) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than 0.17mm for 2 oz. Copper; no less than 0.1mm for 1 oz. Copper and no less than 0.23mm for 3 oz. Copper.

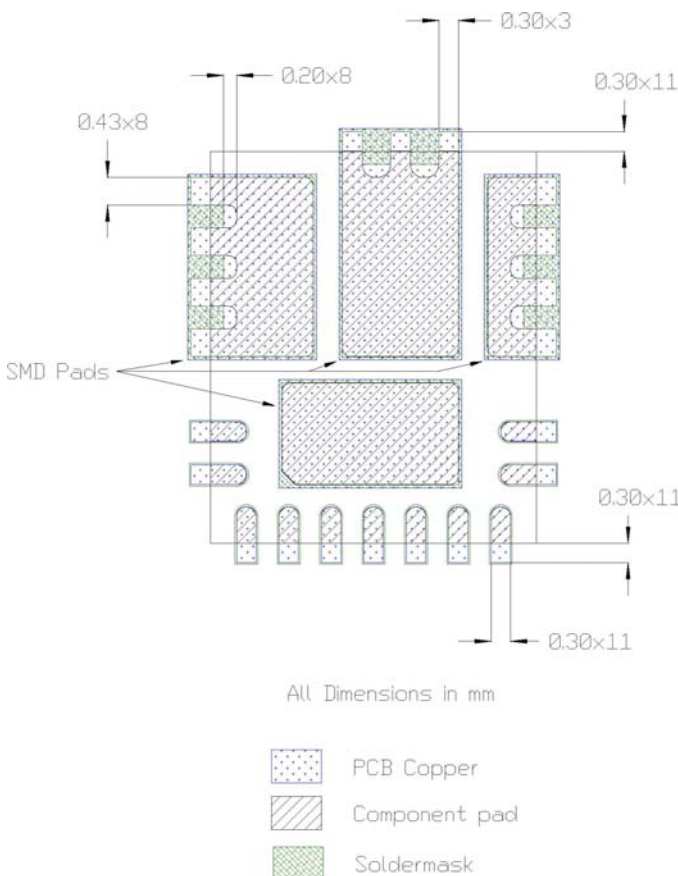


Figure A.1.2(a) PQFN MCM-outline substrate/PCB layout

Solder Resist

A typical solder resist application may have Non Solder Mask Defined (NSMD) lead lands and Solder Mask Defined (SMD) land pads. NSMD provides the maximum tolerance for misalignment of the leads and control of the land pad dimensions. Using SMD on the land pads is not required and may be eliminated to provide compatibility with existing processes.

For an NSMD process, it is recommended that the solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

For an SMD process, it is recommended that the solder mask be applied with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist mis-alignment.

Ensure that the solder resist in-between the lead lands and the pad land is $\geq 0.15\text{mm}$ due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

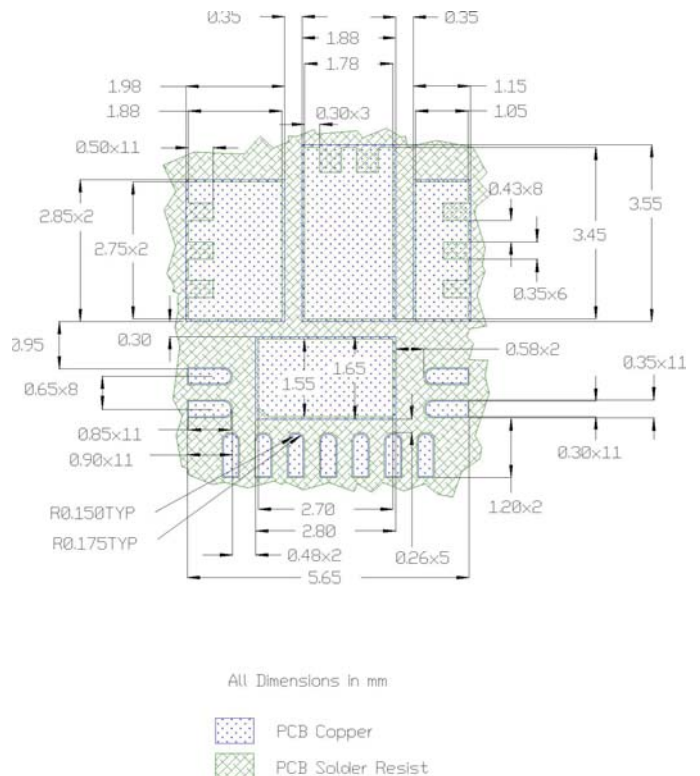


Figure A.1.2(b) PQFN MCM-outline Solder mask layout

Stencil design

The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will be open.

The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste. Land pad stencil should be approximately 75% of the area of the land pads.

Figure A.1.3 shows a typical stencil design following these rules and using a stencil thickness of 0.125mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

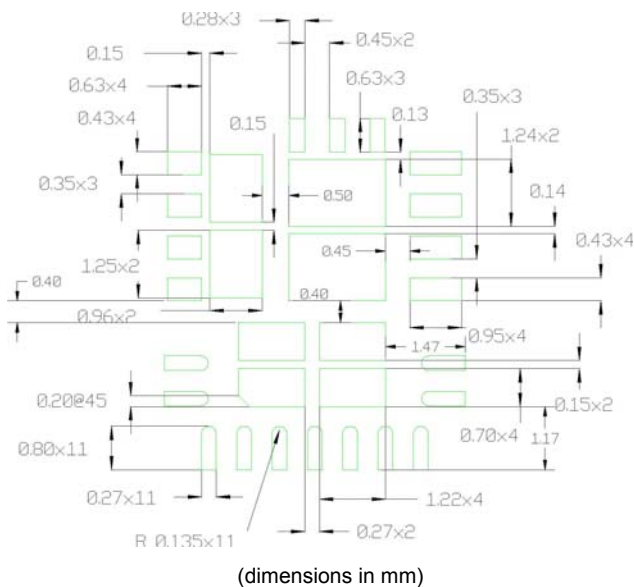


Figure A.1.3(a) PQFN MCM-outline stencil design

Appendix B

Tape & Reel Design

This appendix contains the Tape & Reel design that is currently being used for MCM Power QFN.

