Application Note AN-1089

IRS2136xD and IR2136x Series Comparison

By Andrea Merello, David New

Table of Contents

Introduction

The IRS2136xD is a new family of products that can replace the IR2136x family advantageously by providing functionality improvements, some of which will results in system-level cost savings (e.g., integration of the bootstrap network). These two families are based on the same core design and are pin-to-pin compatible, allowing minimal changes to the previous design. This application note describes the various differences between the existing IR2136x IC family and the new IRS2136xD family, and provides helpful information for adopting the new IRS2136xD HVICs into existing designs.

Family Description and Definition

The IRS213(6, 62, 63, 65, 66, 67, 68) HVICs are high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications.

Proprietary HVIC technology enables rugged monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3 V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an over-current or undervoltage shutdown has occurred.

Over-current fault conditions are cleared automatically after a delay (which is programmed externally via an RC network connected to the RCIN input). The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V.

The new IRS2136xD family introduces some parameter changes. In particular this family features a high voltage bootstrap FET that enables the use of these gate drivers without the external bootstrap network to supply the floating gate driver sections. Table 1 summarizes the main characteristics of the members of IRS2136xD family. A detailed parameter description/comparison of the two families follows after a block diagram comparison.

Part	IRS2136D	IRS21362D	IRS21363D	IRS21365D	IRS21366D	IRS21367D	IRS21368D
Input Logic	$\overline{\text{HIN}}$, $\overline{\text{LIN}}$	HIN, $\overline{\text{LIN}}$	$\overline{\text{HIN}}$, $\overline{\text{LIN}}$	$\overline{\text{HIN}}$, $\overline{\text{LIN}}$	$\overline{\text{HIN}}$, $\overline{\text{LIN}}$	$\overline{\text{HIN}}$, $\overline{\text{LIN}}$	$\overline{\text{HIN}}$, $\overline{\text{LIN}}$
t_{on} (typ.)	530 ns (1)	530 ns (1)	530 ns (1)	530 ns (1)	200 ns	200 ns	530 ns (1)
t_{off} (typ.)	530 ns (1)	530 ns (1)	530 ns (1)	530 ns (1)	200 ns	200 ns	530 ns (1)
V_{IH} (min.)	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V
V_{IL} (max.)	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V	0.8 V
V_{ITRIP+}	0.46 V	0.46 V	0.46 V	4.3 V	0.46 V	4.3 V	4.3 V
V_{CCUV+} / V_{BSUV+}	8.9 V	10.4 V	11.1 V	11.1 V	11.1 V	11.1 V	8.9 V
V_{CCUV-} / V_{BSUV-}	8.2 V	9.4 V	10.9 V	10.9 V	10.9 V	10.9 V	8.2 V

(1) Features a redesigned input filter. Please see page 6 for details.

Table 1: IRS2136xD Summary Table

Block Diagrams

The IR2136, IR21363 and IR21365 share the same block diagram (presented on page 6 of the IR2136x datasheet available at www.irf.com). The IRS2136D, IRS21363D and IRS21365D block diagram is shown in Fig. 1. The only visible difference is represented by the "Integrated BS Diode" block that applies to all new versions.

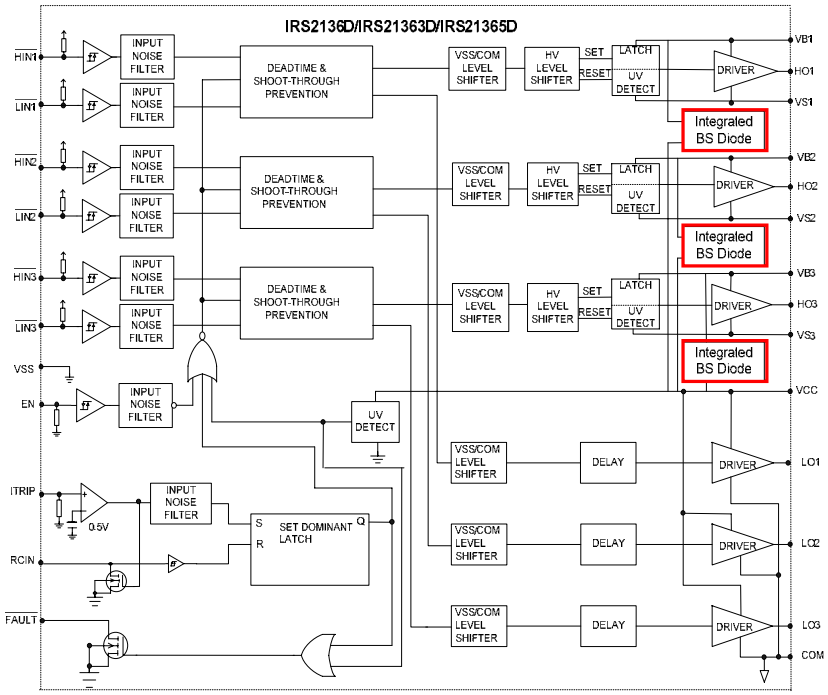

Figure 1: IRS2136D, IRS21363D, IRS21365D Block Diagram

The same considerations apply for the other block diagrams of the two families with one exception. Both the IR21368 and IRS21368D do have the "input filter" block after the HIN/LIN Schmitt triggers as shown in the IRS21368D datasheet on page 13.

The IRS2136xD datasheet addresses the internal bootstrap FET working principle and is documented in the application section. Its equivalent series resistance is mentioned the "Static Electrical Characteristics" section and is reproduced here is Table 2.

Symbol	Definition	Min	Typ	Max	Units
R_{BS}	Internal BS diode R_{ON}	—	200	—	Ω

Table 2: R_{BS} Specification

The integrated bootstrap MOSFET is turned on only during the time when LO is 'high', and has a limited source current due to R_{BS}. The VBS voltage will be charged each cycle depending on the on-time of LO and the value of the CBS capacitor, the DS/CE drop of the external MOSFET/IGBT or the low side free-wheeling diode drop.

In sinusoidal or space vector modulated configurations, the integrated bootstrap diode can replace the external bootstrap network. Limitations may apply for long periods of PWM duty cycle close to 100%. Six step based control schemes still need an external bootstrap diode and resistor to function properly.

Datasheet Changes

Absolute Maximum Ratings:

The absolute maximum ratings for V_B-V_S, V_{cc}-COM, V_{cc}-V_{ss}, LO-COM and HO-V_s of the IRS2136xD family are shown in Table 3. The maximum allowable DC supply has changed from 25 V to 20 V for V_{CC} to V_{SS} and for V_B to V_S, while V_{CC} to COM remains 25 V. The recommended operating voltage of the two families remains the same (20 V). The IRS2136xD series embeds a clamp structure on the supply pins capable of cutting fast and low-power spikes that may be dangerous for the IC.

Recommended Operating Conditions:

The recommended operating conditions of the two families have remained unchanged. Note 1 on page 2 of the IR2136xD datasheet has been changed in the IRS2136xD datasheet. The IRS2136xD Note 1 shows an important improvement of DC operation under negative Vs condition.

IR2136x Note 1: Logic operational for V_S of COM -5 V to COM +600 V. Logic state held for V_S of COM -5 V to COM – V_{BS}.

IRS2136xD Note 1: Logic operational for V_S of COM-8 V to COM +600 V. Logic state held for V_S of COM-8 V to COM – V_{BS}.

Symbol	Definition	Min.	Max.	Units
V_S	High side offset voltage	$V_{B\,1,2,3}$ - 20	$V_{B\,1,2,3}$ + 0.3	V
V_B	High side floating supply voltage	-0.3	625	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25	
V_{SS}	Logic ground	V_{CC} - 20	V_{CC} + 0.3	

Table 3: IRS2136xD Absolute Maximum Extraction

Static Electrical Characteristics (Inputs Thresholds):

The input thresholds shown in Table 4 have been added to the new IRS2136xD datasheet. Input thresholds refer to HIN and LIN inputs.

Additionally, the IRS2136xD family features improved logic threshold values for higher signal to noise rejection at the inputs. Previously, most of the IR2136x HVICs were specified as V_{IH} = 3.0 V; all of the IRS2136xD HVICs are specified as V_{IH} = 2.5 V.

Symbol	Definition	Min	Typ	Max	Units
V_{IH}	Logic "0" input voltage $\overline{LIN1,2,3}$ / $\overline{HIN1,2,3}$ IRS213(6, 63, 65, 66, 67, 68)D Logic "1" input voltage $\overline{LIN1,2,3}$ / HIN1,2,3 IRS21362D	**2.5**	—	—	V
$V_{IN,TH+}$	Input positive going threshold	—	1.9	—	
$V_{IN,TH-}$	Input negative going threshold	—	1	—	

Table 4: IRS2136xD Inputs Thresholds

Static Electrical Characteristics (Undervoltage Thresholds):

The new design introduced a small variation in the undervoltage thresholds for three of the IRS213(63, 65, 66, 67)D parts. The variations are small (a decrease of 0.2 V for the minimum specifications) and likely will not cause any issues for most applications; Table 5 shows the IRS213(63, 65, 66, 67)D values.

Symbol	Definition	Min	Typ	Max	Units
V_{CCUV+} / V_{BSUV+}	V_{CC} supply undervoltage positive going threshold	**10.4**	11.1	11.6	V
V_{CCUV-} / V_{BSUV-}	V_{CC} supply undervoltage positive going threshold	**10.2**	10.9	11.4	V

Table 5: UVLO Thresholds for IRS213(63, 65, 66, 67)D

Static Electrical Characteristics (V_{CC} Supply Bias Current):

The integrated bootstrap feature requires additional bias current; current consumption has increased as shown in Tables 6 and 7. The small increase of current should not cause difficulties for most applications.

Symbol	Definition	Min	Typ	Max	Units	Symbol
I_{QCC}	Quiescent V_{CC} supply current	—	**1.6**	**2.3**	mA	all inputs @ logic 0 value

Table 6: IR2136x V_{CC} Quiescent Current

Symbol	Definition	Min	Typ	Max	Units	Symbol
I_{QCC}	Quiescent V_{CC} supply current	—	**3**	**4**	mA	all inputs @ logic 0 value

Table 7: IRS2136xD V_{CC} Quiescent Current

Static Electrical Characteristics (Input Clamps):

The input clamp specifications of the two families are compared in Tables 8 and 9. When a current limiting resistor is already present in the application, this higher variation in the clamp voltage will not affect the inverter design.

Symbol	Definition	Min	Typ	Max	Units	Symbol
$V_{IN,CLAMP}$	Input clamp voltage (HIN, LIN, ITRIP and EN)	**4.9**	5.2	**5.5**	V	I_{IN}=100 µA

Table 8: Input Clamp Voltage IR2136x

Symbol	Definition	Min	Typ	Max	Units	Symbol
$V_{IN,CLAMP}$	Input clamp voltage (HIN, LIN, ITRIP and EN)	**4.8**	5.2	**5.65**	V	I_{IN}=100 µA

Table 9: Input Clamp Voltage IRS2136x

Static Electrical Characteristics (Inputs Leakage):

In order to measure the leakage current due only to the pull-up or pull-down resistors connected to the input pins and keep the input clamp inactive during such a test, the V_{in} test condition has been changed from 5 V to 4 V. For this reason, the IRS2136xD current absorption is reduced when compared to the IR2136x family.

Dynamic Electrical Characteristics (Input Filters and Propagation Delays):

One of the major changes introduced by the new IRS2136xD HVIC family is the redesigned input filters. The new input filters provide lower pulse distortion and better spike noise rejection as well as short pulses rejection. The input filters have been applied to the HIN and LIN inputs as well as the EN (enable) pin. The working principle of new filters is shown in Fig. 2.

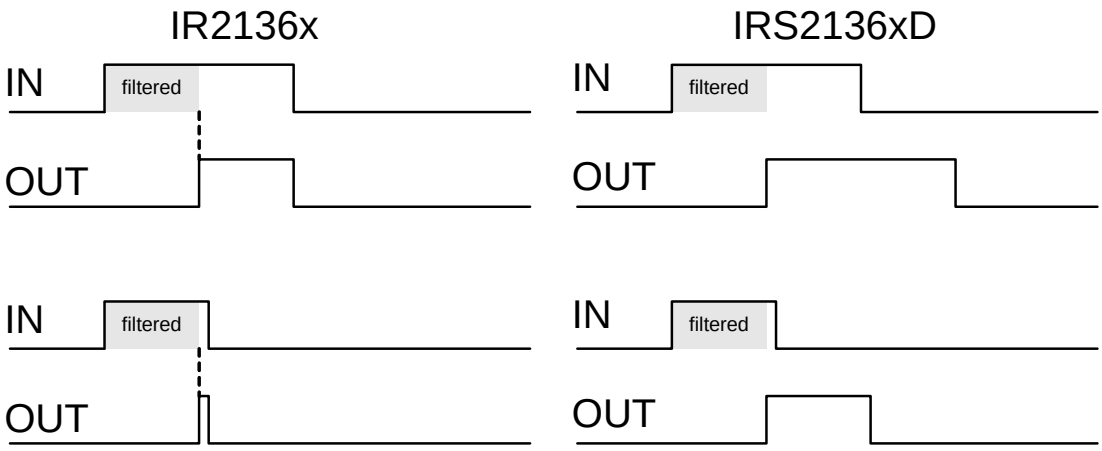

Figure 2: Input Filters Comparison

The input filter characteristics are shown in Figs. 3 and 4 for narrow on (short positive pulse) and narrow off pulses (short negative pulse). The new IRS2136xD input filter is the cause of the increased propagation delays (i.e., t_{on} and t_{off}).

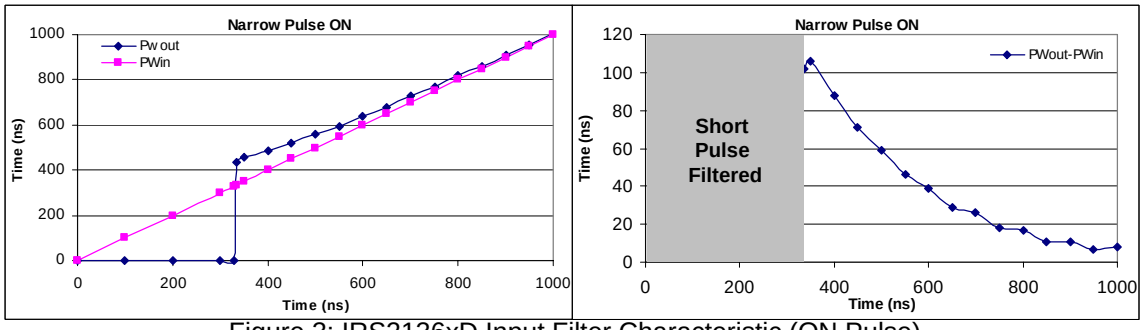

Figure 3: IRS2136xD Input Filter Characteristic (ON Pulse)

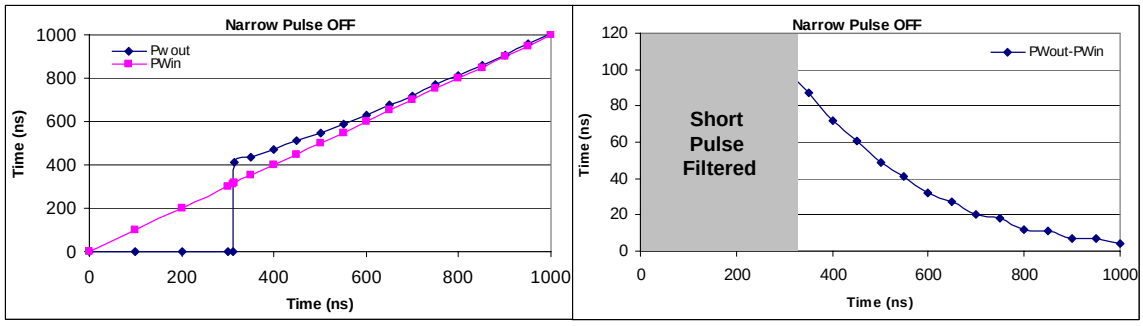

Figure 4: IRS2136xD Input Filter Characteristic (OFF Pulse)

It should be noticed that with the IRS2136xD family, the t_{on} and t_{off} propagation delays are equal, allowing very low pulse width distortion for long pulses. Additionally, matching delay time decreased 50 ns max. Tables 10 and 11 show the propagation delay differences specified in the IR2136x and IRS2136xD datasheets. For the gate drivers which do not have input filters (i.e., IRS21366D and IRS21367D), the propagation delay times (t_{on} and t_{off}) have been reduced and allow lower pulse width distortion.

The minimum HIN pulse width has changed from 1 µs to 500 ns (as shown in the following note) to allow higher PWM control. This change in the specification may affect applications where the controller takes actions related to propagation delays.

IR2136x Note: For high side PWM, HIN pulse width must be ≥ **1000 ns**

IRS2136xD Note: For high side PWM, HIN pulse width must be ≥ **500 ns**

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	300	425	550	ns	V_{IN} = 0 V & 5 V
t_{off}	Turn-off propagation delay	250	400	550		
t_{on} (66, 67)	Turn-on propagation delay	—	250	—		
t_{off}(66, 67)	Turn-off propagation delay	—	180	—		
t_{EN}	ENABLE low to output shutdown propagation delay	300	450	600		V_{IN}, V_{EN} = 0 V or 5 V
t_{EN} (66, 67)	ENABLE low to output shutdown propagation delay	100	250	400		V_{IN}, V_{EN} = 0 V or 5 V
t_{FILIN}	Input filter time (HIN, LIN) (IRS213(6, 62, 63, 65, 68)D only)	100	200	—		V_{IN} = 0 V & 5 V
MT	t_{on}, t_{off} matching time	—	40	75		Ext. deadtime >400 ns

Table 10: Propagation and Filter Timing (IR2136x)

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	400	530	750	ns	V_{IN} = 0 V & 5 V
t_{off}	Turn-off propagation delay	400	530	750		
t_{on} (66,67)	Turn-on propagation delay	—	200	—		
t_{off}(66,67)	Turn-off propagation delay	—	200	—		
t_{EN}	ENABLE low to output shutdown propagation delay	350	460	650		V_{IN}, V_{EN} = 0 V or 5 V
t_{EN} (66, 67)	ENABLE low to output shutdown propagation delay	—	300	—		V_{IN}, V_{EN} = 0 V or 5 V
t_{FILIN}	Input filter time (HIN, LIN) (IRS213(6, 62, 63, 65, 68)D only)	200	350	510		V_{IN} = 0 V & 5 V
MT	t_{on}, t_{off} matching time (on all six channels)	—	—	50		Ext. deadtime >420 ns

Table 11: Propagation and Filter Timing (IRS2136xD)

Dynamic Electrical Characteristics (Deadtime):

Deadtime tolerances have increased. The min/max values add additional margins and should not cause problems to existing designs. Deadtime matching

has improved from 70 ns to 60 ns for the new family; this change should not negatively affect existing designs. Tables 12 and 13 provide a comparison.

Dynamic Electrical Characteristics (T_{ITRIP}):

The ITRIP blanking time (T_{ITRIP}) has increased to increase over-current detection reliability and to reduce the need of an external noise filters at the ITRIP pin. The overall propagation delay (max) for both shutdown and fault communication has increased slightly. No changes will be needed in applications already using the IR2136x family. Tables 14 and 15 provide a comparison.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
DT	Deadtime	**220**	290	**360**	ns	V_{IN} = 0 V & 5 V
MDT	DT matching (Hi->Lo & Lo->Hi on all channels)	—	25	**70**	ns	Ext. deadtime >400 ns

Table 12: Deadtime IR2136x

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
DT	Deadtime	**190**	290	**420**	ns	V_{IN} = 0 V & 5 V ext. deadtime >0 s
MDT	DT matching (Hi->Lo & Lo->Hi on all channels)	—	—	**60**	ns	Ext. deadtime >0 s

Table 13: Deadtime IRS2136xD

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{ITRIP}	ITRIP to output shutdown propagation delay	500	750	**1000**		V_{ITRIP} = 5 V
t_{FLT}	ITRIP to FAULT propagation delay	400	600	**800**		V_{IN} = 0 V or 5 V V_{ITRIP} = 5 V
t_{bl}	ITRIP blanking time	100	**150**	—	ns	V_{IN} = 0 V or 5 V V_{ITRIP} = 0 V

Table 14: Over-current Trip Related Parameters (IR2136x)

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{ITRIP}	ITRIP to output shutdown propagation delay	500	750	**1200**		V_{ITRIP} = 5 V
t_{FLT}	ITRIP to FAULT propagation delay	400	600	**950**		V_{IN} = 0 V or 5 V V_{ITRIP} = 5 V
t_{bl}	ITRIP blanking time	—	**500**	—	ns	V_{IN} = 0 V or 5 V V_{ITRIP} =5 V

Table 15: Over-current Trip Related Parameters (IRS2136xD)

Conclusions

In most cases, any member of the IR2136x family will be easily and advantageously replaced by the new lead-free IRS2136xD family. The application will benefit from a monolithic solution which has an integrating the bootstrap circuit and features improved input filters.