International
IOR Rectifier

Application Note AN-1067

Design Considerations When Using Radiation-Hardened Small Signal Logic Level MOSFETs

Table of Contents

Page

Introduction 1
Acronyms 1
Maximum Rating and Electrical Characteristics 2
Design Considerations 3
Temperature Effects 4
Radiation Performance 5
Output Transfer 9
Switching Time 11
Design and Performance Benefits 13
Lower Gate Drive and Power Requirements 13
Low Saturation Voltage 14
Faster Switching 14
Radiation Performance Test Report 15
Driving from Logic Gates and Linear Circuit Drives 15
Conclusions 22
Acknowledgements/References 23

Balancing requirements when selecting materials and practices for production facilities is not an easy task. This application note provides more background information on thermal cycling and the potential impact of underfill, lead-free solder, insulated metal substrates (IMS) and conformal coatings when using MOSFETs in the DirectFET™ package.

International
IOR Rectifier

APPLICATION NOTE

AN-1067

International Rectifier • 233 Kansas Street El Segundo CA 90245 USA

Design Considerations When Using Radiation-Hardened Small Signal Logic Level MOSFETs

By
Tiva Bussarakons

Introduction:

Radiation hardened power MOSFETs have been used in space applications for many years. However, bipolar transistors have been the only design solutions for small signal and low power applications until recently. International Rectifier has just introduced its 4th generation radiation hardened MOSFET targeted for space design applications. The first of the series is a complimentary pair of low power N and P channel devices. They are designed for general-purpose, low power switching applications. With their low gate threshold voltage of sub 2V, these devices can be driven directly by standard logic gates, linear circuit devices, micro-controllers, or by most devices operating with a voltage source of approximately 3.3-5V with a very low energy requirement. For many design applications, these devices offer distinct performance benefits and simplify circuit designs typical of the industry's standard logic level MOSFETs. In some applications they may directly replace the popular bipolar transistors 2N2222A and 2N2907A with little or no modification to the existing circuit designs and board layout as they are housed in the same surface-mount style package UB (3 LCC). The products are designed and fully characterized for use in commercial and military radiation design applications.

Acronyms:

A	Amperes
BJT	Bipolar Junction Transistor
BVDSS	Drain to source voltage breakdown
BVGSS	Gate to source voltage breakdown
Cdg	Gate to drain capacitance
Cds	Drain to source capacitance
Cgs	Gate to source capacitance
Ciss	Input capacitance
Coss	Output capacitance
Crss	Reverse transfer capacitance
CTR	Current Transfer Ratio
EOL	End of life
fsw	Switching frequency
gfs	Transconductance
ID	Maximum drain current - continuous
IDM	Maximum drain current – pulsed
IDSS	Drain to source leakage current
IGSS	Gate to source leakage current
Isink	Sink current
Isource	Source current

LET	Linear Energy Transfer	TID	Total Ionizing Dose
MOSFET	Metal Oxide Substrate Field Effect Transistor	Tj	Junction temperature
PD	Power dissipation	tr	Rise time
QCI	Quality Conformance Inspection	V	Volts
QG	Total gate charge	VCE(sat)	Saturation voltage
RDS(on)	Drain to source on-resistance	VDS(on)	Drain to source on-voltage
SEE	Single Event Effect	VGS(th)	Gate threshold voltage
SOA	Safe Operating Area	VOH	High-level output voltage, TTL logic gate
td(off)	Turn-off delay time	VOL	Low-level output voltage, TTL logic gate
td(on)	Turn-on delay time	VSD	Source to drain body diode voltage
tf	Fall time	W	Watts

Maximum Rating and Electrical Characteristics:

The first of the series are low power devices housed in the 3-terminal UB LCC (leadless chip carrier) surface mount package. The part numbers are IRHLUB770Z4 and IRHLUB7970Z4 for N and P channels, respectively. These devices are also available in a TO-39 package and in die form. The die dimensions are.040"L x .040"W x 0.008"H. Some of the absolute maximum ratings and electrical characteristics are shown in Table 1 and 2, respectively. The current ratings increase with the TO-39 package. Please note that most of the electrical characteristics shown in the data sheet are for Tj of 25ºC. Normalized performance of key parameters under extreme temperatures can be found in the subsequent paragraphs.

Parameter	Symbol	N-Channel		P-Channel		Unit
		UB	TO-39	UB	TO-39	
Drain to Source Breakdown Voltage	BV_{DSS}	60	60	-60	-60	V
Drain Current-Continuous	I_D	0.8	1.6	-0.53	-1.6	A
Drain Current - Pulsed	I_{DM}	3.2	6.4	-2.12	-6.4	A
Maximum Power Dissipation @25ºC	P_D	0.6	5	0.6	5	W
Gate to Source Voltage	BV_{GSS}	±10	±10	±10	±10	V

Table 1 – Absolute Maximum Ratings

Parameter	Symbol	N-Channel		P-Channel		Unit
		UB	TO-39	UB	TO-39	
On-Resistance	$R_{DS(on)}$	0.55*	0.5*	1.2*	1.2*	Ohms
Gate Threshold Voltage	$V_{GS(th)}$	1 to 2	1 to 2	-1 to -2	-1 to -2	V
Total Gate Charge	Q_G	3.6	3.6	3.6	4	nC
Turn-on Delay time	td(on)	8	8	18	18	ns
Rise Time	tr	10	20	20	20	ns
Turn-off Delay Time	td(off)	26	20	15	15	ns
Fall Time	tf	10	15	25	25	ns

* At the rated I_D

Table 2 – Electrical Characteristics at Tj = 25ºC

Design Considerations:

The radiation hardened logic level MOSFETs have performance characteristics over the temperature range and radiation environments similar to IR's standard radiation hardened power MOSFET generations 2 (R5) and 3 (R6). The only notable difference is the gate threshold voltage, VGS(th) and the power handling capability. These new devices have a lower gate threshold voltage of 1-2V as compared to 2-4V or 2.5-4.5V for the previous generations. While this feature requires lower gate drive voltage levels, the devices are more susceptible to spurious turn-on due to noise. Circuit layout and circuit noise management become one of the key design considerations. The BVGSS rating is also lower, ±10V for these new devices as compared to ±20V for the previous generations. These devices are well characterized under extreme temperatures and radiation environments. Test data and test reports are readily available. The shifts in key performance parameters are included in this note. Designers should account for the shifts in parameters that may be critical to their design applications. The subsequent paragraphs are discussions of the effects that the temperature and radiation environments have on key parameters. These effects are also summarized in Table 3. All other design considerations for the standard MOSFETs apply when designing with these new devices. Refer to the referenced IR application notes for details.

Temperature Effects:

As with most semiconductors, temperature has some effect on the power and current rating of these transistors. Please refer to the corresponding data sheets of the devices and packages for parameter de-rating. Temperature has negligible effect on BVDSS, BVGSS, QG, and switching time. It has considerable effect on IDSS, IGSS, VGS(th), gfs, and RDS(on). However, the only parameters that may have a significant impact on most circuit designs are VGS(th) and RDS(on). These parameters are discussed below.

VGS(th) - Temperature has a direct effect on the threshold voltage. The threshold voltage decreases with increasing temperature and increases with decreasing temperature. The magnitude of this temperature coefficient is inherent in the design and process used in the manufacture of these devices. The temperature coefficient of $V_{GS}(th)$ for these devices is approximately -.003V/ºC. Figures 1 and 2 are normalized $V_{GS}(th)$ with respect to temperature for N and P channel devices, respectively.

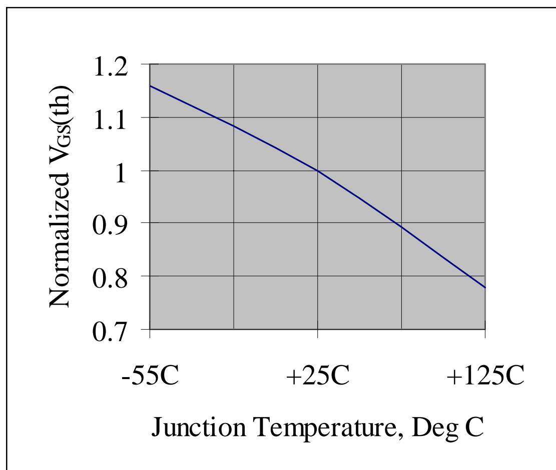


Figure 1 - Normalized V_{GS}(th) vs. Temperature N Channel

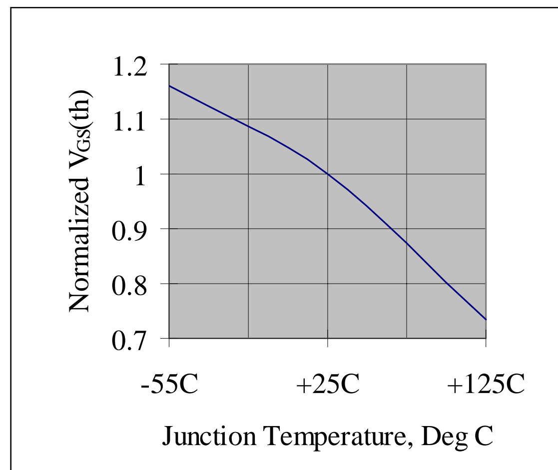


Figure 2 - Normalized V_{GS}(th) vs. Temperature P Channel

R_{DS}(on) - The R_{DS}(on) has a positive temperature coefficient because it is dependent on the silicon carrier mobility. The mobility decreases with temperature because there is more scattering by phonons at higher temperatures. This is mostly the issue in the lightly doped epi. In the source and in the inversion layer, the mobility is less dependent on phonon scattering since it is dominated by impurity scattering. The typical temperature coefficient of R_{DS}(on) is approximately 1.6 mOhm/ºC for these devices. Figures 3 and 4 illustrate the normalized R_{DS}(on) performance of the N and P channel devices for V_{GS} = 5V. The effect of the package resistances is negligible. The curves represent the typical on resistance change vs. temperature.

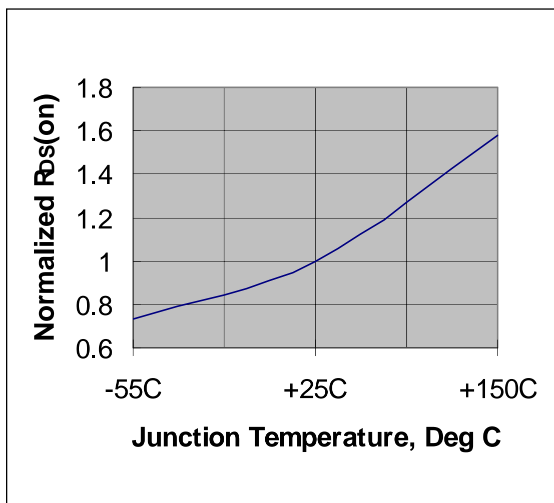


Figure 3 - Normalized R_{DS}(on) vs. Temperature N Channel

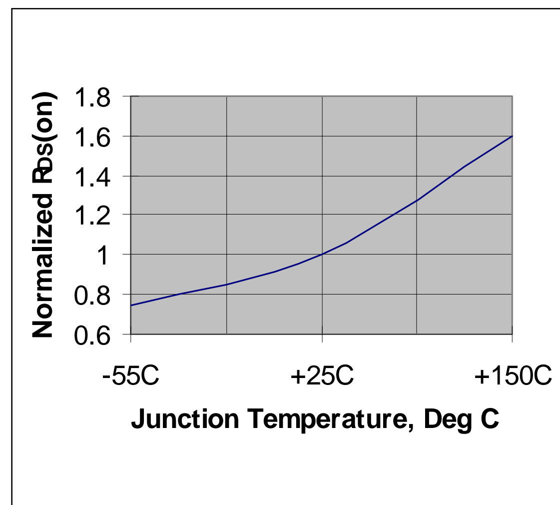


Figure 4 - Normalized R_{DS}(on)) vs. Temperature P Channel

Radiation Performance

These transistors are designed for continuous operation in harsh radiation environments. The devices are characterized for performance under total ionizing dose (TID) up to 1Mrads, single event effects (SEE) for heavy ions up to the LET of 82 MeV-cm^2/mg and neutron fluence up to 1E15 n/cm2. Performance characterizations under prompt dose are in process.

TID - The total ionizing dose has negligible effect on BVDSS and RDS(on). The worst-case limit with respect to various radiation doses is presented in the data sheets. TID has some effect on IDSS, gfs and VGS(th). VGS(th) limits in the data sheets include the TID effect. For IDSS and gfs, the specification limits on the data sheet are conservative. The specification limits can be used as the worst-case design scenario that includes TID effect.

SEE - Testing has shown that these transistors are resistant to both single event gate rupture (SEGR) and single event burnout. BVDSS is the only parameter that is significantly affected by heavy ions. Figures 5 and 6 show the safe operating areas (SOA) under heavy ions with LET ranging from 37 (bromine) to 82 (gold) MeV-cm^2/mg for N and P channel devices, respectively

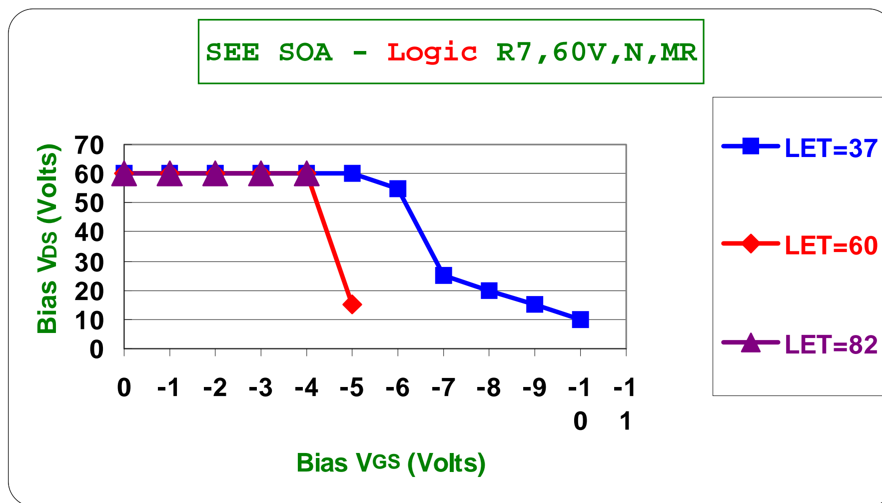


Figure 5. SEE Safe Operating Area – N Channel

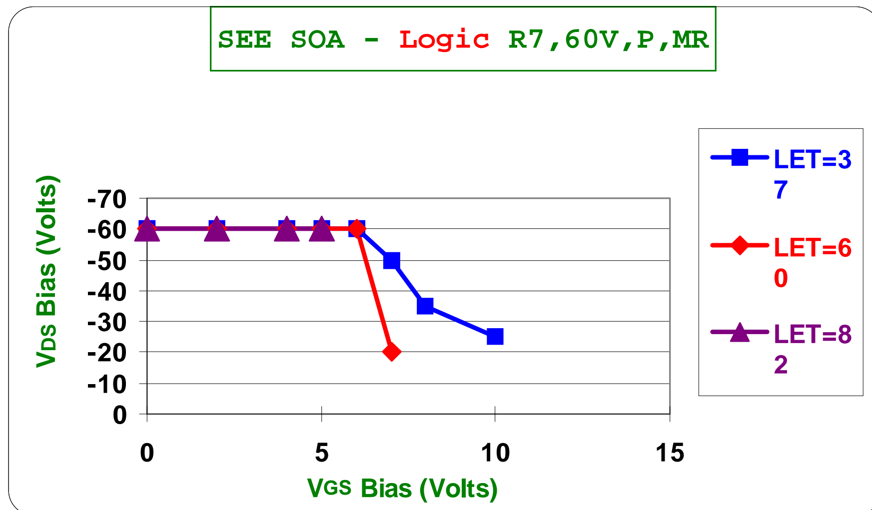


Figure 6. SEE Safe Operating Area – P Channel

Neutron – Neutron radiation has some effect on IDSS, IGSS, RDS(on) and VGS(th) for N channel device only. It has negligible effect on all other parameters and VGS(th) of P channel device. The limits of IDSS and IGSS in the data sheets account for these effects and may be used for worst-case analysis. Figure 7 is a normalized VGS(th) for N channel device. Figures 8 and 9 are typical RDS(on) performances of N and P channel devices. It follows that the on-resistance for both device types remains constant for up to neutron fluence of 1e14 n/cm2.

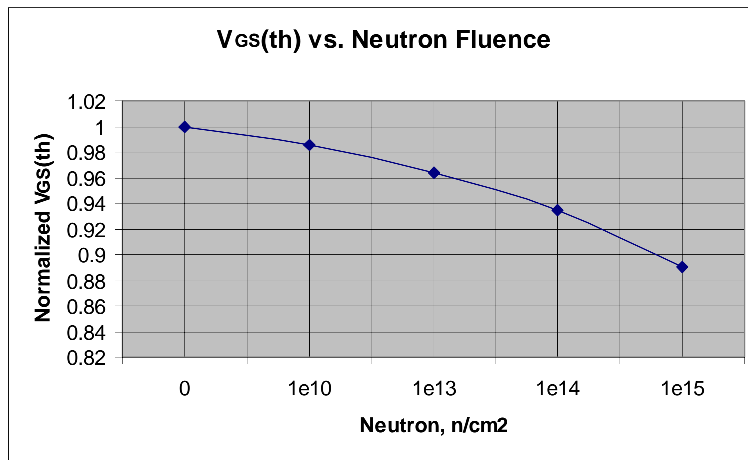


Figure 7 – Normalized VGS(th) for N Channel Device

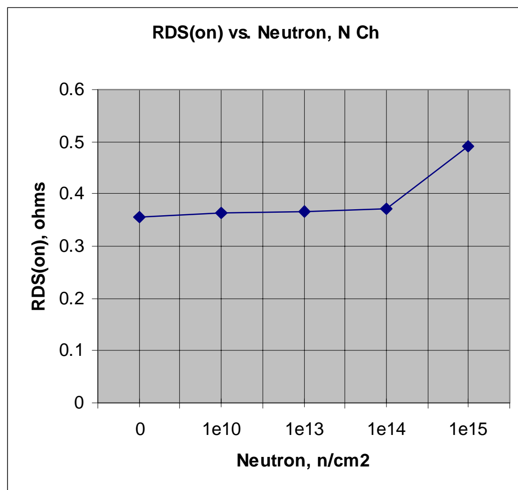


Figure 8 – Typical RDS(on) vs. Neutron, N Ch

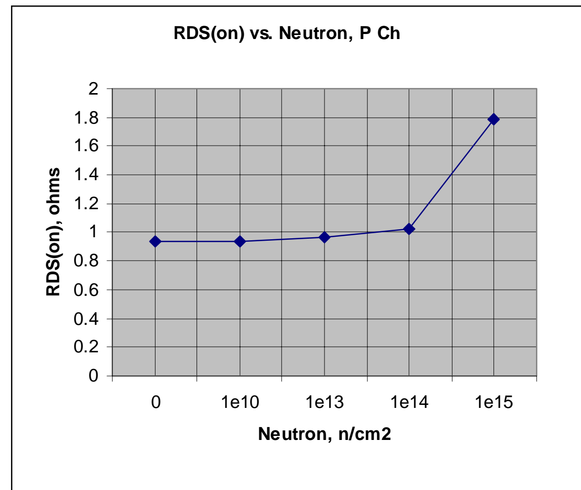


Figure 9 – Typical RDS(on) vs. Neutron, P Ch

Table 3 summarizes the effects that temperature and radiation have on the performance parameters of the rad-hard logic level MOSFETs. Standard design rules including aging and end of life (EOL) degradation should apply for designs using these devices.

Parameter	Temperature Effect	Radiation Effect
P_D	Package dependent, de-rating is required	Not applicable
I_D	Package dependent, de-rating is required	Not applicable
$V_{GS}(th)$	Has negative temperature coefficient of approximately 3mV/C	Slight decrease under TID and neutron. Neutron has negligible effect on P channel. Limit in data sheet accounts for the effect. SEE resistance to LET = 82
BV_{DSS}	Negligible	No degradation under TID and neutron. Degraded under SEE. Refer to SEE SOA curves.
BV_{GSS}	Negligible	No degradation
$R_{DS}(on)$	Has positive temperature coefficient, approx. 1.6 mOhm/C. Refer to normalized $R_{DS}(on)$ curve for a typical performance.	Negligible under TID. Negligible up to neutron of 1E14 n/cm2.
I_{DSS}	Considerable, refer to limits in data sheet	Slight increase with respect to increasing TID and neutron
I_{GSS}	Negligible	Negligible under TID. Slight increase under neutron.
Q_G	Negligible	Negligible
gfs	Negligible	Negligible under TID and neutron up to 1e14 n/cm2

Table 3. Summary of Temperature and Radiation Effects on the Performance Parameters

Output Transfer

To insure a proper enhancement (turn-on) of the devices, a suitable voltage must be applied to the gate. The minimum voltage level is about 2.5V for the N channel and –2.5V for the P channel in order to conduct in the neighborhood of 100 mA at VDS of 1 Volt and higher. Figures 10 and 11 show the gate drive voltage required at –55C to enhance the N channel and P channel devices for different levels of drain current. These curves represent the typical worst-case performance of these transistors at -55ºC, where VGS(th) is highest. A slightly higher gate voltage should be employed to compensate for lot-to-lot variations and to insure optimal switch time. The optimum range is 4.5V to 5.5V at current levels of 1 Amp and higher.

To insure a complete turn-off, the gate must be biased with a negative or zero voltage (circuit ground) with respect to source for an N channel. Under no condition should it exceed +0.5V for the specified temperature range. Refer to the data sheets for the typical performances at room and at 150ºC temperature.

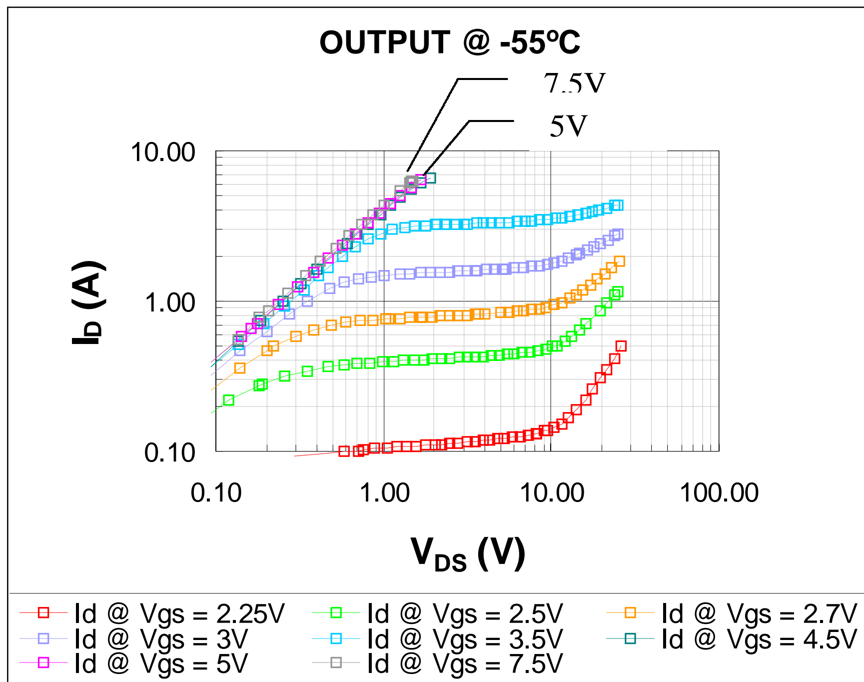


Figure 10. Typical Output characteristics at -55ºC, N Channel

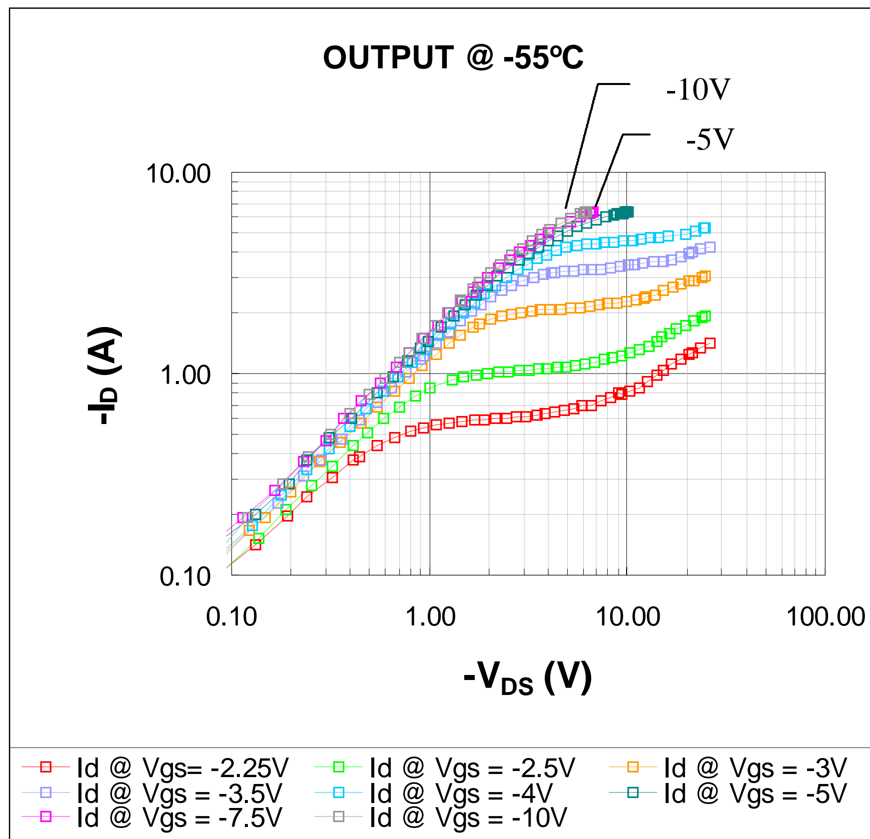


Figure 11. Typical Output Characteristics at -55ºC, P Channel

Switching Time

MOSFETs are known for their fast switching speed and low DC losses. When driven with sufficient gate voltage, a MOSFET will conduct with a very low on-resistance. However, for high frequency switching applications in the range of 200KHz and higher, switching losses will predominate. In order to provide the fastest transition time gate drive design becomes critical to keep the switching losses to a minimum. For design applications using these low power devices, similar design considerations apply although the impact of switching losses is not as critical. In fact, for some circuit applications, controlling the switching time may be desirable. Figure 12 defines the switching times of a typical MOSFET.

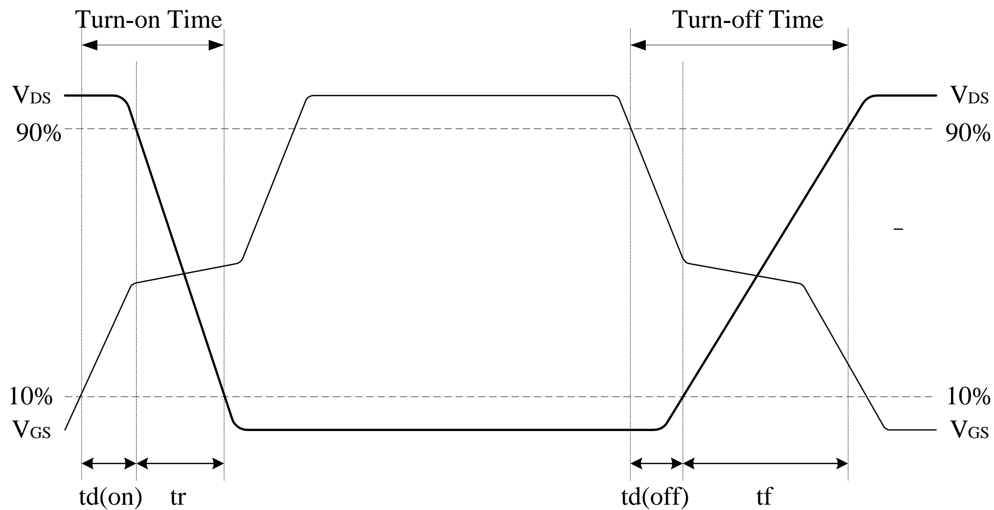


Figure 12. Switching Time Definitions

Many application notes have been written about how to properly drive a MOSFET, and they offer formula to predict the switching times. For most designs with standard or logic level MOSFETs for low or high power applications, the simplest and most accurate method to predict the switch time is to use the gate charge data, which is available on the data sheet. For a given gate charge (QG), a drive current has a direct impact on the switch time by the following formula:

$$t = QG/IG$$

Where t is switch time, QG is gate charge and IG is gate drive current. Refer to Figure 13. It is clear from this formula that the higher the gate drive current (Isource), the faster the turn-on time. Similarly for the turn-off, a higher Isink (or lower impedance path to remove the charge from the gate) will provide a faster turn-off time. While this is true for most high power designs where the drain current is high (Rload is low) and the time required to discharge the Coss is negligible, Coss becomes the predominant factor for low current applications. A high Rload (low drain current) will lengthen the discharge time of the drain voltage/ current resulting in a slow turn-off time. The new rad-hard logic level MOSFETs are optimized for switching performance with drain currents in the range of 10mA to over 1A.

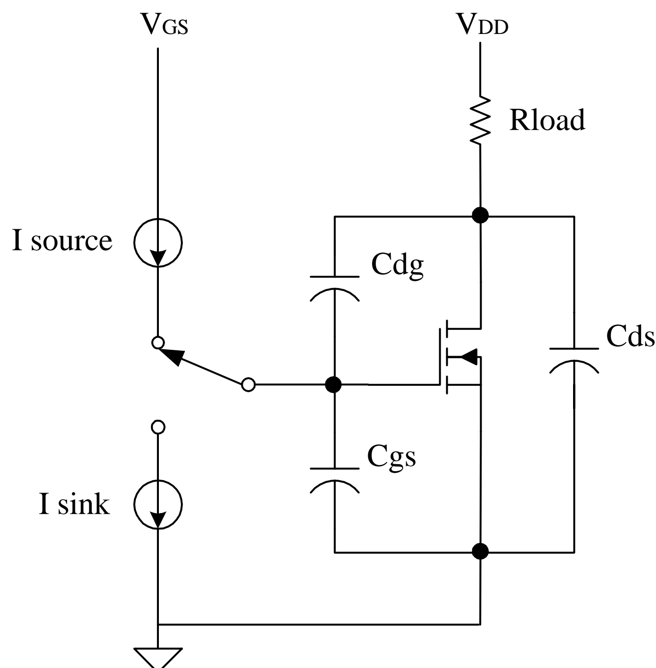


Figure 13. Gate Drive Currents with a MOSFET Equivalent Circuit

Design and Performance Benefits

As with all MOSFETs, these devices offer several performance benefits that are superior to bipolar transistors in switching applications. Discussion of the benefits follows below.

- Lower gate drive current and power requirements
- Faster switching – reducing propagation delay
- Lower VDS(on) as compared to BJTs VCE(sat)
- Designed and characterized for radiation design applications – test data support
- Can be driven directly from logic gates

Lower Gate Drive Current and Power Requirements

A MOSFET is a voltage driven device. A voltage source is applied to the gate to cause drain to source conduction. Very little gate current is required to cause this conduction and a complete enhancement. A BJT such as the 2N2222A requires base current to cause the conduction to take place from collector to emitter. To insure saturation, a BJT requires a minimum base current (IB) for a given collector current (IC) as dictated by a DC current gain (HFE). The minimum IB is equal to IC/HFE. To saturate a BJT with a collector current 200mA, a minimum of 4mA is required for a bipolar device that has an HFE of 50. This current gain may reduce to 25% of its initial maximum limit due to aging and EOL radiation effect. The base current will need to increase to 16 mA to insure the saturation in this design example.

The increase in base current demand may eliminate BJTs from many design applications requiring an interface to logic gates, linear IC's and opto-isolators, as most of these devices are only capable of providing a source current of a few to 10mA with limited selection of up to 20mA. Opto-isolators suffer a reduction of CTR under extreme temperatures and under most radiation doses. A reduction of as much as 70-80% of its rated CTR is quite normal for many of the devices in the market today. Given this scenario, the logic level MOSFET is the solution, as they do not have the minimum gate current requirement to contend with. Only a few milli-amperes from a 5V source are sufficient to satisfy the switching operations.

It follows that the increased base current of the BJT means more wasted power due to the inefficiency. Unlike the BJT, the energy required to turn on a MOSFET is independent of the drain current. It is a function of VGS, QG and fsw (switching frequency). With a QG of 3.6nC, fsw of 100KHz and VGS of 5V, the approximate power loss can be calculated using the following formula:

$$P = VGS \times QG \times fsw$$
$$P = 5 \times 3.6\times10^{-9} \times 100 \times10^{3} = 1.8mW$$

When using a device with open collector additional power during off cycle needs to be included. This should amount to approximately 1.667 mW for (VDD/Rpull-up x VCE(sat) = 5V/1.5Kohms x 0.5V =1.667 mW)

an 54LS01 device. This will bring the total power loss to 3.467mW (1.8mW + 1.667mW). For other types of device, the power loss may be slightly different depending on the amount current drawn to through the pull-up resistor, which is normally dictated by the maximum allowable current to insure the maximum $V_{CE(sat)}$ of the sink transistor.

The approximate power loss to drive the bipolar transistor in the example above can be calculated as follows:

Assuming the base voltage (V_B) to be 5V and 50% duty cycle, the power loss is then:

$$P = V_B \times I_B \times 0.5 = 5 \times 16 \times 10^{-3} \times 0.5 = 40 \text{ mW}.$$

This is about 11 times (40 mW/3.467 mW = 11.5) the power loss of the MOSFET device. Please note that the wasted power in the base resistor is included in the V_B drop to simplify the calculation. Should V_B reduce to 2V to minimize the power loss, it would amount to 16 mW or about 4.6 times the power loss of the MOSFET device.

While this loss is a mere 40 mW or the unlikely scenario of 16 mW, the accumulation of such losses will add up on the larger scale and will drain (the) precious power. It will also increase the weight of a spacecraft as the solar panel and power circuits must be sized for the increased power due to the inefficiency.

Lower Saturation Voltage, $V_{DS}(on) < V_{CE}(sat)$

A MOSFET dissipates less power and increases the circuit efficiency with its lower on-voltage than a bipolar transistor. The N channel device has a maximum R_{DS}(ον) οφ .55 ∧ ατ 25ºC and a typical R_{DS}(ον) οφ 0.56∧ (.4 ∧ τψπ ατ 25ºC. x 1.4) at 110ºC. For a circuit that switches at 250mA, the drain to source voltage is approximately 0.14V as compared to a typical V_{CE}(sat) of a 2N2222A of 0.3V. This translates to a power loss of 35 mW for MOSFET vs.75 mW for 2N2222A. Also, this low saturation voltage may enhance designs that require near zero ground reference especially at a very low current, the drain-source voltage could virtually be zero when the MOSFET is used as a clamping device to a circuit ground.

Faster Switching

MOSFETs are known for their fast switching performance. They switch approximately 3 to 10 or more times faster than a comparable bipolar device. Being a majority carrier device, it outperforms the BJT in that its turn-off is not delayed by minority carrier storage time in the base, and the switching time performance is independent of temperature. A MOSFET begins to turn off as soon as its gate voltage drops down to its threshold voltage. This results in a shorter propagation delay than a BJT. For many design applications this characteristic improves circuit response time and reliability. It often translates to less stress on a load-bearing device such as a primary switch of a DC-DC converter during overload sensing and protection mode.

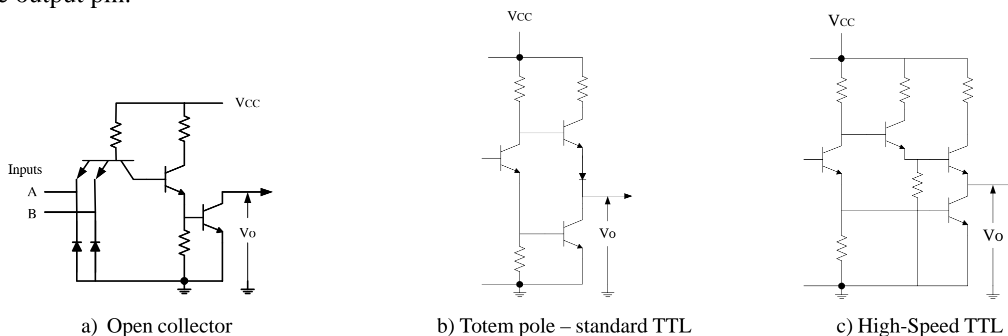
Radiation Performance Test Report

Unlike the standard bipolar transistors, these radiation hardened logic level MOSFETs are designed to operate in radiation environments. The devices are tested and characterized for space applications. Radiation test reports and QCI qualification data packs are available. Products are qualified in accordance with the radiation hardness assurance per MIL-S-19500. DSCC qualification of these devices is in process.

Driving From Logic Gates and Linear Circuit Devices

The logic level MOSFETs are extremely fast switching devices. The total switch time is less than 80ns under an ideal gate drive condition with the operating drain current near or equal to their rated currents. With their low threshold voltage of 1-2V, the rad-hard logic level MOSFET's are designed to be driven directly by the industry's standard logic gates, linear circuits, micro-controllers, or most devices that operate from a 5V source. In lightly loaded applications, they may even be able to be driven directly by 2.5 V and 3.3 V complementary CMOS logic outputs. However, the switching time performance varies due to different output currents (Isource and Isink) of the drivers. When selecting a logic gate or a linear circuit device, as a driver, the sink and source currents are critical to switching performance of the logic level MOSFET's, the higher the source/sink currents, the faster the switching time. Conversely, if control of the switching time is desirable, a gate resistor may be introduced to limit the peak gate current to slow the switching speed.

Some of the TTL logic gates such as 54/74 (standard TTL), 54S/74S (Schottky), 54LS/74LS (low power Schottky), and 54F/74F (high speed TTL) series have an open collector output configuration while others have a totem pole output. The simplified output configurations of the TTL logic devices are shown in Figure 14. The totem pole outputs depicted in Figure 14b and 14c do not actually deliver the full supply voltage of VCC in the high-level output condition. The high-level output voltage (VOH) is between 2.4 to 2.7V for the supply voltage of 5V. To insure a complete enhancement and the lowest possible RDS(on), a 5V gate drive voltage is required. This can be accomplished with an addition of a pull-up resistor from the 5V supply bus to the output pin.



a) Open collector b) Totem pole – standard TTL c) High-Speed TTL

Figure 14. Simplified TTL Logic Gate Output Configurations

The gate threshold voltage, VGS(th) of these devices decreases with increasing temperature. At high temperatures it can approach VOL(max), maximum low-level output voltage, which is about 0.5V worst case for most TTL logic gates. Care should be taken to insure that the minimum VGS(th) is higher than VOL(max) at the highest operating temperature in order to guarantee a complete turn-off.

Figure 15 is a sample circuit driving the N channel logic level MOSFET with a 54LS01, 2 input NAND gate. The 54LS01 has an open collector output. A pull-up resistor, R2, is required to obtain proper gate drive voltage. During turn-on, the pull-up resistor limits the gate drive current. During turn-off, the 54LS01 must sink both the gate current and the pull-up resistor current. To insure that the VOL is not greater than 0.5V, this current (IOL) must not be greater than 4mA as specified by the 54LS01 data sheet. With VOL not exceeding 0.5V, the logic FET is assured to turn off. It can be seen from the test data of Table 4 that with zero gate resistance and the higher source/sink current with the pull-up resistor of 1.5 kOhms, the circuit yields the fastest switching time, and the device switches faster with the higher drain currents. Figures 16 and 17 are typical turn-on and turn-off switching waveforms with a pull-up resistor of 3K and an operating drain current of 250mA.

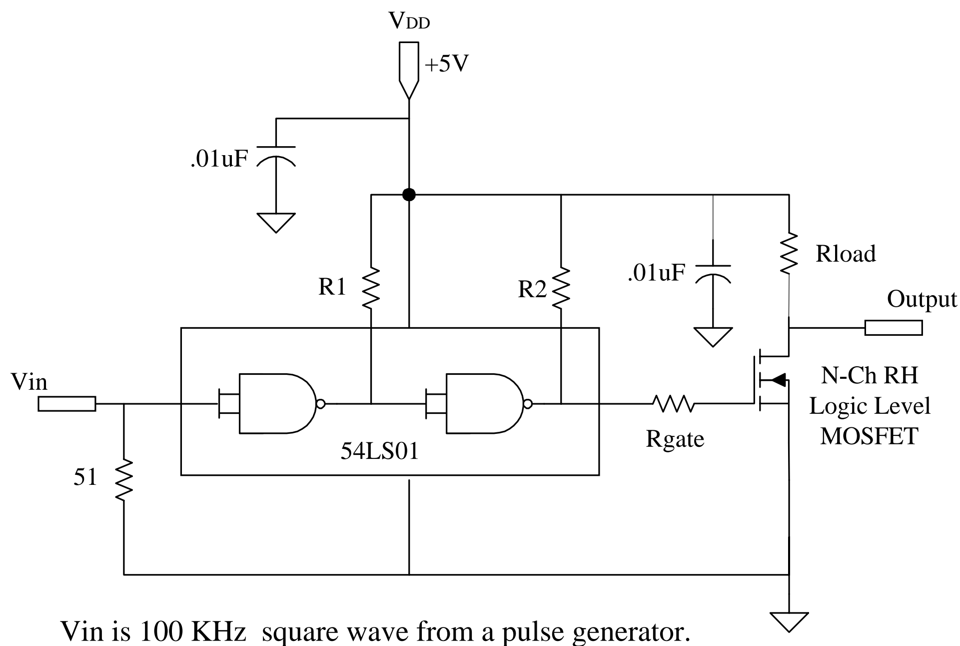


Figure 15. Switching Time Test Circuit Driving from a 54LS01, a Low Power Schottky NAND Gate

Rload (ohms)	~I_D (mA)	Rgate (ohms)	R2 (ohms)	Switching Time (ns)			
				td(on)	tr	td(off)	tf
500	10	0	3K	200	110	40	180
51	100	0	3K	200	280	18	15
20	250	0	3K	220	340	16	17
500	10	220	3K	200	240	75	200
51	100	220	3K	220	300	60	40
20	250	220	3K	240	340	52	40
500	10	470	3K	240	280	160	200
51	100	470	3K	260	320	120	90
20	250	470	3K	260	380	110	80
500	10	0	1.5K	100	100	40	180
51	100	0	1.5K	100	140	18	15
20	250	0	1.5K	120	160	17	7

Table 4. Switching Time Test Data of N Channel Logic Level FET driven by a 54LS01 NAND gate

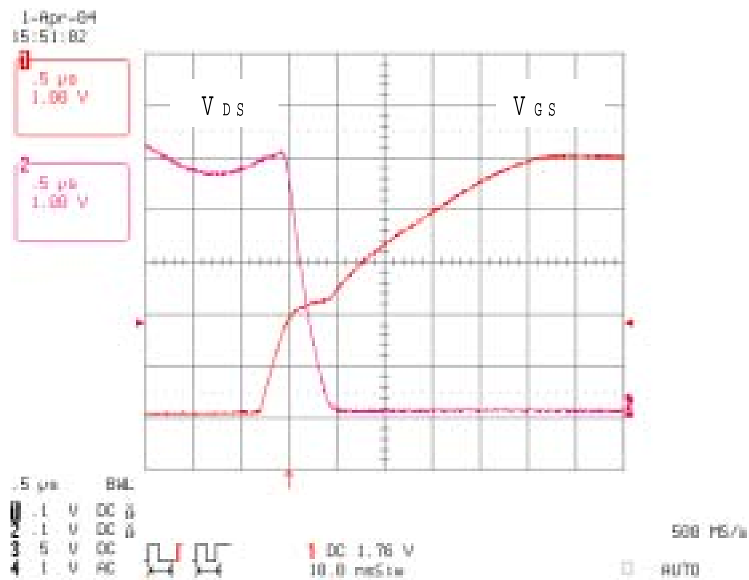


Figure 16. Turn-on Switching Waveform Driving from a 54LS01 with 3K Pull-up Resistor and Drain Current of 250mA

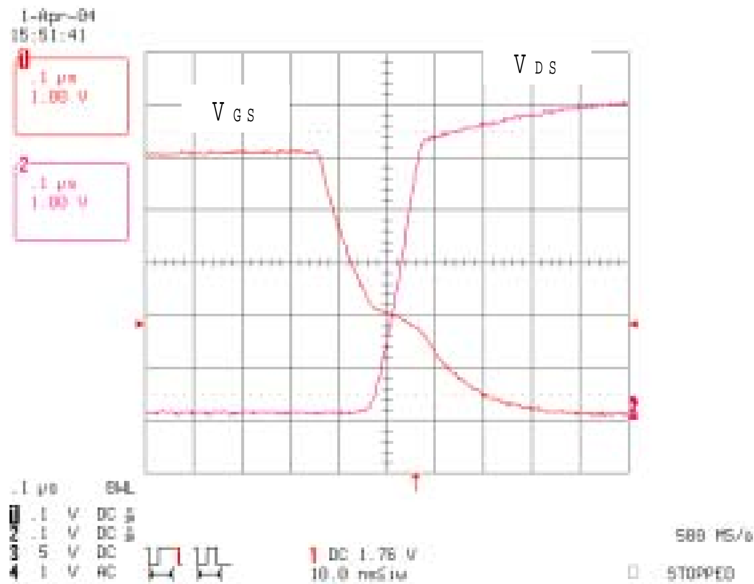
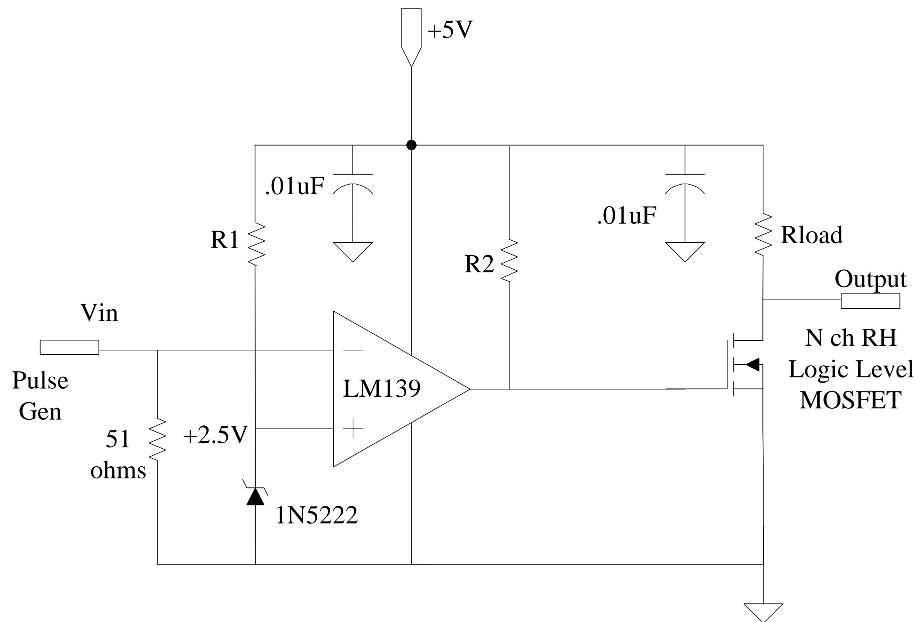


Figure 17. Turn-off Switching Waveform, Driving from a 54LS01 with 3K Pull-up Resistor and Drain Current of 250mA

Figure 18 shows the switching time test circuit for driving an N channel logic level MOSFET from an LM139, which has an open collector output. Table 5 shows the typical switching time performances with different pull-up resistors and drain currents



Vin is a triangle ramp, approx. 3VP-P, swing from 0 to 3V,100KHz, from a pulse generator.

Figure 18. Switching Time Test Circuit Driving from a Voltage Comparator LM139

Rload (ohms)	~ID (mA)	Rgate (ohms)	R2 (ohms)	Switching Time (ns)			
				td(on)	tr	td(off)	tf
500	10	0	3K	180	240	110	190
51	100	0	3K	200	330	70	30
20	250	0	3K	200	400	70	25
500	10	0	1.5K	100	120	110	200
51	100	0	1.5K	110	160	70	30
20	250	0	1.5K	100	210	75	30

Table 5. Switching Time Test Data Driving from an LM139, voltage comparator

For CMOS logic devices, the maximum supply voltage VCC is normally15V with complete electrical characterizations available at 5V and 10V for most devices. All CMOS circuits usually have an output configuration as shown in Figure 19. It consists of a P-channel MOSFET connected in series with and N-channel MOSFET (drain to drain) with the gates tied together. The output usually swings to the VCC or 5V for VOH and down to zero volt, thus a pull-up resistor is not required to insure a complete enhancement. Figure 20 shows the switching time test circuit for driving an N-channel rad-hard logic level MOSFET from a CD4049UB inverting buffer with the CMOS output configuration. Table 6 is the typical switching performance for different drain currents.

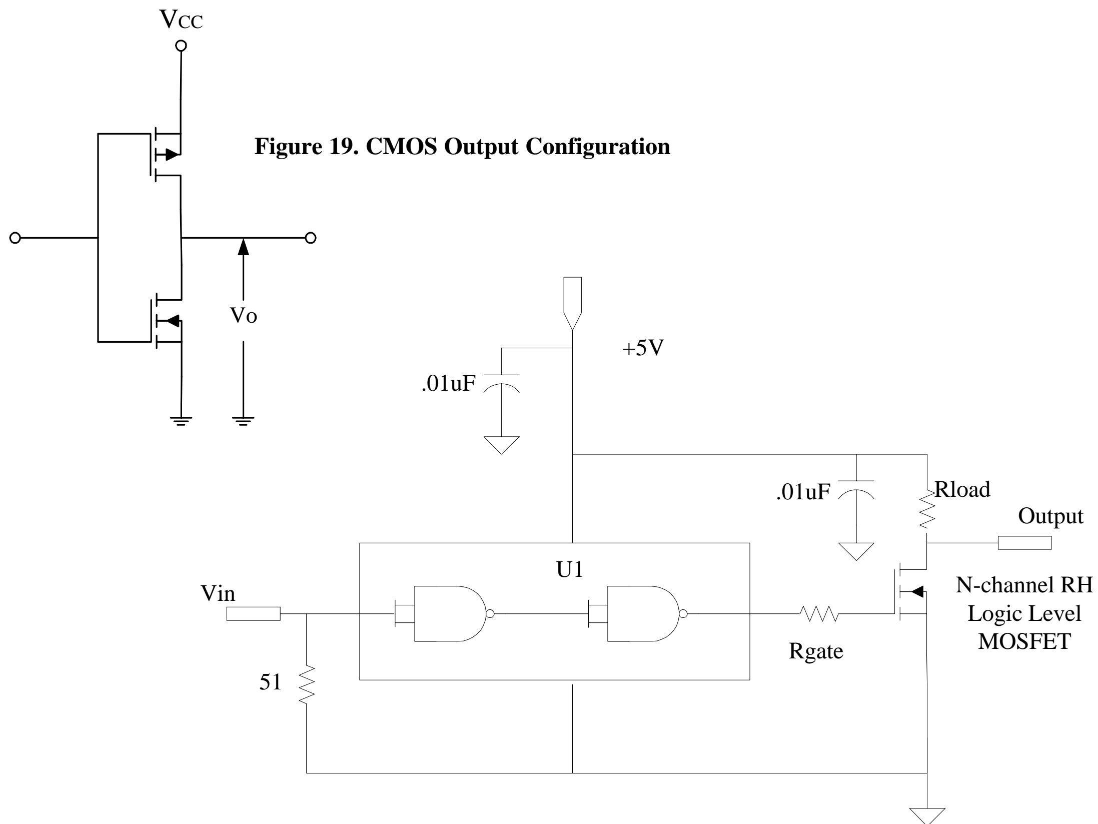
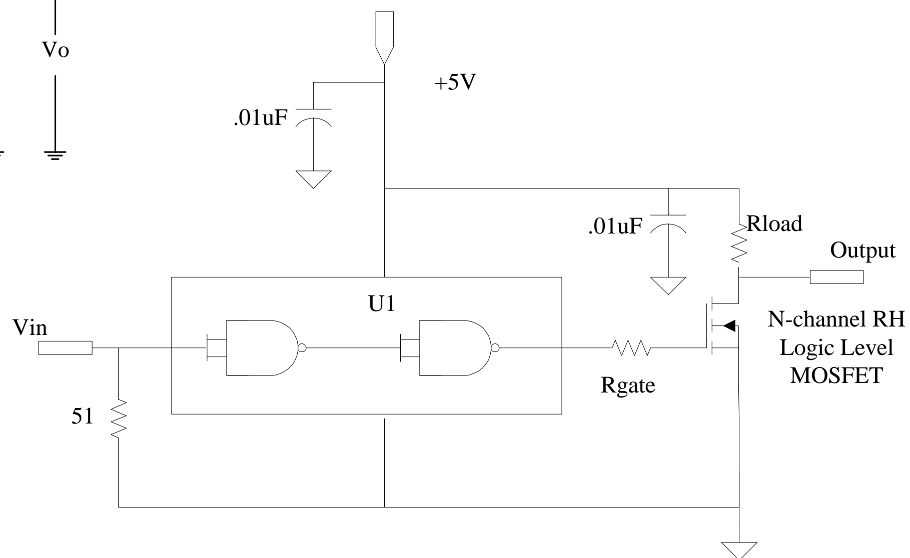


Figure 19. CMOS Output Configuration



Vin is 100KHz square wave, 0-5Vp-p from a pulse generator.

Figure 20. Switching Time Test Circuit Driving an N-Channel Logic Level MOSFET from an Inverting Buffer CD4049UB

Rload (ohms)	~ID (mA)	Rgate	Switching Time (ns)			
			td(on)	tr	td(off)	tf
500	10	0	48	40	58	225
51	100	0	40	50	30	22
20	250	0	40	60	28	10

Table 6. Typical Switching Time Performance Driving from a CMOS output CD4049UB Inverting Buffer.

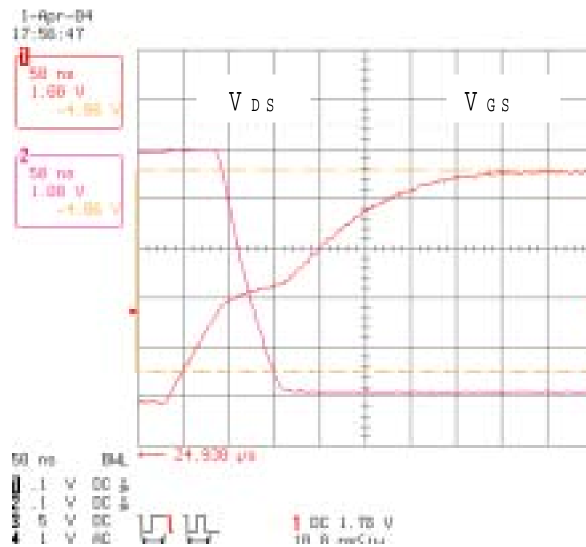


Figure 21. Turn-on Switching Waveform Driving from a CD4049UB for Drain Current of 250 mA

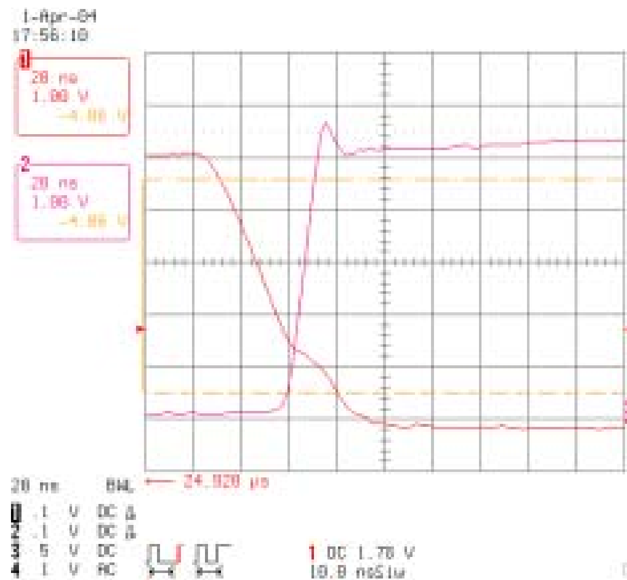


Figure 22. Turn-off Switching Waveform, Driving from a CD4049UB for Drain Current of 250mA

Conclusions

The radiation-hardened logic level MOSFETs are designed for use in harsh radiation environments. The devices are fully characterized for commercial and military space design applications. TID, SEE and neutron radiation test reports are available. The devices are optimized for low current switching design applications from a few milli-amperes to over 1A. With their low threshold voltage of 1-2V, they are ideal when used to interface directly with most logic gates, linear IC's, micro-controllers and other device types that operate from a 3.3-5V source. They are the design solution for most circuits that require a high current gain, thus simplifying circuit designs and reducing component count. With their low power drive requirements and lower VDS(on) than the comparable BJTs, they improve circuit efficiency, resulting in size, mass and cost reduction at the system level.

Acknowledgements

I would like to thank the following colleagues for their invaluable input, test support, technical advice, and product information.

Mr. Huy Cao
Mr. Milt Boden
Mr. Tu Dao
Mr. Kare Lund
Mr. Lorentz Ou
Mr. Alan Tasker
Mr. Bjarne Soderberg

References:

1) Laszio Kiraly, “Low Gate Charge HEXFETS Simplify Gate Drive and Lower Cost”, International Rectifier, Design Tip DT 94-7A.
2) “Gate Drive Characteristics and Requirements for Heft’s”, International Rectifier, Application Note AN-937.
3) Vrej Barkhordarian, “ Power MOSFET Basics”, International Rectifier, Application Note.
4) “Use of Gate Charge to Design the Gate Drive Circuit for MOSFETs and IGBTs”, International Rectifier, Application Note AN-944.
5) “The Do’s and Don’ts of Using MOS Gate Transistors”, International Rectifier, Application Note AN-936.

International
IOR Rectifier
WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105
http://www.irf.com/ *Data and specifications subject to change without notice.* *7/8/2004*