

Application Note AN-1025

Designing a Power Supply Using the IRIS40xx Series

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Flyback Converter Power Supplies are very popular due to their simplicity, low cost, and ability to generate a number of outputs. Using the IRIS40xx series of Integrated switchers, and following the design procedures laid out in this application note and the other documents referenced, make the task of designing a basic power supply a simplified process. This application note gives step by step guidelines to guide you through designing your power supply.

APPLICATION NOTE

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International Rectifier • 233 Kansas Street El Segundo CA 90245 USA

Designing a Power Supply using the IRIS40xx Series

By Jonathan Adams

TOPICS COVERED

Introduction
Typical Circuit
Design Procedure

1) INTRODUCTION

Flyback Converter Power Supplies are very popular due to their simplicity, low cost, and ability to generate a number of outputs. Using the IRIS40xx series of Integrated switchers, and following the design procedures laid out in this application note and the other documents referenced, make the task of designing a basic power supply a simplified process. This application note gives step by step guidelines to guide you through designing your power supply.

2) TYPICAL CIRCUIT

Fig 1) on page 2 shows a typical single output offline power supply. This circuit will be used as the reference for the design procedure laid out in this application note. The circuit is applicable to all the IRIS devices, but obviously the diode bridge DB1 is not required if the input is a DC voltage.

This circuit uses an LM431 precision shunt regulator in the voltage control loop to achieve the best accuracy, but it will be shown later that there are other alternatives which can be used for the regulation for different cost/performance characteristics.

The circuit also shows the input EMI filter consisting of inductor L1 and capacitor C1. The values and calculations for these components will not be included here, but there are various publications on filter design which would help with the design of these, and take into account that the lowest frequency you would need to filter out is the minimum operating frequency of the IRIS part in the design.

3) DESIGN PROCEDURE

3.1) DEFINE POWER SUPPLY PARAMETERS

The first step is to define the parameters for the desired power supply. These are listed below:

- | | | |
|--|--------------------------------|---------------------------------------|
| 1) Minimum AC Input Voltage | V_{ACmin} | |
| 2) Maximum AC Input Voltage | V_{ACmax} | |
| 3) Line Frequency | f_{AC} | |
| 4) DC Bus Ripple Voltage | $V_{DCRIPPLE}$ | |
| 5) Main Output Voltage | $Vo1$ | |
| 6) Main Output Full Load Current | $Io1$ | |
| 7) Main Output Ripple Voltage | $Vo1_{RIPPLE}$ | |
| 8) Bias Supply Voltage | VCC | (select to be in the range of 16-20V) |
| 9) Additional Output Voltages | $Vo2..VoN$ | (N=4 for a 4 output supply) |
| 10) Additional Output Full Load Currents | $Io2...IoN$ | |
| 11) Additional Output Ripple Voltages | $Vo2_{RIPPLE}....VoN_{RIPPLE}$ | |
| 12) Main Output Accuracy | $Vo1_{TOL}$ | |
| 13) Main Output Regulation | $Vo1_{REG}$ | |
| 14) Estimated efficiency | η | |
| 15) Optocoupler Gain | G_{OC} | ($G_{OC} = 1$ is recommended) |

2.2) SELECT IRIS PART FOR APPLICATION

Part Number	Voltage Rating (V)	Max. Output Power (W)	Rdson (Ohms)
IRIS4007(K)	200	30	0.4
IRIS4011(K)	650	60	3.9
IRIS4013(K)	650	120	1.95
IRIS4015(K)	650	180	0.9

Using the above table select the part suitable for the application. Use the following guidelines:

DC input upto 100Vmax - Use 200V part
 AC input up to 70Vmax - Use 200V part

Universal Line Input - Use 650V part
 200-240VAC Input - Use 650V part

Note: Using a part at or close to its maximum power rating will require a larger heatsink, so if space constraints are important or airflow is limited, derate the power to approximately 1/2 the maximum. e.g. for a 60W adaptor it would be better to use an IRIS4013(K) than an IR4011(K).

2.3) DEFINE IRIS OPERATING PARAMETERS

We now need to define some operating parameters for the IRIS part that was selected in the above step. The parameters required are listed below:

- | | | |
|-------------------------------------|-----------|------------------------------------|
| 1)Minimum Operating Frequency | f_{min} | |
| 2)Maximum Duty Cycle | D_m | |
| 3)Parallel Resonant Capacitor Value | C_{res} | (Use values in the range 47pf-1nF) |

2.4) DESIGN TRANSFORMER (T1)

Refer to AN1024a “Flyback Transformer Design for the IRIS40xx Series”. Also the IRIStran.xls Excel spreadsheet can be used and is available on the website.

2.5) INPUT DIODE BRIDGE (DB1)

The input bridge is selected by using the following:

$$P_{Imax} = \frac{P_o}{\eta}$$

where Po is the maximum output power calculated in 2.4).

$$I_{INrms} = \frac{P_{Imax}}{V_{ACmin} \times \cos \phi}$$

cos φ is the power factor which can be assumed to be 0.6. The result is I_{INrms} which is the minimum current rating for the diode bridge.

$$V_{DCmax} = V_{ACmax} \times \sqrt{2}$$

The resultant V_{DCmax} calculated gives the minimum Voltage rating for the diode bridge, also a general rule of thumb is to use 600V for a 230V input, and use 800V for a universal input.

2.6) INPUT FILTER CAPACITOR (C2)

To calculate the input filter capacitor, we need to calculate the peak voltage of the DC bus at minimum line voltage, then by calculating the discharge time and the rms current of the circuit, we can calculate the required capacitor value.

$$V_{DC\min pk} = V_{AC\min} \times \sqrt{2}$$

$$\text{discharge time } t_D = \frac{1}{2f_{line}}$$

We are assuming a worst case here that the capacitor has to hold up from one peak to the next of the fullwave rectified DC voltage. This is longer than in reality but gives a conservative value for the capacitor to improve the ripple voltage.

$$C = \frac{I_{Prms} \times t_D}{V_{DCRIPPLE}} \text{ where } V_{DCRIPPLE} \text{ is the value we specified at the beginning}$$

This gives the value of capacitor, the voltage rating is taken from the calculation of the $V_{DC\max}$ in section 2.5)

2.7) OUTPUT RECTIFIERS (D6,D2)

In a discontinuous flyback power supply the output rectifiers are subject to high peak and rms currents. The peak reverse voltage is a function of the maximum input voltage and the transformer turns ratio.

Minimum current rating = I_{srms} calculated in section 2.4)

$$V_{Drev} = V_O + \left[V_{DC\max} \times \frac{N_S}{N_P} \right]$$

V_{Drev} is the minimum voltage rating for the diode. The output rectifiers are usually the source of the most power dissipation in a flyback converter, so the main high power outputs should be designed to use Schottky diodes to reduce the conduction losses. The bias winding and low power auxiliary windings can commonly use very small fast switching diodes e.g. 1n4148 depending on the current and voltage rating calculated.

2.8) OUTPUT CAPACITORS (C7)

The output capacitors in flyback circuits are subject to high rms and ripple currents due to the high peak currents in a discontinuous design, so care is needed to make sure they are specified correctly to ensure

reliability and lifetime are not compromised.

There are a number of important factors when specifying the output capacitors. They are:

- 1) Capacitance Value
- 2) Ripple Current
- 3) Low ESR
- 4) Temperature of operation (85°C or 105°C)
- 5) Lifetime
- 6) Voltage rating

First we need to calculate the value of capacitor using the following equation

$$C_O = \frac{I_O \times 10}{V_{O\text{ripple}} \times f_{\min}}$$

where I_O is the full load output current, f_{\min} is the minimum operating frequency of the IRIS device, and $V_{O\text{ripple}}$ is the desired output ripple voltage.

The ripple current $I_{O\text{ripple}}$ for the output capacitor is calculated from:

$$I_{O\text{ripple}} = \sqrt{I_{s\text{rms}}^2 - I_O^2}$$

where $I_{s\text{rms}}$ is the secondary rms current calculated during the transformer design process in section 2.4). Commonly the desired capacitor value and voltage rating required give a capacitor with a ripple current rating lower than what is required, so it may be necessary to either increase the voltage rating of the capacitor or use a number of capacitors in parallel to achieve the required ripple current.

2.9) OUTPUT FILTER (L2,C9)

The output filter is a simple LC filter consisting of L2 and C9 in the typical circuit. We need to design the filter to have a cutoff frequency much lower than the operating frequency, so that it will effectively reduce the switching noise observed at the output. However there is another factor which needs to be taken into account, due to the fact that the main output capacitor is before the filter. The filter capacitor C9 will tend to supply current to the circuit particularly under transient conditions as L2 will limit the transient current from the main output capacitor C7, so C9 should also be a low ESR, high ripple current capacitor, and the value should be set so that it is not significantly lower than the main output capacitor C7 or this will lead to significant ripple current in C9. A good rule is to set the filter capacitor C9 to be approximately half the value of the main output capacitor C7. Therefore the required filter inductor value can be calculated from:

$$L_F = \frac{1}{4\pi^2 f_c^2 C_F}$$

where L_F and C_F are the filter components, and f_c is the desired cutoff frequency of the LC filter. A good value to use here is in the range of 5-10kHz for a minimum operating frequency(f_{min}) of 50-100kHz.

2.10) Vcc COMPONENTS (R3,C6)

Resistor R3 is required to provide the startup bias for the IRIS40xx. This is needed to start the circuit until the bias winding comes into play and continues to supply the Vcc power. C6 needs to be selected to be a value large enough to sustain the Vcc voltage above the UV-(negative undervoltage lockout threshold) level until the bias winding start supplying power.

The minimum current required by Vcc during the startup period is the worst case quiescent current which is 400 μ A. It is better to add a small amount to this to allow for the leakage in C6 also so 450 μ A would be a better value to work with. This current needs to be supplied at the lowest Line voltage so R3 value can be calculated from:

$$R3 = \frac{V_{DC\min} - V_{bias}}{I_{qcc\max}}$$

For C6 if we assume it takes approximately 5ms for the bias winding to start supplying power we can calculate the value of C6 required. Working on worst case conditions, the $I_{cc\max}$ operating current is 30mA, and a starting voltage of 16V, and a UV- level of 11V. C6 can be calculated from:

$$C6 = \frac{I_{cc\max} \times \Delta t}{\Delta V}$$

Where $\Delta t = 5ms$, and $\Delta V = 16-11=5V$ from the above data. This equation will give a minimum value, select the next largest available standard value. Note using a large value for this capacitor will result in a long start delay at low line, so it is best to use the next largest value in favour of putting a very large value in here for C6.

2.11) CURRENT SENSE CIRCUIT(R6, R7,C5, D5)

R7 is the main primary current sensing resistor. R6 and C5 form a filter to filter out the current spike at switch on of the FET, due to the charge stored in the resonant capacitor C3, and the winding capacitance of the transformer. D5 is commonly a small schottky diode used to clamp the source pin to ground in the possible case of a negative voltage at the source.

R7 is calculated from:

$$R7 = \frac{0.78}{I_p}$$

where I_p is the peak primary current from section 2.4), and the 0.78 is the V_{TH1} of the IRIS devices.

For D5 a small 1A 30V schottky diode is usually sufficient, and may not be needed in most cases. R6 is commonly set to a value in the range of 500 to 1kOhms. The reason for this will be seen later.

C5 is selected to form a low pass filter with R6. Set to have a 3dB frequency of 500kHz, this ensures the 3dB point is higher than the maximum switching frequency of the power supply, but will stop spurious high frequency noise from entering the FB pin.

By setting the cutoff frequency and the R6 value, C5 can be selected from:

$$C = \frac{1}{2\pi \cdot f_c R}$$

2.12) DELAY CIRCUIT(D3,D4,C4,R5)

The delay circuit is used to feedback the quasi-resonant signal from the bias winding to the FB(feedback) pin, it also is used to provide the 1.35mA holding current for the internal latch in the IRIS40xx.

Diodes D3 and D4 are simply low voltage fast switching diodes, so typically a 1n4148 type or equivalent would be sufficient. If we look at the equivalent circuit for the delay circuit it will look like the circuit shown in fig2) below (ignoring the capacitor C4).

From this equivalent circuit we can now calculate the required value for R5 from:

$$R5 = \frac{V_{CC} - (V_{D3} + V_{D4} + ((I - 1.35mA) \cdot (R6 + R7)))}{I}$$

Where I is the total peak delay circuit current, and we would set this to 5mA.

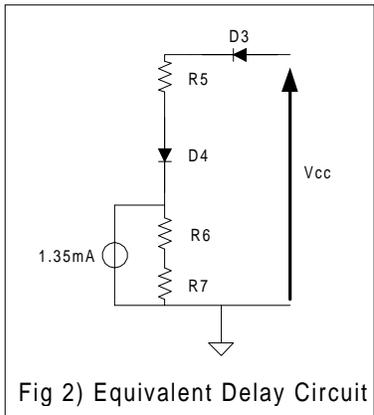


Fig 2) Equivalent Delay Circuit

2.13) SNUBBER NETWORK(D1,C10,R11)

To calculate the requirements of the snubber circuit we need to know the leakage inductance of the transformer. An easy way to specify this is to specify it as a percentage of the primary inductance. Another option is to actually measure the leakage inductance at the primary by shorting the secondary windings. This would give a good result if the transformer construction is consistent and a good LCR meter is used.

The required snub voltage is calculated from:

$$V_{snub} = V_{DSS} - V_{DCmax} - V_R$$

where V_R is the allowed reflected voltage from secondary to primary.

Usually we would set this value to be about 100V.

The diode needs to be able to block a minimum voltage of the snub voltage+the maximum DC bus voltage, so:

$$V_{D3} > V_{snub} + V_{DCmax}$$

the current rating does not need to be large as the rms current in the snubber is usually relatively small, so a 1-2A diode would be commonly used. The diode needs to be a fast recovery type to reduce the reverse current flow when the FET in the IRIS40xx turns on.

We can also calculate the snubber capacitor and resistor from:

$$C_{10} = \frac{I_P^2 \times L_{LK}}{(V_R + V_{snub}) \times V_{snub}}$$

$$R_{11} = \frac{(V_{snub} + V_R)^2 - V_R^2}{0.5 \times L_{LK} \times I_P^2 \times f_{DCmax}}$$

where f_{DCmax} is the frequency at the maximum DC bus voltage. As a general rule the f_{DCmax} is 2x the f_{min} .

2.14) VOLTAGE CONTROL LOOP(OP1,R4,D1,R8,R9,R10,C11)

The voltage control loop of the circuit in fig 1) uses an LM431 precision shunt regulator to provide the output voltage control. This method provides the best possible accuracy in the output voltage, but there are alternatives, for example a simple zener diode could be used in place of the LM431, and the zener diode could even be used on the bias winding to reduce cost, by eliminating the optocoupler, but this method gives much lower accuracy, because it is dependent on the coupling between the bias winding and the secondary winding.

For the purpose of the calculations here we will use the circuit from fig 1). First of all we have fixed the optocoupler gain at 1. R9 and R10 are calculated based on a simple voltage divider off the output voltage to the reference voltage of the LM431, such that:

$$R9 = R10 \left[\frac{V_o}{V_{ref}} - 1 \right]$$

where V_{ref} = 2.5V for the LM431. R10 can be set at a value and R9 calculated from there (R10 should be a minimum of 1kOhms).

The maximum feedback current is dependant on the value of R6, and now we will see why we set this

value to be in the range of 500 Ohms to 1kOhms.

Lets set R6 to 680 Ohms, then the maximum feedback current from the voltage control loop is set by R6 and the Vth1 of the IRIS40xx device (which is 0.78V typ). Therefore I_{FBmax} is calculated from:

$$I_{FBmax} = \frac{V_{th1}}{R6}$$

So in the case above the I_{FBmax} is 1.15mA.

To calculate R8 we use the maximum forward current for the diode in the optocoupler, its forward voltage , the reference voltage and the output voltage so that:

$$R8 \geq \frac{|V_O - [V_{FDopto} + V_{ref}]|}{I_{Fmax}}$$

By look at the current/collector voltage characteristic of the optocoupler we can find out what the voltage across the transistor will be for the maximum feedback current at I_{Fmax} , and hence we can calculate the required value of R4 from:

$$R4 = \left(\frac{V_{CC} - V_{CEopto}}{I_{FBmax}} \right) - R6$$

The last step is to stabilize the control loop, as it has to deal with the phase shift caused by crossing the transformer boundary, and this is easily achieved with the capacitor C11, which usually needs to be in the range 0.01 to 0.1uF. This is a great simplification as much more can be done to accurately model the response of the control loop, its poles and zeros, and accurately compensate for these, but usually the above approach is sufficient.