International
IOR Rectifier

APPLICATION NOTE

Application Note AN-1016

Hermetic Surface-Mount Discrete Semiconductor, Solutions to Assembly Integration

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This application note discusses the reliability and ruggedness issues of the ceramic leadless chip carrier (CLCC), SMD and TO-25x hermetically sealed packages for high reliability design applications.

Introduction

A hermetically sealed package is generally required to house a semiconductor device to insure the device's reliability and ruggedness for high reliability design applications. Typical semiconductor devices are MOSFETs (metal-oxide-semiconductor-field-effect-transistors), bipolar transistors, Schottky rectifiers, PN junction diodes, and insulated gate bipolar transistors (IGBT). Hermetic surface mount packages, leadless chip carriers (also known as LCC or CLCC) have served this function well and have been in existence for more than 20 years. While the leaded packages (TO-257, TO-254, etc.) continue to find their use in many current designs, a vast majority of new electronic equipment designs have been integrating new surface mount packages, taking advantage of its smaller size, lighter weight, and the excellent thermal performance that the new surface mount packages (SMD) offer. Many high frequency circuit designs benefit from the inherently low inductance and low resistance these packages provide. In many instances, the new SMDs are the absolute requirement. Figure 1 shows the hermetically sealed packages that are discussed in the article, the ceramic leadless chip carrier (CLCC), the new SMD and the leaded TO-25X packages.

Successful assembly integrations of plastic SMD devices are well established because of the temperature coefficient of expansion (TCE) of the package is comparable to the industry's standard board materials, FR-4 and polyimide to which the devices are mounted. Additionally, the temperature range, coldest to hottest temperature extremes where most assemblies with plastic SMD's are required to operate, are generally benign.

Unlike the plastic SMD, the popularity of the hermetic SMD devices has been somewhat hindered by the TCE incompatibility of the SMD package and the board materials, and significantly wider operating temperature demands. A soldered joint of a device to a PC board assembly can crack when it is subjected to temperature extremes, i.e., during a soldering operation, environmental stress screening (ESS) or temperature cycling screens. The ESS and temperature cycling screens simulate the assembly's operating environments prior to flight missions.

Solutions to the hermetic SMD assembly integration will be presented in this article. With the availability of low TCE (temperature coefficient of expansion) board materials, advances in materials, innovative SMD carrier designs, and maturity of the power module assembly technology, the hermetic SMD devices can be now successfully and economically integrated in most of system designs. This article will focus on the new generation hermetic surface mount packages hereafter referred to as 'SMD'.

CLCC SMD TO-25X

Figure 1. Hermetically Sealed Packages (drawing is not to scale)

New Surface-Mount Package Construction

The new hermetic SMD package consists of three terminal pads, a ceramic housing, a seal ring, and a lid. Figure 2 depicts the package structure. To insure the package's integrity, the package materials are carefully chosen to closely match the TCE of the silicon die, which has a TCE of 4.2 ppm/°C. Table 1 lists TCE property of these materials. To minimize weight while achieving package's ruggedness, the SMD package uses relatively low mass density material in ceramic alumina (Al_2O_3) for housing. Higher mass density alloys are used as needed to insure mechanical ruggedness, Kovar for lid and seal ring, and copper-tungsten (CuW) for terminal pads. Additionally, package piece parts are shaped to eliminate excess material without compromising the mechanical integrity. These piece parts are brazed together to form a hermetic, semiconductor die housing. This results in smallest and lightest possible packages.

As illustrated in Figure 2, two smaller pads are gate and source terminals of a MOSFET device or anode terminal(s) for a rectifier. A semiconductor die is soldered to the large terminal pad. This is typically a drain terminal for a MOSFET device or a cathode terminal for a rectifier. It also serves as a thermal path to an external heat sink. The thin structure of the pad provides a very short thermal path from the heat source (die) to an external heat sink. Combined with the outstanding thermal conductivity property of CuW, the package produces a very low thermal resistance path, thus a very low package junction-to-case thermal resistance (θ_{JC}).

The SMD's are a three-terminal device. The CLCC packages do offer up to 40 terminals in larger sizes and as low as 3 terminals in a very small package. SMD package differs notably from its predecessor, the CLCC surface mount package. One major difference is in the package base design where the CLCC uses tungsten feed-through or metalized solid alumina (Al_2O_3), and as stated previously the SMD uses a thin slice of CuW to minimize the package thermal resistance. This results in θ_{JC} improvement of about 60%, 1.67 °C/W for SMD .5 and about 4.5 °C/W for an equivalent CLCC with a same die size. With low θ_{JC} and larger pad sizes, SMD's find most of their use in higher current and higher power applications. Conversely, the use of CLCC packages is limited to low current and low power applications.

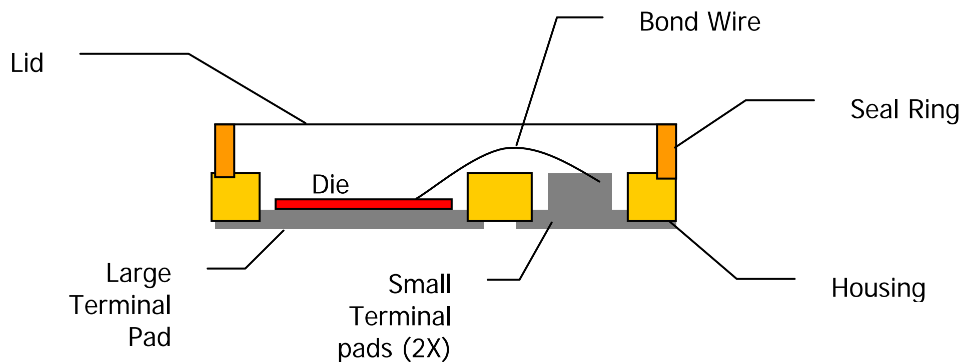


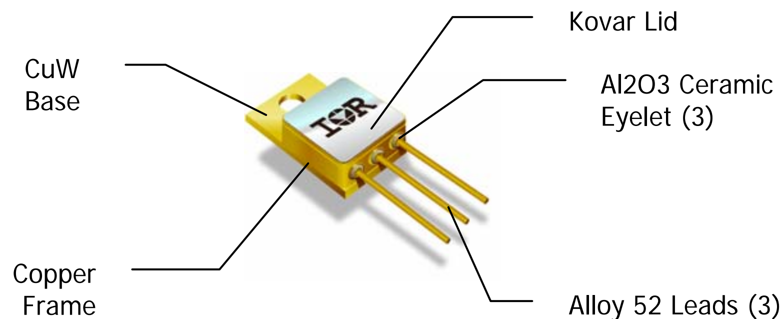
Figure 2. SMD Package, Cross-Sectional View (drawing is not to scale)

Device Elements	Material	TCE (ppm/°C)
Die	Silicon	4.2
Terminal Pads	CuW	6
Housing	Al2O3	6.4
Seal Ring	Kovar	5.1
Lid	Kovar	5.1

Table 1. TCE Property of Package Elements

TO-25X Package Construction

Figure 3 illustrates the construction of the leaded style TO-25X packages. The package uses relatively high mass density materials such Kovar for the lid and seal ring, copper for frame, metalized BeO for substrate (not shown), alloy 52 for leads, and copper-tungsten for base. The packages are sized to facilitate die assembly and to accommodate internal leads extension. Moreover, external space is required for leads extension. All these factors result in a larger and heavier package than a comparable SMD package. While the base of a TO-25X package is more than 3 times the thickness of the SMD's, .050″ vs. .015″, their thermal resistances are however, comparable.



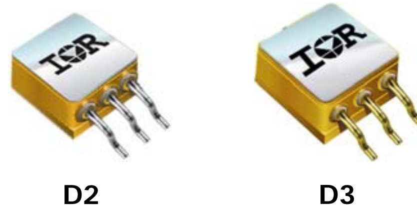
Note: Substrate is attached to the base internally and it is not shown.

Figure 3. TO-25X Package Construction

D2 and D3 Packages

D2 and D3 packages are basically tab-less TO-257 and tab-less TO-254, respectively. They are now available as standard package options. These packages use similar package materials and have the same basic construction as the TO-257 and TO-254, but have smaller footprints than their counterparts. The other difference is the leads configuration where leads of D2 and D3 packages are formed for surface-mount assembly. Refer to Figure 4 for these packages. Weight, thermal resistance and foot print data of various SMD's and leaded styles including the new D2 and D3 packages are shown in Table 2.

While their availability has somewhat reduced the weight and footprint disparities between the SMD and TO-25X, these improvements are not expected to slow the use of SMD packages for new designs.



D2 D3

Figure 4. D2 and D3 packages

PACKAGE	WEIGHT typical (grams)	FOOT PRINT		θJC (C/W) (1)	Package Style
		(mm^2)	(in^2)		
SMD .5	1.1	76	0.118	1.67	Surface-mount
SMD 1	2.6	181	0.281	0.83	Surface-mount
SMD 2	3.3	234	0.362	0.42	Surface-mount
SMD 3	3.4	250	0.387	0.42	Surface-mount
D2	3.45	165	0.256	1.67	Surface-mount/Thru-hole
D3	7.2	286	0.444	0.83	Surface-mount/Thru-hole
TO-39	0.98	267	0.414	8.3	Thru-hole
TO-257	7	219	0.340	1.67	Thru-hole
TO-254	9.3	336	0.521	0.83	Thru-hole
TO-258	10.9	447	0.693	0.42	Thru-hole
SMD 1&2 Carrier	1.7	391	0.606	0.25	Surface-mount

Note: 1) Die size dependent. A typical die size is assumed for each package.

Table 2. Weight, thermal resistance and foot print data of all package options discussed in this article.

Low Ohmic TO-257, TO-254, D2 and D3

The latest package innovation is the improvements in package resistance. The new low ohmic versions are now available in TO-254, TO-257, D2, and D3 packages. The package resistances are as low as 1 milliohm for TO-254 and D3 packages, and as low as 2 milliohms for TO-257 and D2 packages. This major improvements stem from the change in lead material from Alloy 52 to copper zirconium, and the addition of a copper plate over the metalization of the substrate.

While the improvement offsets the package resistance advantage the SMD has over an equivalent leaded package, the advantages in inductance, footprint, and weight remain.

Benefits of SMD over Leaded Packages

1) Size and Weight Benefits

Comparisons of the commonly used packages are shown in figures 5, and 6. A same die size is used for each comparison. SMD .5 is compared to TO-257 and D2. SMD 1 is about twice the size of the SMD .5 and is compared to TO-254 and D3. SMD 2 and SMD 3 are the largest packages of the family. While SMD 2 is commonly used for a single device design, SMD 3 lends itself to high current applications where its pads layout simplifies board layout when two or more devices are paralleled. Either SMD 2 or SMD 3 package may replace TO-254 or D3 package.

In all instances, the comparisons clearly demonstrate that the SMD packages are significantly lighter and will occupy considerably less board space than their leaded counterparts. As much as 84% weight reduction is realized when SMD.5 is used in place of TO-257 and as much as 65% in foot print reduction. While the leaded parts have a thicker base and include a BeO substrate and the SMD's have thinner base and are without a substrate, the packages' thermal resistances are virtually the same for SMD .5, D2 and TO-257 packages.

If a carrier is required and is included as part of the assembly of SMD 2, the weight reduction benefit reduces slightly from -65% to -46%. And that the carrier's footprint actually takes more packaging space than the TO-254, from -31% to +16%. Figure 7 shows these comparisons. It will be noted later however, that an SMD device may be the package of choice due to its electrical performance benefits.

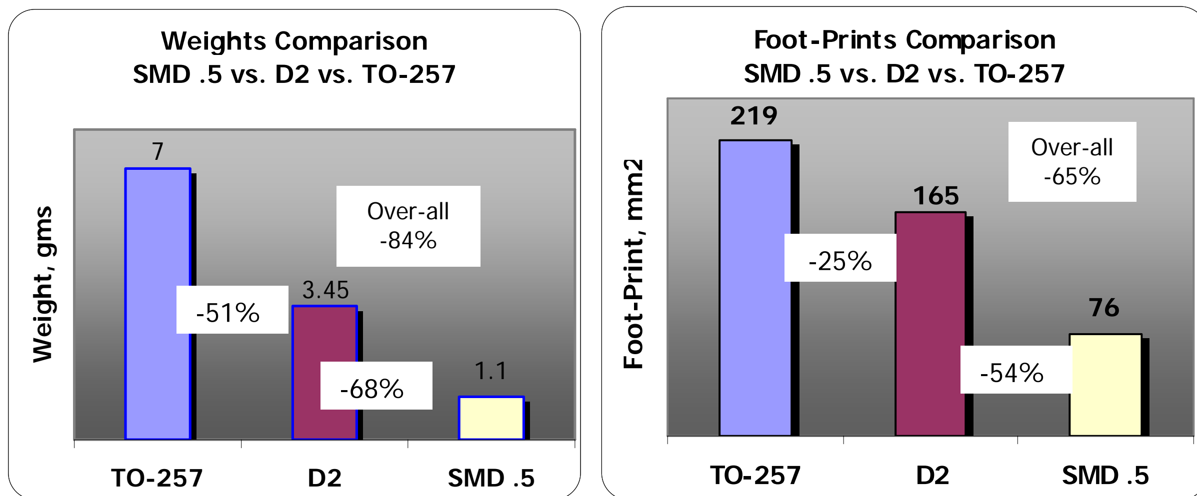


Figure 5. Weight and Foot Print Comparisons, SMD .5 vs. D2 Vs. TO-257

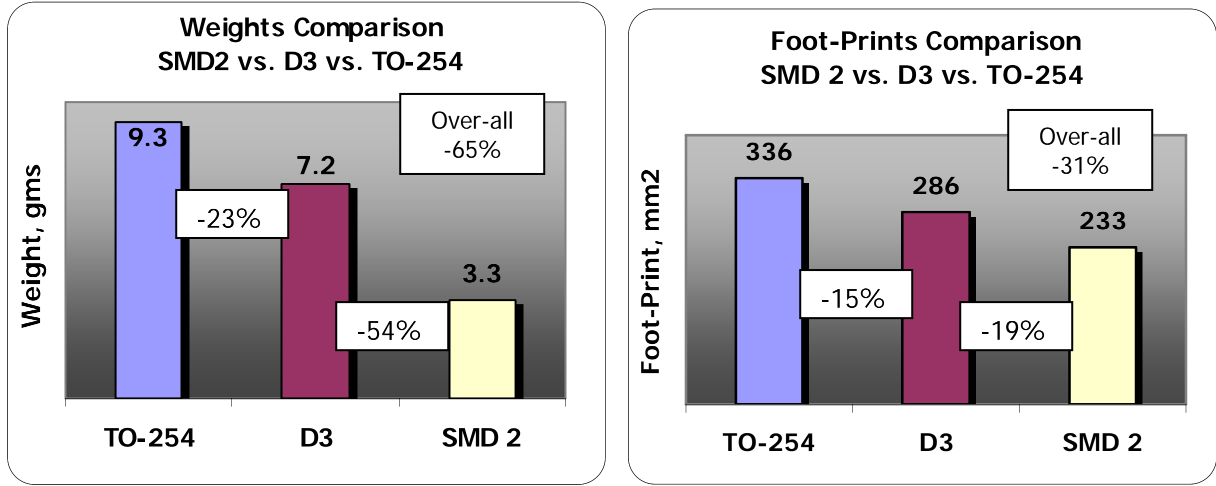


Figure 6. Weight and Foot Print Comparisons, SMD 2 vs. D3 and TO-254

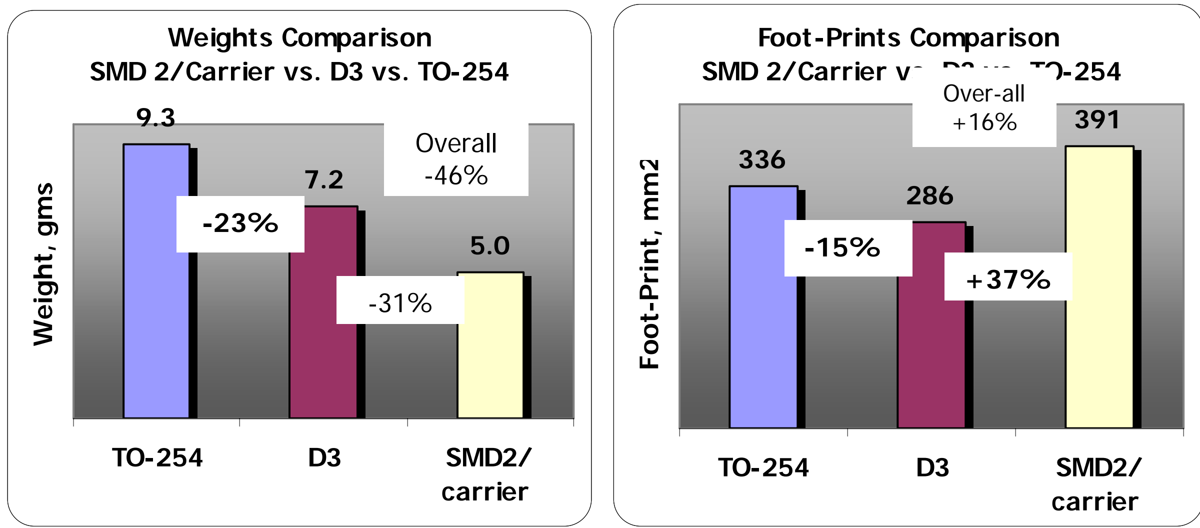


Figure 7. Size and Weight Comparisons of SMD 2 on a carrier vs. D3 and TO-254

2) Electrical Performance Benefits

Inductance and Resistance

SMD, due to its low package resistance and low lead inductance, provides excellent electrical performance especially in high frequency switching applications. Table 3 lists typical lead inductances and package resistances of the popular packages. Note that these values are a function of internal bond wires and internal package structure. They may vary greatly depending wire length, wire size, number of wires

used, substrate metalization, and lead material. External lead length of 0.25 inch is included in the analysis for leaded packages, D2 and D3. The package resistances of the SMD styles are significantly lower than their leaded counterparts. However, the low ohmic versions of TO-254, TO-257, D2, and D3 are now available and have markedly narrowed this disparity. While their package resistances represent substantial improvements, their lead inductances remain the same as the TO-257, TO-254, D2, and D3 packages.

PACKAGE	Package Resistance, typ. (mohms)	Inductance, typ. (nH)		
		Drain Lead	Source Lead	Package Total
SMD .5	1.3	-	-	4
SMD 1	0.4	0.8 - 2	2.8 - 4.1	4- 6
SMD 2	0.5	0.8 - 2	2.8 - 4.1	4- 6
SMD 3	0.1	0.8 - 2	2.8 - 4.1	4 -6
TO-254/D3	6	5 - 8.7	8.7 - 15	15-23
TO-257/D2	8	5 - 8.7	8.7 - 15	15-23
TO-258	5	5 - 8.7	8.7 - 15	15-23
Low Ohmic TO-257/D2	2.5	5 - 8.7	8.7 - 15	15-23
Low Ohmic TO-254/D3	1	5 - 8.7	8.7 - 15	15-23
SMD 1&2 Carrier	0.2	-	-	2

Table 3. Typical Values of Package Inductance and Resistance

Skin Effect

In switching applications, skin effect can cause AC losses in the leads of the package, and in some designs these losses can be greater than DC (resistance) losses. Leads of a TO-25X package contain ferromagnetic materials. Magnetic field is generated as current passes through the leads. Eddy currents induced in the leads by the magnetic field cause skin effect. Skin effect causes current in a lead to flow only on the outer periphery of the leads. The depth of this annular conducting area is inversely proportional to the square root of the frequency[1].

For a 40 mils diameter lead (wire size of TO-254), the ratio of AC resistance to DC resistance at 50 KHz is about 1.35. The ratio increases to 1.75 (~29%) as the frequency rises from 50 KHz to 100 KHz. The resistance ratio is also a function of the lead's diameter. The resistance ratio increases as the lead's diameter increases. Increasing the lead's diameter from 40 mils to 60 mils (TO-258), the AC resistance to DC resistance ratio increases by about 50% at the frequency of 100 KHz[1]. The AC losses will further reduce the circuit efficiency.

In most assembly configurations, an SMD package lends itself to layouts where components are in close proximity yielding short circuitry interconnections. This results in low circuit resistance, low circuit inductance and negligible AC losses which improve the circuit efficiency and produce cleaner switching waveforms, which reduces components size of snubber circuits.

SMD Assembly Integration Design Guidelines

When integrating SMD devices to an assembly design, TCE of the board/substrate material must be closely matched to TCE of the SMD's, typically within 2-3 ppm/°C to minimize mechanical stress and to insure the mechanical integrity. Additionally, proper cooling must be provided to insure that the devices' operating junction temperatures are maintained below the desired level under the worst-case condition. A device's thermal characteristics, θ_{JC} and θ_{JA} (junction-to-ambient thermal resistance) are essential and must be considered in the design process.

Low Power Designs

For semiconductors with low power dissipations (less than 0.5 watt) in the SMD and CLCC style packages can be attached directly to the traditional FR-4 or polyimide printed wiring board (PWB). However, due to considerable TCE mismatch, this assembly integration is limited to small outline packages where the largest package dimension is less than .4". Assembly's mechanical integrity depends greatly on the exact board configuration, device package style/dimensions, and solder used for device attachment. To insure a successful assembly design and integration, actual board design and the selected SMD packages must be assembled and subjected to the simulated qualification environments.

For designs with larger SMD/CLCC packages, low TCE board materials are the solution. Board materials with TCE of 7-9 ppm/°C are now available. Other TCE control techniques for a printed wiring board include the use of molybdenum or copper-invar-copper as the board stiffener. For larger CLCC packages, gull-wing leads (J or L lead style) can be attached to provide a stress-relief with excellent success. Figure 8 depicts the gull-wing leads attachment for a CLCC package.

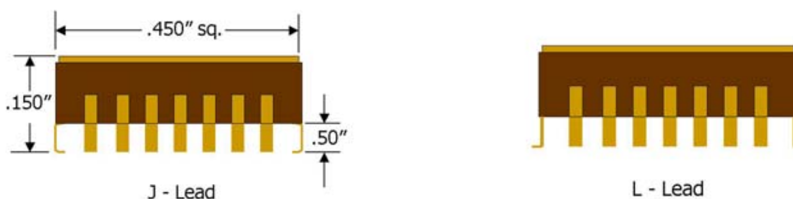


Figure 8. CLCC Gull-Wing Leads Attachment

SMD can be bonded to a board with a silver filled epoxy or with a soldering process. For an attachment using solder, eutectic alloys should be used. Preheating of assembly prior to soldering and allowing the assembly to cool naturally after a soldering process, are highly recommended. Exposing the SMD components to temperatures in excess of 300°C is prohibited. Permanent damage to the SMD components may result.

Since most printed wiring board materials, i.e. FR-4, polyimide, are poor thermal conductors, the PWB should not be considered as a thermal medium or heat spreader for cooling a device unless the copper traces are sufficiently large, or that the board is designed to remove heat, i.e., via the copper inner layers which in turn are fastened to a heat sink or chassis for heat removal. Otherwise, it is clear that the cooling of this device relies almost entirely on the package's ability to dissipate thermal losses in the free convection environment. The package's θ_{JA} then becomes the key design parameter. For space environments where convection is nonexistence and radiation cooling is minimal, conduction is the only effective method of cooling. The board assembly must include means of cooling an SMD or CLCC for an on-board assembly design.

Design Example:

For a device dissipating .5 watt and θJA of 50 °C/W, the junction temperature (TJ) shall equal 100 °C for an ambient temperature (TA) of 75°C. This is based on the formula PD = [TJ – TA]/θJA, where PD is the device's power dissipation, TJ is the operating junction temperature, TA is the ambient temperature, and θJA is the package's junction-to-ambient thermal resistance.

High Power Designs

For high power applications where an SMD device dissipates a few watts or more and must be cooled with a heat sink, there are two basic assembly integration techniques, which are described as follows:

1) SMD with Leads

For this assembly technique, the SMD is attached with flat copper leads for electrical connections. The device is bonded to a heat sink or a heat spreader via its lid with a thermally conductive epoxy or a thermal pad for cooling purposes. The SMD is electrically isolated from the heat sink as the lid is isolated from the semiconductor die. The junction-to-lid thermal resistance (θ_{JL}) is the critical parameter for this design approach. The junction-to-lid thermal resistances (θJL) of the SMD packages are as follows:

SMD .5 - 12°C/W.
SMD 1 - 7.0°C/W
SMD 2 - 7.0°C/W

Thermal resistance of the bonding epoxy must be included when determining the total thermal resistance of the assembly. Figure 9 depicts a typical SMD with leads, and Figure 10 illustrates the assembly integration of an SMD with leads. It is apparent that cooing of these devices via its lid is limited to power dissipation of less than a few watts depending on the T_J max design requirements, as the θ_{JL}'s are relatively high.

Another common assembly technique is to bond the leaded surfaces of the SMD directly to a heat sink with a thermally conductive epoxy or a thermal pad. Unless the bonding medium contains an insulating material, placing a thin layer of ceramic at the bonding interface will provide the required electrical isolation.

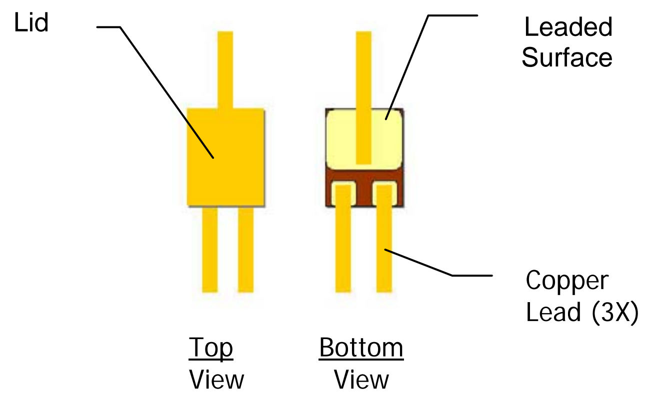


Figure 9. SMD with Leads

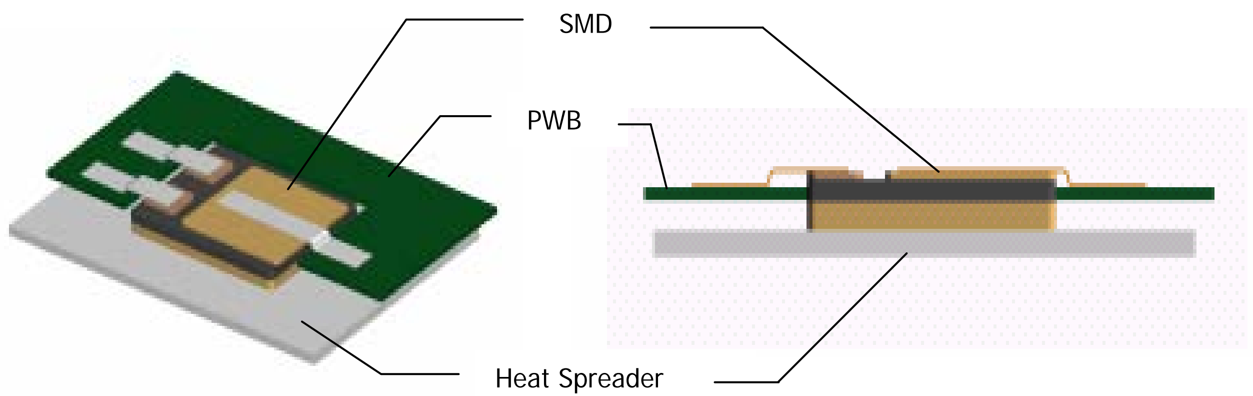


Figure 10. SMD Assembly Integration Technique with Cooling via SMDs Lid.

2) SMD Carrier Assembly

For assembly designs with one or two SMD devices, the SMD carrier may be the solution to a cost-effective design. SMD carrier is a leaded DBC substrate with three extended flat copper leads (one each for gate, drain and source terminal as in the case of a MOSFET device). An SMD device is soldered to the carrier resulting in an isolated ready-to-use SMD assembly. With its good thermal conductivity and excellent dielectric properties, the ceramic layer within the DBC provides the SMD device the essential electrically isolated thermal path with negligible impact on the overall thermal performance of the assembly. SMD carriers and assembly elements are shown in Figure 11.

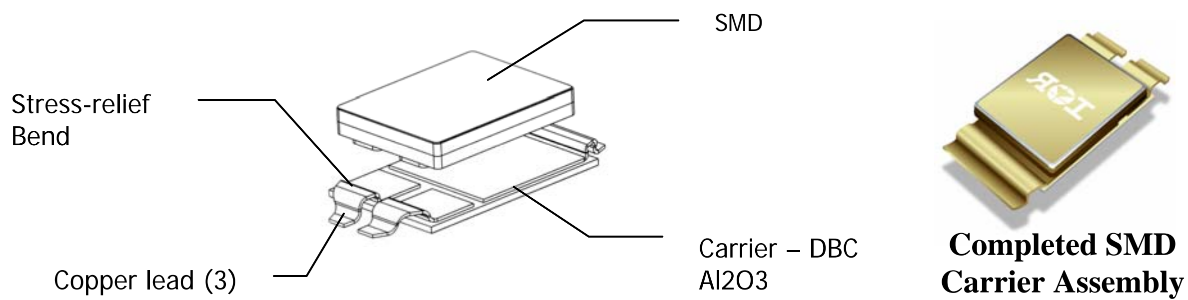


Figure 11. SMD Carrier Assembly

Figure 12 illustrates a design implementation using the SMD carrier assemblies. In this design approach, all small signal and low power components are populated on a printed wiring board assembly. The SMD carrier assemblies are bonded to a base-plate with a thermally conductive epoxy. The base or chassis is usually a thermally conductive metal such as serving as a cold plate or heat sink for the entire assembly. Electrical connections from a carrier assembly to the board are made through the copper leads of the carrier. The overall assembly's junction-to-base thermal resistance (θ_{JB}) depends on the die size, substrate material and the carrier bonding material. For a carrier assembly with SMD 2 device using size 6 die, alumina substrate, and silver-filled bonding epoxy, the θ_{JB} is about 0.8 - 1°C/W.

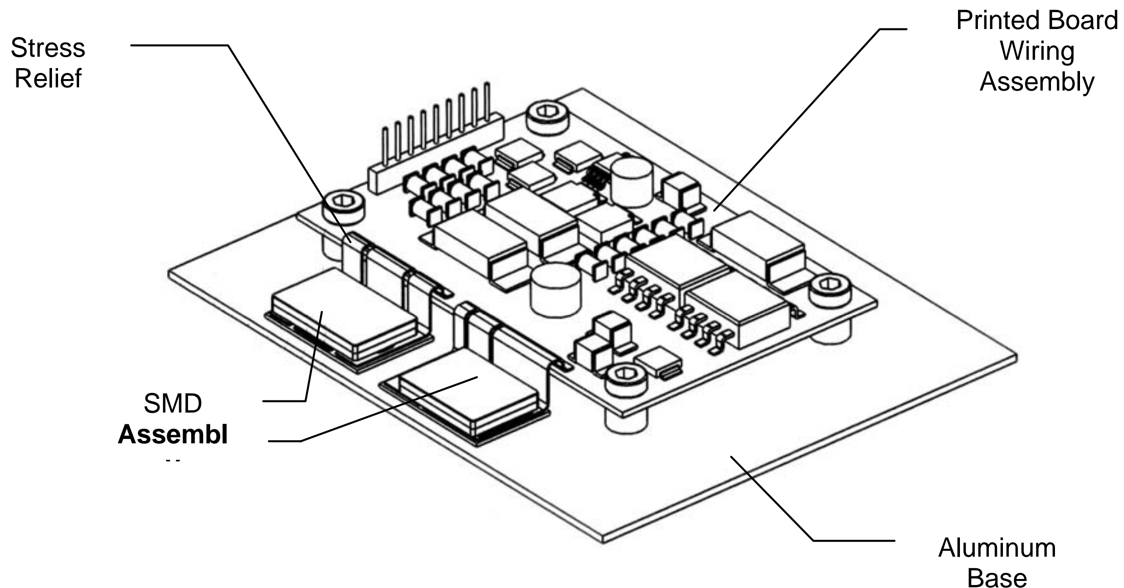


Figure 12. An Assembly Integration Using SMD Carrier Assemblies

Verification Methods for Attachment Integrity

The conventional visual inspection method cannot be used for an assembly populated with SMD devices as the soldered connections are not visible. The approved inspection methods are x-ray, sonoscan, and thermal response. If the inspection cannot be performed in-house, there are several independent laboratories that have the proper equipment and will perform the required inspection for a fee.

SMD Rework Procedure

Should replacement or re-alignment of an SMD be required, a hot air system with appropriate orifice masking to protect surrounding components may be needed. Preheating of the assembly to within 50°C of the solder's melting temperature will facilitate the rework process. Temperature must be carefully controlled and monitored when applying heat to the device to avoid permanent damage to the SMD.

Conclusions

The Hermetic SMD is the package of choice for designs that require smaller size and lighter weight assembly. Additional benefits include cleaner switching waveforms and higher circuit efficiency. Populating an SMD on a printed wiring board is limited to low power applications. For a larger SMD, board materials with a low TCE are now available to simplify the assembly designs as an SMD can be

populated directly on the board. Additionally, gull-wing leads attachment is a viable option for a CLCC package. For high power applications, there are two basic assembly integration methods. Assembly techniques include the use of an SMD with copper leads and SMD carrier assembly. These assembly integration techniques will facilitate the assembly design process and proliferate the use of the surface mount devices.

Reference:

1) A. I. Pressman, "Switching Power Supply Design," McGraw-Hill, Inc., New York