

XPhase™/DirectFET™ VRM10.1 Test Fixture DB4C

(This PRELIMINARY documentation corresponds to DB4C board Revision 4)

DESCRIPTION

The test fixture DB4C, which works with VRM10 high-efficiency demo board DB3C, consists of VRM external circuit and connector, Intel mPGA 603 CPU Socket, and Dynamic VID test circuit. The mPGA 603 socket is intended for Intel VTT tool. The test circuit generates Intel VRM 10 6-bit Dynamic VID.

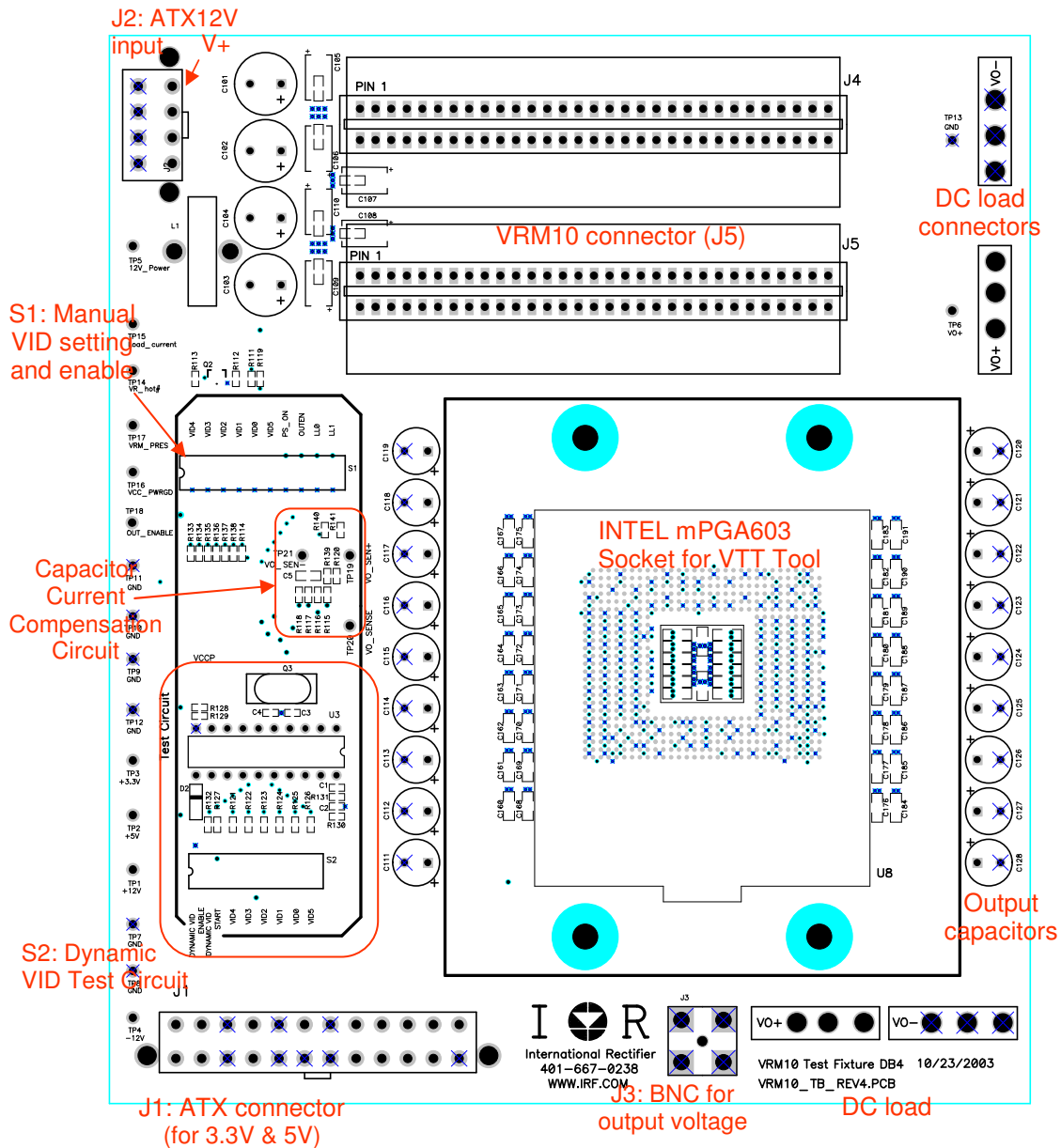


Fig. 1 DB4C Test Fixture Layout

TEST PINS AND CONNECTORS

Reference	Symbol	Description
J1	ATX	ATX 24 pin connector (compatible with 20 pin connector)
J2	ATX12V	ATX12V 8 pin 12V connector (compatible with 4 pin connector)
J3	VCCP	BNC test point for Vcore (for measuring output waveform)
TP1	+12V	12V supply voltage from J1 (not used)
TP2	+5V	5V bias voltage from J1 (required for output logic signals)
TP3	+3.3V	3.3V bias voltage from J1 (required for VID and enable signals)
TP4	-12V	-12V supply voltage from J1 (not used)
TP5	12V_POWER	12V Power supply for VRM (up to 20A input current)
TP6	VO+	Output Voltage for Vcore (same signal as connected to the BNC)
TP7-TP12	GND	Ground
TP13	VO-	Ground return of Vcore
TP14	VR_hot#	VRM over temperature signal. "Low" indicates VRM over-temperature.
TP15	Load_current	Load current indicator. Connected to IShare bus of VRM.
TP16	VCC_PWRGD	VCC power good signal. "High" indicates power good.
TP17	VRM_pres	VRM president signal. "High" indicates the presence of VRM.
TP18	OUT_ENABLE	Output enable signal. "High" indicates the VRM is enabled.
TP19	VO_SEN+	Connected to VO_SEN+ input of VRM
TP20	VO_SENSE	Connected to remote sense point of CPU socket
TP21	VO_SEN-	Connected to ground return input of VRM

DYNAMIC VID AND REGULAR VID SELECTION

A microcontroller and external circuits is used to generate the dynamic VID. Place VID0-VID5 of S1 at "OFF" position, and use switch S2 to select the VID code. Place "Dynamic VID" of S2 at "ON" position to enable the Dynamic VID function, and the LED will be lit. The waveform of VDAC voltage is shown in Fig. 2, and the slew rate of VDAC can be programmed by R113 and C100 on the VRM, which are located between VDAC pin and VOSNS- pin of IR3081.

Dynamic VID function can be disabled by turning "Dynamic VID" of S2 to "OFF" position. S2 can also be used to select regular VID if VID0-VID5 of S1 are at "OFF" position.

If the microcontroller is not plugged in, S1 should be used for VID code selection.

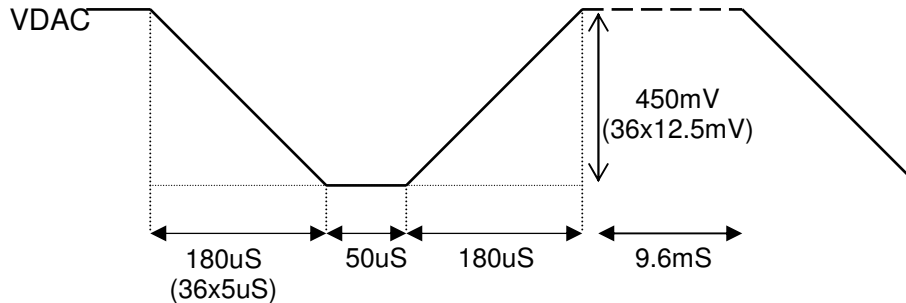


Fig. 2 VRM10.1/10.2 Dynamic VID Waveform

DIP Switch S1 (Manual VID and Controls):

Reference:	Symbol	Description
S1 Position 10	LL1	Load line control for VRM10.1 (reserved)
S1 Position 9	LL0	Load line control for VRM10.1 (reserved)
S1 Position 8	OUTEN	Output enabling. Place the switch at "OFF" position (OUTEN = high) to enable the converter.
S1 Position 7	PS_ON	ATX Power Supply ON control. Place the switch at "ON" position (PS_ON pin shorted to ground) to enable the ATX power supply
S1 Position 1-5, 6	VID4-VID0, VID5	VID code selection. Place the switch at "ON" for "0", or at "OFF" for "1". If VTT tool or Dynamic VID circuit is used to set the output voltage, place these switches at "OFF" positions.

DIP Switch S2 (Dynamic VID):

Reference:	Symbol	Description
S2 Position 1	Dynamic VID Enable	Place the switch at "ON" position to enable the dynamic VID circuit, "OFF" to manually select VID using S1
S2 Position 2	Dynamic VID	Dynamic VID selection. Place this switch at "ON" position to start the "Dynamic VID" function, and at "OFF" to use regular VID on S2.
S2 Position 3-7, 8	VID4-VID0, VID5	VID0 - VID5 of Dynamic VID. Place the switch at "ON" for "0" and at "OFF" for "1". If VTT tool or S1 is used to set the output voltage, place these switches at "OFF" positions.

Intel VRM10 COMPATIBLE 6-Bit VID

Processor Pins (0 = low, 1 = high)						Vout (V)	Processor Pins (0 = low, 1 = high)						Vout (V)
VID4	VID3	VID2	VID1	VID0	VID5		VID4	VID3	VID2	VID1	VID0	VID5	
0	1	0	1	0	0	0.8375	1	1	0	1	0	0	1.2125
0	1	0	0	1	1	0.8500	1	1	0	0	1	1	1.2250
0	1	0	0	1	0	0.8625	1	1	0	0	1	0	1.2375
0	1	0	0	0	1	0.8750	1	1	0	0	0	1	1.2500
0	1	0	0	0	0	0.8875	1	1	0	0	0	0	1.2625
0	0	1	1	1	1	0.9000	1	0	1	1	1	1	1.2750
0	0	1	1	1	0	0.9125	1	0	1	1	1	0	1.2875
0	0	1	1	0	1	0.9250	1	0	1	1	0	1	1.3000
0	0	1	1	0	0	0.9375	1	0	1	1	0	0	1.3125
0	0	1	0	1	1	0.9500	1	0	1	0	1	1	1.3250
0	0	1	0	1	0	0.9625	1	0	1	0	1	0	1.3375
0	0	1	0	0	1	0.9750	1	0	1	0	0	1	1.3500²
0	0	1	0	0	0	0.9875	1	0	1	0	0	0	1.3625
0	0	0	1	1	1	1.0000	1	0	0	1	1	1	1.3750
0	0	0	1	1	0	1.0125	1	0	0	1	1	0	1.3875
0	0	0	1	0	1	1.0250	1	0	0	1	0	1	1.4000
0	0	0	1	0	0	1.0375	1	0	0	1	0	0	1.4125
0	0	0	0	1	1	1.0500	1	0	0	0	1	1	1.4250
0	0	0	0	1	0	1.0625	1	0	0	0	1	0	1.4375
0	0	0	0	0	1	1.0750	1	0	0	0	0	1	1.4500
0	0	0	0	0	0	1.0875	1	0	0	0	0	0	1.4625
1	1	1	1	1	1	OFF ¹	0	1	1	1	1	1	1.4750
1	1	1	1	1	0	OFF ¹	0	1	1	1	1	0	1.4875
1	1	1	1	0	1	1.1000	0	1	1	1	0	1	1.5000
1	1	1	1	0	0	1.1125	0	1	1	1	0	0	1.5125
1	1	1	0	1	1	1.1250	0	1	1	0	1	1	1.5250
1	1	1	0	1	0	1.1375	0	1	1	0	1	0	1.5375
1	1	1	0	0	1	1.1500	0	1	1	0	0	1	1.5500
1	1	1	0	0	0	1.1625	0	1	1	0	0	0	1.5625
1	1	0	1	1	1	1.1750	0	1	0	1	1	1	1.5750
1	1	0	1	1	0	1.1875	0	1	0	1	1	0	1.5875
1	1	0	1	0	1	1.2000	0	1	0	1	0	1	1.6000

Note1: Fault mode, error amplifier output disabled.

Note2: Typical initial setting for the test fixture

OPERATING PROCEDURES

1. VID Selection

If the microcontroller in DIP20 socket for Dynamic VID is not plugged in, use S1 to select VID. If the microcontroller is plugged in, turn VID0-VID5 of S1 to “OFF” position and use S2 to select VID or dynamic VID.

2. Output Load Connection

Use Intel mPGA603 Voltage Transient Test (VTT) tool as the DC or AC load, or connect an external load between output load connectors VO+ and VO- . There are two set of load connectors as shown in figure 1. The test fixture can test up to 120A average current and 135A peak current.

TP6 and TP13 are for output voltage testing only, not for powering the load.

3. Input Power Connection

Connect ATX12V power supply to J2. This is the main input to the VRM and should be able to supply up to 20A current.

Connect ATX power supply to J1, and turn position 7 of S1 to “OFF” (PS_ON = high) to enable the ATX output voltage. This is just to provide bias voltages required by the logic control signals (such as OUTEN) on the test fixture and VRM.

If bench power supplies are preferred, +5V and +3.3V power should be connected to TP2 and TP3, respectively.

Under normal startup procedure, the 12V power supply should be turned on before or at the same time with other supplies.

4. Inserting and Enabling VRM

Turn off the 12V supply before inserting or removing any VRM into connector J5.

Make sure that the VRM is inserted in the correct direction. Check for the end of the VRM which has all the control signals. Align this end with the control line traces on the test fixture. (When in doubt, set the current limit to the 12V input to 1A)

Turn on the 12V supply voltage, followed by the 3.3V and 5V bias voltages.

Turning position 8 of S1 to OFF (OUTEN = high) to enable the VRM. Note that this requires the 3.3V supply voltage to be connected.

5. Observing Output Voltages

To obtain accurate Vcore output voltage, measure the voltage between TP19 and TP21 on the test fixture.

J3 (BNC) can be used to observe output voltage waveform during transient response test using the VTT.

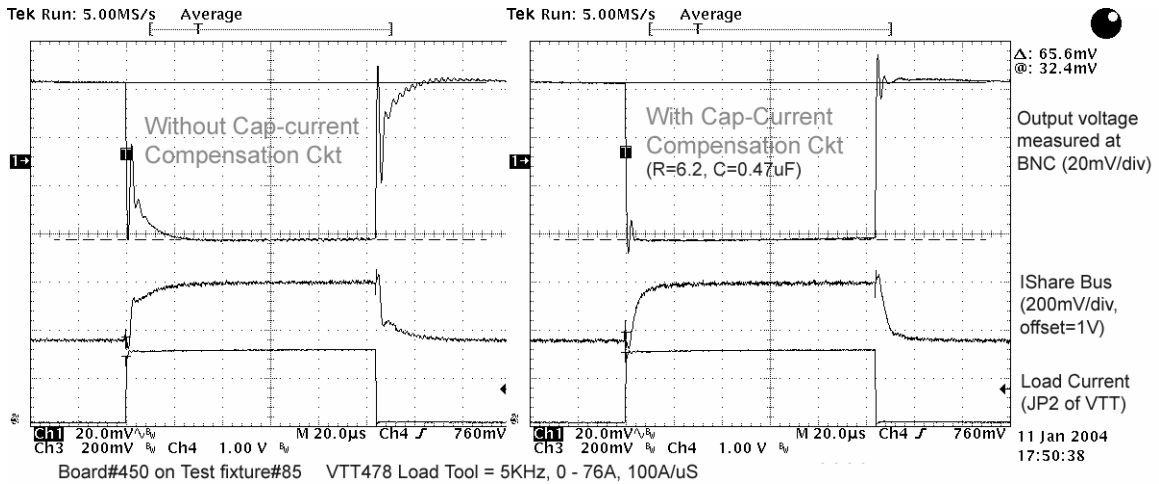
The “Power Good” signal can be observed at TP16. Note that this requires the 5V power supply to be connected.

6. Frequency Response measurement

If required, a network analyzer can be connected to TP19, TP20 and TP21 for frequency response measurements.

7. Capacitor Current Compensation Circuit

The test fixture is equipped with a capacitor-current compensation circuit that may dramatically improve the dynamic response of the VRM. The effects can be seen in the following two sets of waveforms.

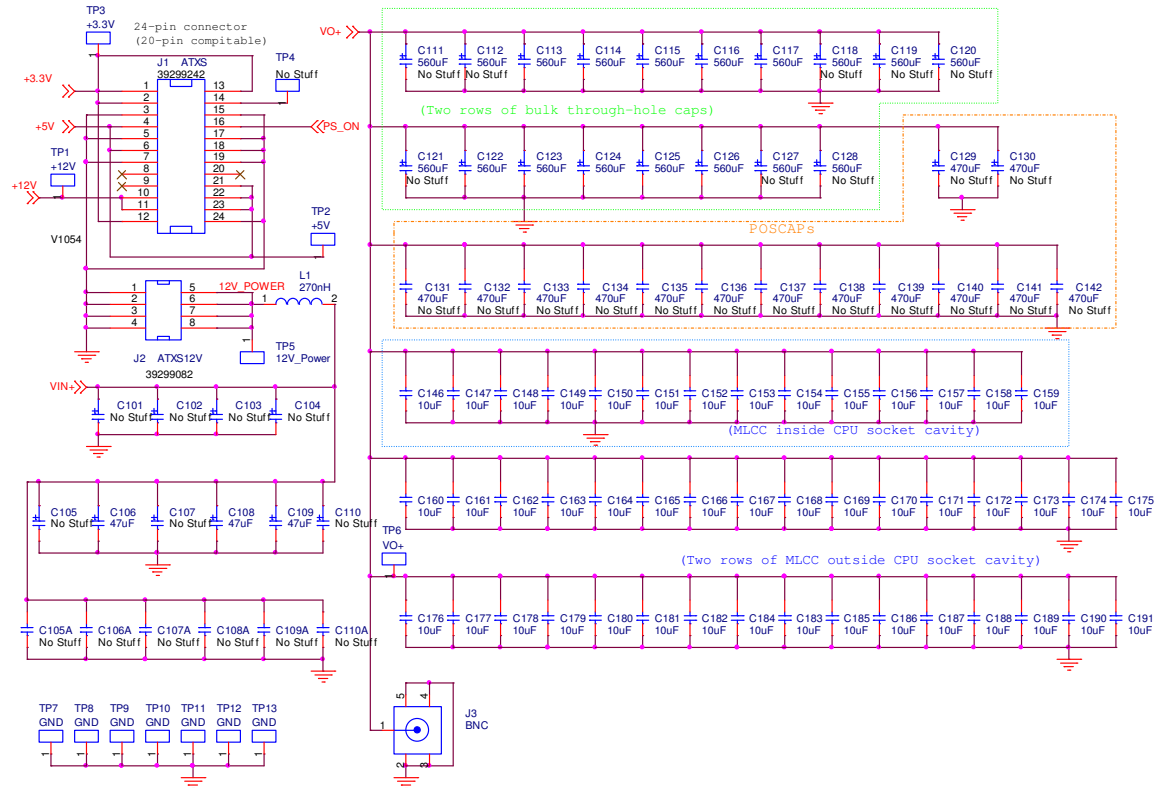


Details of the Capacitor Compensation Circuit are presented in the appendix.

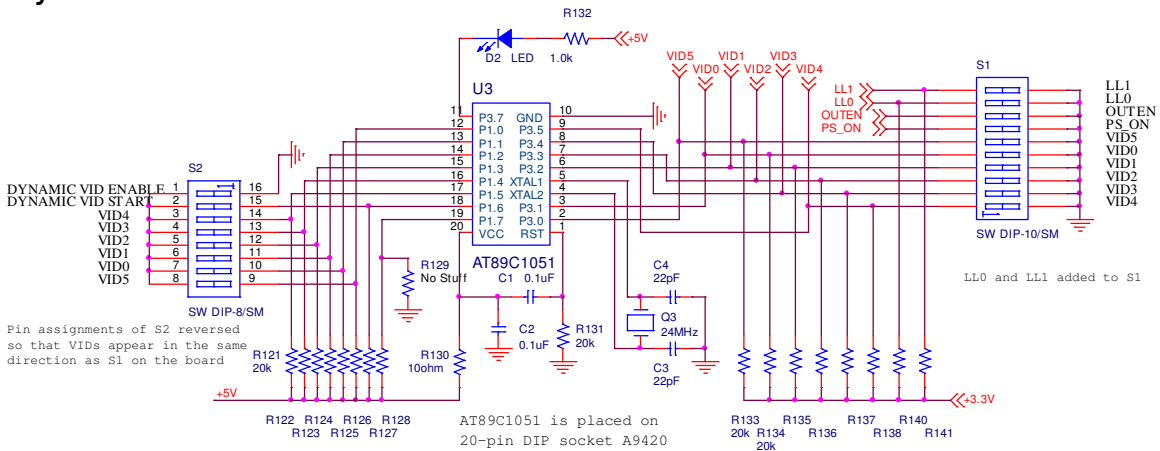
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SCHEMATIC

Power Stage

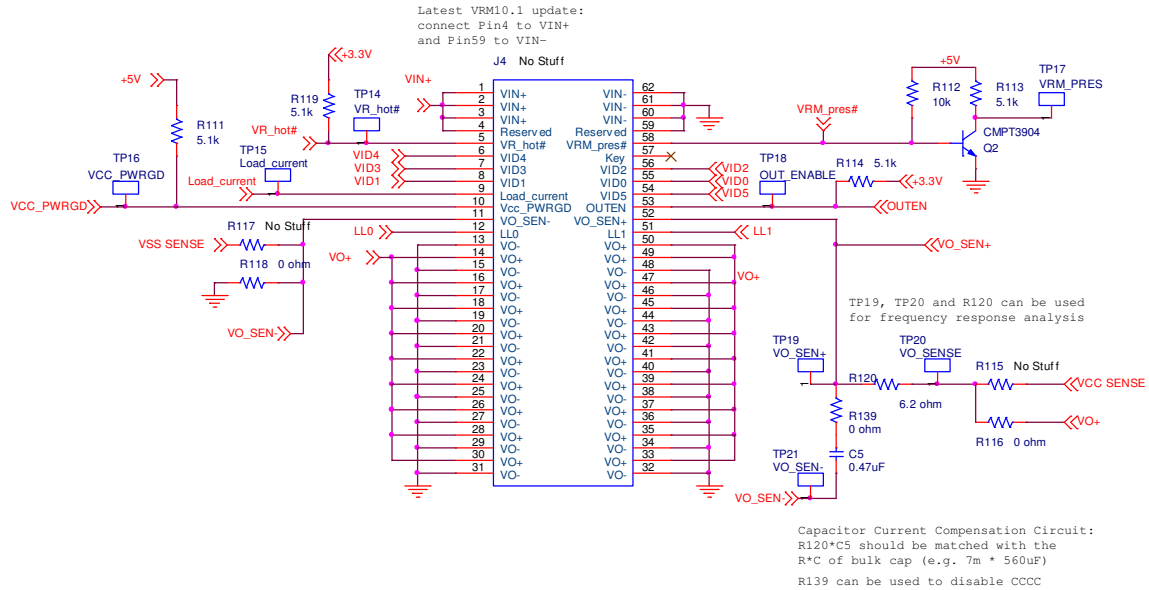


Dynamic VID

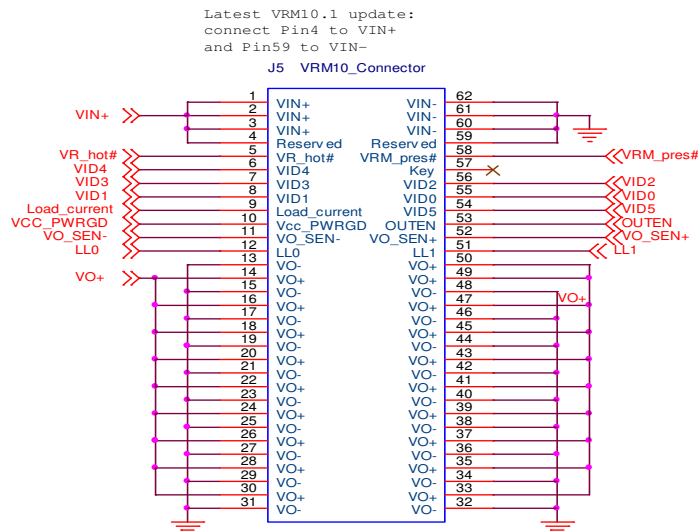


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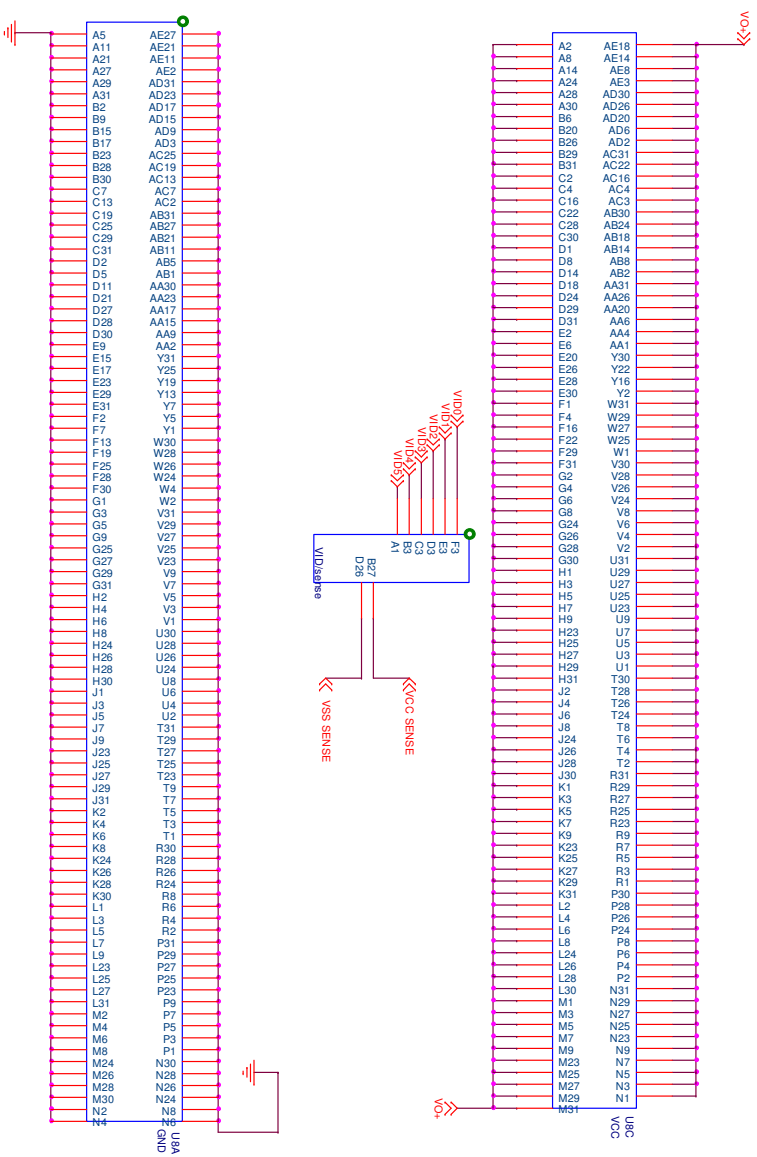
VRM 10 Connector#1



VRM 10 Connector#2



603-pin CPU Socket



BILL OF MATERIAL

VRM10 2U High Efficiency Demo Board (DB3C rev4.1). Revised: Monday, November 03, 2003

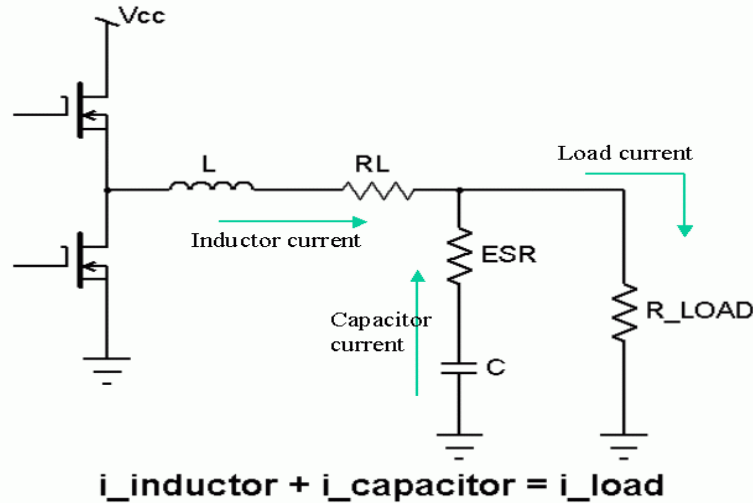
Reference	Value	Volt.	Tol	Footprint	Part Number	Vender
C1,C2	0.1uF	16V	20%	603	C1608X7R1C104M	TDK
C3,C4	22pF	16V	5%	603	C1608C0G1H220J	TDK
C5	0.47uF	25V	10%	805	C2012X7R1E474K	TDK
C101,C102,C103,C104 C109A,C110A	1500uF	16V	20%	CAP200		Rubycon
C106,C108,C109	47uF	16V	20%	7343	16TPB47M	Sanyo
C113,C114,C115,C116,C117, C122,C123,C124,C125,C126	560uF	4.0V	20%	CAP150	PSA4VB560M11	UCC
C146,C147,C148,C149,C150, C151,C152,C153,C154,C155, C156,C157,C158,C159,C160, C161,C162,C163,C164,C165, C166,C167,C168,C169,C170, C171,C172,C173,C174,C175, C176,C177,C178,C179,C180, C181,C182,C183,C184,C185, C186,C187,C188,C189,C190, C191	10uF	6.3V	20%	1206	C3216X5R0J106M	TDK
D2	LED			QTLP650	QTLP650C4CT	Digi-Key
J1	ATXS			MOLEX_24PIN	39299242	Molex
J2	ATXS12V			MOLEX_8PIN	39299082	Molex
J3	BNC			BNC	A24517-ND	Digi-Key
J4	VRM10_Con			VRM10_CON	6-530843-5-ND	Digi-Key
J5	VRM10_Con			VRM10_CON	6-530843-5-ND	Digi-Key
L1	270nH		20%	CT450	CTX01-16543	Coiltronics Central Semi
Q2	CMPT3904	30V		SOT23	CMPT3904-IRR	
Q3	24MHz			CSM_7	XC582CT-ND	Digi-Key
R111,R113,R114,R119	5.1k		5%	603		Digi-Key
R112	10k		5%	603		Digi-Key
R117,R115	0 ohm		5%	603		Digi-Key
R116,R118,R139	0 ohm		5%	603		Digi-Key
R120	6.2 ohm		1%	603		Digi-Key
R121,R122,R123,R124,R125, R126,R127,R128,R131,R133, R134,R135,R136,R137,R138, R140,R141	20k		5%	603		Digi-Key
R129	0 ohm		5%	603		Digi-Key
R130	10ohm		5%	603		Digi-Key
R132	1.0k		5%	603		Digi-Key
S1	SW DIP-10/SM			DIPSW20	CT21910MST	Digikey
S2	SW DIP-8/SM			DIPSW16	CT2198MST	Digi-Key
TP1	+12V			TESTPOINT	V1054	Digi-Key
TP2	+5V			TESTPOINT	V1054	Digi-Key

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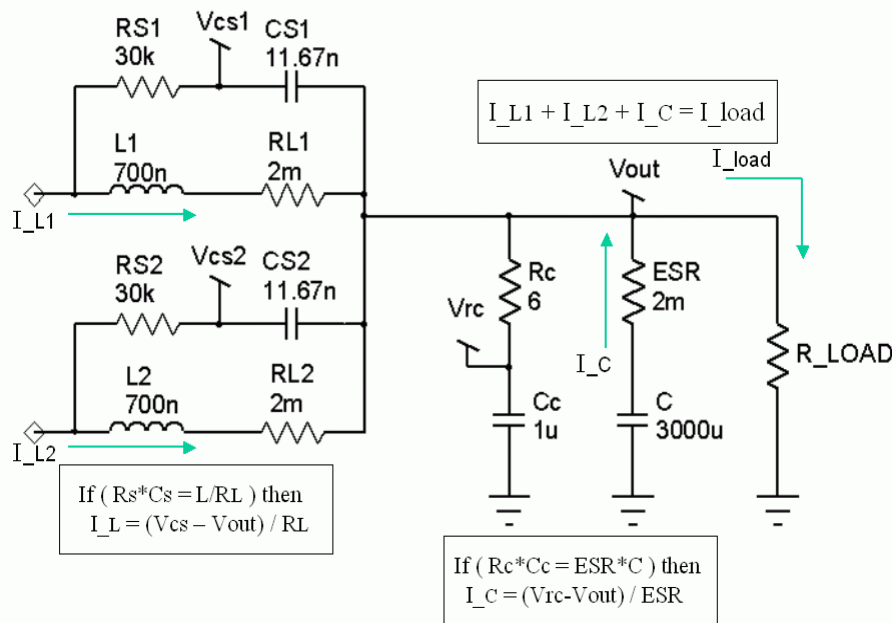
TP3	+3.3V	TESTPOINT	V1054	Digi-Key
TP4	-12V	TESTPOINT	V1054	Digi-Key
TP5	12V_Power	TESTPOINT	V1054	Digi-Key
TP6	VO+	TESTPOINT	V1054	Digi-Key
TP7,TP8,TP9,TP10,TP11, TP12,TP13	GND	TESTPOINT	V1054	Digi-Key
TP14	VR_hot#	TESTPOINT	V1054	Digi-Key
TP15	Load_current	TESTPOINT	V1054	Digi-Key
TP16	VCC_PWRGD	TESTPOINT	V1054	Digi-Key
TP17	VRM_PRES	TESTPOINT	V1054	Digi-Key
TP18	OUT_ENABLE	TESTPOINT	V1054	Digi-Key
TP19	VO_SEN+	TESTPOINT	V1054	Digi-Key
TP20	VO_SENSE	TESTPOINT	V1054	Digi-Key
TP21	VO_SEN-	TESTPOINT	V1054	Digi-Key
U3	AT89C1051	DIP20	AT89C1051	Atmel
U8	VCC	604BGA		
U8	GND	604BGA		
U8	VID/sense	604BGA		

Appendix: Principles of Capacitor Current Compensation Circuit

As illustrated below, the load current is the sum of inductor current and bulk capacitor current. At steady state, inductor current is approximately equal to load current, because the average capacitor current is zero. But during a sudden load change, the capacitor current actually accounts for most of the transient current. Therefore, if only the inductor current is used to control the droop compensation circuit, a large error will occur at the output voltage during transients.



The goal of the Capacitor Current Compensation Circuit is to accurately represent the load current, by summing the (measured) inductor current with the (estimated) capacitor current. A correct droop control signal, based on the load current, can then be used to compensate the output voltage. The basic circuit is outlined by the following diagram:

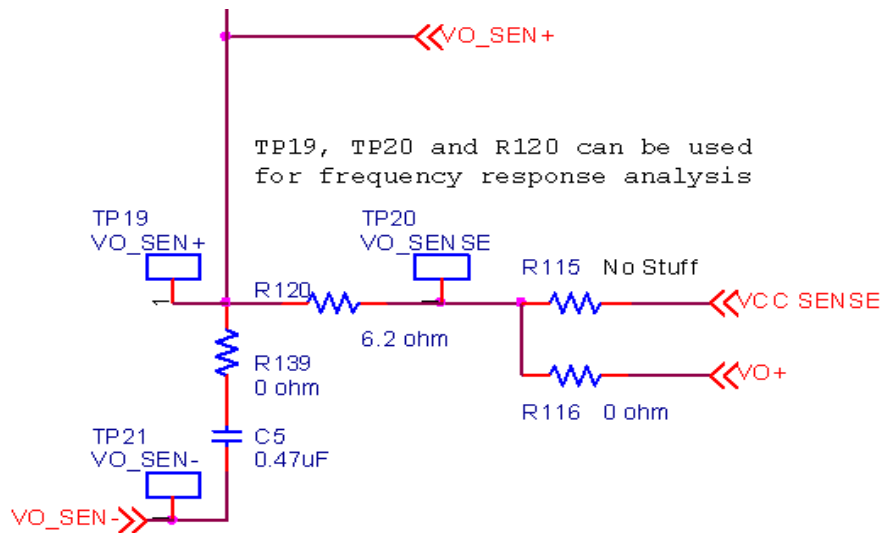


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A simple serial RC network, consisting of discrete components R_c and C_c, is placed in parallel to the main output capacitor. The trick is to make the time constant of the two R-C networks identical, such that the potential drop across the internal ESR is identical to that across the external R_c (since the internal resistance of C_c is negligible compared to R_c). The current flowing out the main output capacitor is now determined by:
 $I_c = (V_{rc} - V_{out}) / ESR$.

The actual load current is the sum of inductor current(s) and capacitor current. An accurate droop control signal can then be generated based on the actual load current.

In another implementation (see below), the capacitor current information is used to offset the error amplifier, so that a correct step response in output voltage can be achieved - even if a perfect droop control signal is not available. This method is particularly important because it means that existing controllers (based on traditional inductor sensing or R_{dson} sensing) can be compensated externally to give highly accurate transient responses in AVP applications.



Capacitor Current Compensation Circuit:
 R120*C5 should be matched with the
 R*C of bulk cap (e.g. 7m * 560uF)
 R139 can be used to disable CCCC

In principle, we need the RC-time constant of R120 and C5 to be the same as the time constant of the bulk output capacitors. For example, if we are using 560uF, 7 milli-ohm Aluminum-poly cap, its time constant is 3.9uS. So R120xC5 should be around 3.9uS.

In practice, due to tolerances in component parameters and various second-order effects, this compensation circuit should be fine-tuned to give the best response.