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**To: Distribution**

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## Reliability Qualification of New Device PVT412A in 6L-PDIP Package

Three qualification lots of PVT412A in 6L-PDIP package completed Autoclave, Temp-Cycling, HTB and THB Reliability Tests without the occurrence of any reliability failure. Based on these reliability test results, the PVT412A in 6L-PDIP Package is qualified and released to production. The level of qualification is industrial level.

The PVT412A is similar to the previously qualified device PVT412. The differences between PVT412 and PVT412A are:

Device	Rdson	Iload	Die Size	PVG Die
PVT412	27 ohms	140 mA	38x54	PVG15A
PVT412A	6 ohms	240 mA	78x88	PVG25A

The test conditions and results are as follows:

### Rel Test #1 - Autoclave Humidity Test

Test Condition: 16 Hours of Autoclave @ +121°C, 100%RH and 15 PSIG.  
Bias Condition: None

Results:

Device	Pkg	Lot Number	Assy	Hour	SS	Reject	EOT Date
PVT412A	6L-PDIP	P112850, Lot 1	Cirtek	16	20	0	04/11/02
PVT412A	6L-PDIP	M289433, Lot 2	Cirtek	16	20	0	05/30/02
PVT412A	6L-PDIP	M289434, Lot 3	Cirtek	16	20	0	05/30/02

### Rel Test #2 - Temperature Cycling

Test Condition: 1000 cycles between -40°C and 125°C ( $\Delta T=165^\circ\text{C}$ , Dry-Air to Dry-Air)  
Bias Condition: None

Results:

Device	Pkg	Lot Number	Assy	Cycle	SS	Reject	EOT Date
PVT412A	6L-PDIP	P112850, Lot 1	Cirtek	1000	20	0	04/30/02
PVT412A	6L-PDIP	M289433, Lot 2	Cirtek	1000	20	0	07/03/02
PVT412A	6L-PDIP	M289434, Lot 3	Cirtek	1000	20	0	07/03/02

### Rel Test #3 - High Temperature Bias (HTB) Test

Test Condition: 1008 Hours @ 110°C  
 Bias Condition:  $V_{in}$  = 6V through 5.1K $\Omega$  resistor, (Reverse Bias)  
 $V_{out}$  = 320V of  $V_{max}$  through 222K $\Omega$  resistor, (Forward Bias)

Results:

Device	Pkg	Lot Number	Assy	Cycle	SS	Reject	EOT Date
PVT412A	6L-PDIP	P112850, Lot 1	Cirtek	1008	20	0	05/22/02
PVT412A	6L-PDIP	M289433, Lot 2	Cirtek	1008	20	0	07/10/02
PVT412A	6L-PDIP	M289434, Lot 3	Cirtek	1008	20	0	07/10/02

### Rel Test #4 - Temperature Humidity Bias (THB) Test

Test Condition: 1008 Hours @ +85°C and 85%RH  
 Bias Condition:  $V_{in}$  = 6V through 5.1K $\Omega$  resistor, (Reverse Bias)  
 $V_{out}$  = 10V through 222K $\Omega$  resistor, (Forward Bias)

Results:

Device	Pkg	Lot Number	Assy	Cycle	SS	Reject	EOT Date
PVT412A	6L-PDIP	P112850, Lot 1	Cirtek	1008	20	0	06/03/02
PVT412A	6L-PDIP	M289433, Lot 2	Cirtek	1008	20	0	07/10/02
PVT412A	6L-PDIP	M289434, Lot 3	Cirtek	1008	20	0	07/10/02