PCB layout guidelines

From the IGBT team at IR
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“Parasitics” (unwanted L, R, C) have much influence on switching waveforms and losses.

The IGBT itself has its own parasitics: some stray inductance in the wire bonds and capacitances in silicon. These are an integral part of the device.

A good PCB layout adds little additional parasitics beyond what is already inside the device.

We will focus on five elements:

1. Inductance in the DC loop
2. Inductance in the AC loop
3. Common emitter inductance
4. Reverse transfer (Miller) capacitance and gate drive impedance
5. Layout requirements for paralleling
1. Inductances in the DC loop

Stray inductances can be in the DC side of the loop or in the AC side. The inductances in the DC side are responsible for the voltage transients on the bus. These transients are proportional to $L_{\text{stray}} \frac{di}{dt}$ and depend, in part, on the control scheme.

The effects of these inductances can be mitigated with a low-ESR capacitor connected as close as possible to the IGBT terminals.
2. Inductances in the AC loop

Residual inductance in the DC loop and stray inductances in the AC loop are the main cause of voltage spikes at turn-off. These inductances charge-up when the IGBT is turned on and discharge at turn-off, causing an overvoltage on the collector.

There are only two ways of mitigating these spikes:

1. Good PCB layout: short tracks and/or paralleled tracks with current flowing in the opposite directions, ground planes, etc.
2. Snubbers and clamps: expensive and lossy.
Typical waveforms of overvoltage at turn-off

- **Low Loop Inductance**
  - Higher Loop inductance causes higher and longer voltage spikes
  - Increases Power Dissipation
  - Increases EMI signature

- **Large Loop Inductance**
Effect of switching speed on the switching transients

Faster switching causes higher and longer voltage spikes. Some IGBTs have softer switching characteristics with lower $\frac{di}{dt}$. They are optimized for medium-frequency switching (1-8kHz).
Effect of AC loop inductance on short circuit waveforms

During a short circuit the stray inductances get charged to a high level of current. They get discharged at turn-off with a voltage spike that may take the IGBT into avalanche.
Stray inductances may cause driver to latch

When the high-side IGBT turns off, current transfers to the low-side diode. Negative volt-seconds are applied to LS2 and LD2 to discharge them, while positive volt-seconds are required to charge LD1 and LS1. This causes the Vs pin of the IC to go below ground.

ICs tend to latch when any pin is brought below ground. Gate driver ICs are built with different levels of noise immunity. Some are more rugged than others.
AC loop inductance can cause the gate driver IC to latch

Low AC loop Inductance

High AC loop Inductance

Exceeding the –Vs spec of the gate driver IC can cause gate driver malfunction (latch up, retriggering, etc)
“Common emitter inductance” is the inductance that is common to the collector current and to the gate drive current. The voltage developed across this inductance during turn-on and turn-off adds/subtracts from gate voltage and slows down di/dt. It increases switching losses but reduces EMI.

It can be eliminated by running separate wires to the emitter pin: one for the emitter, the other for the gate drive return.
4. Miller capacitance and gate drive impedance

Any dv/dt that appears on the collector is coupled to the gate through a capacitive divider $C_{RES} - C_{GE}$

The voltage spike on the gate is determined by:
- The ratio of these two capacitances
- The dv/dt on the collector
- The gate drive impedance

Very low gate drive impedance effectively shorts $C_{GE}$, and prevents a dv/dt induced turn-on, as long as the stray inductance of the gate drive is minimized. Run short and parallel tracks for gate drive and gate drive return. **Do not** rely on the common (power) ground for the gate return.
Waveforms during a dv/dt induced turn-on

The shoot-through current flows after the gate voltage exceeds $V_{\text{TH}}$. The rest is capacitive charging current. Shoot-through currents increase losses and impair equipment reliability.
General PCB Layout Guidelines

- Place the DC bus capacitors as close to the IGBTs as possible to reduce the loop area. Choose bus capacitors with low ESL.
- Distribute the DC bus capacitors close to the half bridges of the three phase inverter so all three half bridges have symmetrical switching paths.
- Add decoupling capacitors across the DC bus at each pole, close to the IGBTs.
- Place the positive and negative planes of the DC bus on top and bottom layers of the PCB. Make the planes overlap as much as possible to reduce the DC loop inductance.
- For inverters using high power modules, use laminated bus bars.
- Reduce the distance between the high side and low side IGBTs to reduce the AC loop inductance and to prevent damage to gate driver ICs.
- Avoid wire wound shunt resistors. They are highly inductive and cause voltage spikes and oscillations.
- Reduce gate drive impedance to prevent $dv/dt$ induced turn-on.
- Use IGBTs with low $di/dt$ transitions when operating at medium frequencies (1-8kHz).
Special considerations when paralleling

When paralleling the stray parameters need to be reduced and equalized

1. Equalize common-source inductances. They impact the di/dt and cause unbalances in switching losses.

2. A 10% unbalance in individual stray inductances in the drain coupled with a 10% unbalance in d/dt translates in an overshoot unbalance of 20%. The impact on switching losses may be acceptable in many applications.
When switching losses are important

A reasonable amount in switching unbalance can be tolerated when switching losses are small compared to conduction losses. In this case a simple in-line arrangement can be satisfactory.

If switching losses are important, stray parameters need to be equalized to avoid unbalances in switching losses and junction temperatures. A circular arrangement may be necessary.
In conclusion

Layout is critical to reliable operation of power circuits
Please, give it the necessary attention!