HIGH EFFICIENCY DC/DC CONVERTER FOR SOLID STATE POWER AMPLIFIER

Kåre Lund, Lass Sølver Pedersen

International Rectifier Denmark
Literbuen 10C DK-2740 Skovlunde, Email: klund1@irf.com

ABSTRACT

On commercial telecommunication satellites using Phased Array Antennas (PAA) up to 70 % of the available payload power is handled by the DC/DC converters supplying the Solid State Power Amplifier (SSPA) for each antenna element.

This paper presents the rationale for selecting the optimum topology with respect to the key parameters efficiency and mass. The choice is furthermore supported by considerations for EMC performance, component availability, physical realization and qualified processes.

The optimum solution found is on an ultra high efficiency main stage based on a full-bridge input switch with patented integrated magnetic and patented Hy-bridge rectification using synchronous rectifiers. The topology offers almost ideal cancellation of the input and output ripples when used on a tightly regulated bus. The solution is also presented in a non-isolated version

Efficiency for a 60 W EPC* is more than 93 % (galvanic isolated) and 94 % (galvanic non- isolated) including two auxiliary outputs.

1. Introduction

The business segment of satellite communication has experienced a prosperous development in the last decades, this is best exemplified by the development for one of the biggest operator in this segment; Inmarsat.

	Satellites In orbit	Mass at launch [kg]	Launched
Inmarsat 2	4	1200	1990-1992
Inmarsat 3	5	2070	1996-1998
Inmarsat 4	2 +1 spare	5950	Q1-Q2 2005

Table 1. The development in the last decade of the Inmarsat satellite fleet.

The growth in mass and satellites in orbit has been driven by an increased need for bandwidth, transmitted signal strength and coverage on ground.

	Phased array antenna elements	Mobile Link *EIRP [dBW]	Bandwidth [kbps]
Inmarsat 2	1	39	0.6
Inmarsat 3	33	48	Up to 64
Inmarsat 4	150	67	432

Table 2. Development in the communication payload for the Inmarsat satellite fleet.

This rapidly increase in “strength” of the communication payload has naturally been accompanied by an increasing need for satellite power.

	Platform power [W]	Payload power [W]
Inmarsat 2	1440	650
Inmarsat 3	2300	1600
Inmarsat 4	12000	9000

Table 3. Development in power demands for the Inmarsat satellite fleet.

For the Inmarsat 4 satellites the EPC for SSPA handles 75% of the payload power and hereby 55 % of the total power available from the platform, making the EPC and the SSPA the single most important payload component for the satellites power budget, and as a natural consequence the efficiency becomes the most important performance parameter for the EPC for SSPA.

The second most important performance parameter is mass, this is driven by the mass penalties seen on space programs, the penalties are reflecting the cost to lift and operate the mass into space. The mass penalty for large GEO communication satellites normally equals 60$/g. For the Inmarsat 4 satellites having 150 EPCs for SSPA this equals a 9000$/g mass penalty for each of the three delivered satellites.

However, as the overall mass of the 150 EPCs equals approximately 40 kg or less than 1 % of the overall mass of the satellite this parameters is not surrounded with the same amount of hysteria from prime contractor as the efficiency. Thus the two key parameters for an EPC for SSPA in a prioritised rank are:

1. Efficiency
2. Mass

EPC = Electronic Power Conditioner. A unit containing more than one DC/DC converter and control electronics for custom specific features. Such as protection, timing and telemetry. *EIRP = Effective Isotropic Radiated Power (signal strength)

Proc. ‘Seventh European Space Power Conference’, Stresa, Italy,
9-13 May 2005 (ESA SP-589, May 2005)

With these key parameters in mind, this paper outlines the design consideration taken by IR Hirel design team in the design of a 60W EPC having below main characteristics:

Parameter	Value	Comment
Input bus voltage	50 V ± 1%	Astrium Eurostar 3000 platform
Output 1, voltage	7.5V-9V (± 2%)	Output is user adjustable
Current	6.7A, 7.5A	Max load Current limit min.
Power	60.3W	Max
Output ripple	<5 mVrms	Frequency domain, including CS
Output 2, voltage	5V (± 2%)	
Current	0.27A	Max
Power	1.35W	Max
Output ripple	<2 mVrms	Frequency domain, including CS
Output 3, voltage	-5V (± 2%)	
Current	0.25A	Max
Power	1.25W	Max
Output ripple	<1 mVrms	Frequency domain, including CS
Protection	Over current protection on all output. Under voltage shutdown on input	
TC	Pulse command	Latching relay
Timing between outputs	YES	-5V to arrive 2 msec before positive outputs at turn ON, vice versa at Turn OFF

2. BLOCK LEVEL DESIGN

It has been chosen to make the EPC as a two converter solution, with a high efficient main output converter and a small and simple Fly-back converter supplying internal auxiliary supply and feeding the linear regulators placed on the low power +/- 5 V outputs.

2.1. Block diagram

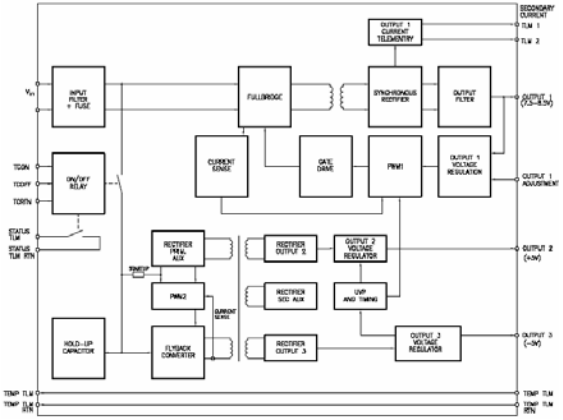

Fig 1 Block diagram

The main output is utilizing a Full-Bridge driving a Hy-Bridge topology, the PWM1 uses peak current mode control with direct voltage sense, also for the fly-back a current mode control scheme is chosen. Current mode control is chosen for simple tuning of the control loops, to eliminate line regulation issues and in combination with the integrated magnetic to eliminate saturation of the transformer, even during abnormal operation.

To maintain high efficiency and at the same time to cross the galvanic isolation barrier a gate transformer is used to control the bridge mosfet's, instead of an active part (eg. IR2110)

For initial start-up a simple dropdown resistor from the bus is charging the drive capacitor for the PWM2. For high efficiency the Fly-back is powered and regulated by use of a bootstrap winding (primary AUX).

Linear regulators for output 2 and 3 ensure well regulated (+/-2 % EOL) low noise output voltages and individual current limitation.

Timing between outputs is always an issue of great concern for EPCs, the SSPA gallium arsenide field effect transistor (GaAsFET) needs a negative voltage to pinch off the channel before the positive main output is applied. Failure to do so results in destruction of the GaAsFETs and loss of the SSPA function.

With full control and hereby fault separation of all voltages, it is possible to make a well controlled timing between all outputs, the hold-up circuit is providing energy for the negative output during power down.

The ON-OFF control scheme is done by use of a latching relay to interface with a standard high level pulse command making it easy adaptable to most platform specifications.

Also the EPC is using a input UVP circuit placed on the secondary side hereby it can be an integral and combined part of the timing circuit ensuring a well defined performance during start-up and shut down.

3. SELECTION OF THE MAIN CONVERTER TOPOLOGY

3.1. Calculation Baseline

Since 96% of the EPC power is handled by the main converter, the efficiency and mass of the EPC is mainly determined by this stage. Therefore, the rationale for selecting the topology for this converter will be detailed in the following. Efficiency and mass will be estimated for the three main parts of the converter, the primary power bridge, the transformer and chokes and finally the rectifier stage. For each part the selected solution as well as the most promising alternative is analysed.

All efficiency calculations are done at:
Vin=50V
Output 1: 8.5V, 6.7A
Output 2: 5V, 200mA (nominal load)
Output 3: -5V, 190mA (nominal load)

The IR Denmark design group has during the last decade developed and refined a design tool for the most common used power topologies the tool is capable to predict the efficiency and the mass of the power stage with great precision, see also figure 8. The tool has been used in this paper to calculate efficiencies for the chosen solution and the alternative solutions for further comparison.

3.2. Choice of Main Power Bridge

The choice of the man bridge stands between a full and half-bridge. A clamped full bridge with ZVS (Zero Voltage Switching) is chosen. A clamped bridge is controlled in such manner that the primary winding is shorted in the off-periods where no voltage is applied to the winding. This preserve the energy stored in the leakage inductance for the transformer for charging the capacitance of the mosfets prior to turn-on (ZVS).

In the chosen bridge the voltage stress do not exceed the supply and the relatively low input voltage makes it possible to use 100V mosfet's and still able to keep a 50% derating for Vds.
Comparing the full bridge with the half bridge results in preference for the full bridge as the half-bridge is not clamped resulting not only in voltage spikes but low load situations will be associated with a numerous problems due to its limited ability to lead the current back to the bus. This means that designers often will have to change the sync rectifiers to 100V types. Also to control the spikes (EMC) it will be needed to use a snubber. Therefore the choice stands between higher efficiency versus higher mass (if any).

A die size 3 IRHF57130 is used and is a good trade-off between conductive losses and switch losses for the actual power level. The higher currents in the Half-Bridge would logically call for larger die size but no other component was found to give a better result.

3.3. Efficiency and Mass

The best efficiency is found at 110kHz, the efficiency benefits is found to be negligible at lower frequencies and the magnetic parts mass will grow to unacceptable levels.

The efficiency results using the above designs are:

	Full-Bridge		Half-Bridge	
Magnetic	0.758W	1.27%	0.699W	1.16%
Bridge	0.714W	1.20%	1.116W	1.86%
Rectifiers	1.042W	1.75%	1.044W	1.74%
Ploss tot.	2.62W	4.4%	3.163W	5.26%
Total η		95.6%		94.74%

Results are only for the main stage, the same component types are used for both setups:

The slightly lower losses of the Half-Bridge magnetic are due to zero transformer current in the off period.

The mass penalty for using a Full-Bridge is found to be 5g compared to a Half-Bridge solution. As the efficiency is the key parameter for the EPC, the Full-Bridge is chosen.

3.4. EMC

The full bridge produces clean and almost spike free voltage and current waveforms. For regulated busses and constant output voltage it can get close to 100% duty cycle and thereby constant current draw leading to a need for a very limited input filter.

4. CHOICE OF MAGNETIC LAYOUT

4.1. IM (Integrated Magnetic)

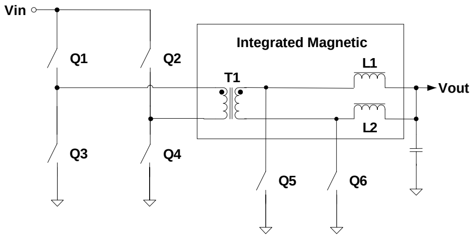

Fig. 2. Main stage

The main transformer and the output chokes of the converter are based upon an integrated magnetic structure in order to optimize efficiency, mass and volume. That means T1, L1 and L2 uses the same magnetic core and is realized as one integrated magnetic component. Combining the transformer and the output chokes on the same core presents several advantages:

- Optimum utilization of the ferrite core
- Free magnetizing current in the transformer (see also section 6.)
- No saturation of the transformer (during turn-On and turn-Off)
- Low stray magnetic field
- Lower losses for same mass

4.2. Efficiency and Mass

The IM (integrated magnetic) has not only given electrical improvement but also maximise the utilization of the magnetic material.

For mass comparison a calculation setup for a traditional Hy-bridge converter build with discrete components and the same surrounding components has been made. EFD cores are found to be the best alternative and have been scaled to give the converter the same efficiency as for the IM baseline.

The efficiency results using the above philosophies are:

	IM		Discrete magnetic	
Magnetic	0.758W	1.27%	0.822W	1.38%
Bridge	0.714W	1.20%	0.714W	1.20%
Rectifiers	1.042W	1.75%	1.042W	1.75%
Ploss tot.	2.62W	4.4%	2.683W	4.5%
Total η		95.6%		95.5%

The mass of the IM is 37.5g and the discrete magnetic mass is found to be approximately 57.8g. With a mass penalty of more than 20g and no efficiency benefits the IM solution is chosen even it is more complicated to manufacture and test.

5. CHOICE OF MAIN OUTPUT RECTIFIER

5.1. The Hy-Bridge.

The choice to use a Hy bridge is due to its efficiency performance and the fact that the Integrated magnetic can be utilized on this topology with the associated advantages.

The Hy-bridge rectifier operates at optimum with a clamped input bridge and is then combining all good parameters from other topologies. During the off period the rectifiers “share” the output current, the currents will differ with the current in the leakage inductance of the transformer. With synchronous rectifiers the Hy-bridge also has the ability to transfer current back to the line.

5.2. Efficiency and Mass

The output rectification could be made with either synchronous rectifiers or diodes. To make this choice efficiency and mass calculation has been made for both methods.

When selecting a Mosfet as synchronous rectifier, switch timing is of outmost importance for an efficient converter, this means that the best efficiency is not found with the part with lowest Rdson but with part that in a combination with a good Rdson is “light” to drive. The best combination is for this 60W EPC, is found using the IRF7YSZ44VCM a size 4 die. An amobead (magnetic snubber) is used to prevent the switch transition to strike a resonance between the stray inductance and the mosfet’s output capacitance. By preventing the resonance, other snubbers than the amobead on the secondary side is not necessary. It cost approximately 100mW close to 0.2% efficiency to insert the amobead.

For the diodes the best choice is 1N6815 a 40 V 25A in a ThinKey-2 package.

The efficiency results using the above philosophies are:

	Mosfet		Diode(1N6815)	
Magnetic	0.758W	1.27%	0.77W	1.26%
Bridge	0.714W	1.20%	0.715W	1.17%
Rectifiers	1.042W	1.75%	2.808W	4.58%
Ploss tot.	2.62W	4.4%	4.293W	7.0%
Total η		95.6%		93.0%

As the efficiency is the key parameter for the EPC, synchronous rectification is chosen even though it has a mass penalty estimated to 9g.

5.3. EMC

The Hy-Bridge provide double frequency and for regulated busses and constant output voltage it can get close to 100% duty cycle and thereby will the output current get close to cancellation and become a DC current leaving the need for a very limited output filter. The size/mass of the output filter is often set by other parameters like load step and loop performance immunity to various load impedances.

6. Synergy of the Main Stage

The choice to combine the clamped full-bridge with the synchronous rectified Hy-bridge on an integrated magnetic is not three randomly independent choices

The clamped bridge shorts the primary winding and by that preserves the energy for ZVS, but the same energy/current will on secondary side keep most of the output current in the rectifier that is about to be turned off, this means that there still are “positive” current in the Amobead/Rectifier for smaller output currents than if the bridge had been unclamped and the rectifiers had shared the output current equally.
As a result the amobead works down to 3% of the maximum output current in clamped bridge configuration where for the non clamped bridge the current in the amobead will go negative when the converter goes into light-mode (the current continues negative) at 30% of the maximum output current.

The integrated magnetic can contain the transformer winding and both of the output inductors at the same time. Consider the two output inductors each mounted on a leg of an E-core if phased correctly they will share the same DC flux and force the AC flux to flow in the third leg, this AC flux will be equal to the AC flux in the transformer hence the transformer can have a free ride on the third (middle) leg of the E-core.

7. Bread board Results

The described converter has been build and tested, the test results presented in this chapter is for the complete converter. As shown in figure 1

The EPC seen from the top, on the PCB there is made room for some extra output filtering,

Fig. 3. The Electronic Power Conditioner

7.1. The bridge voltage and current stress

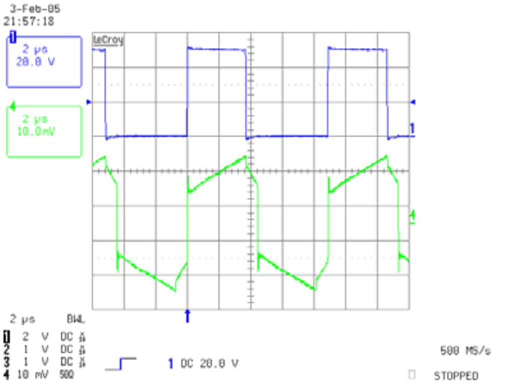

Fig. 4. Main bridge voltage and primary winding current 1A/div

Figure 4 shows the voltage in one branch of the main bridge and the current into the primary transformer winding, as it can be seen the voltage and current waveforms is without spikes and with a minimum of component stress.

7.2. The rectifiers voltage and current stress

Getting close to a duty cycle of 50% the output current ripple of the two output inductors almost cancel out one another.

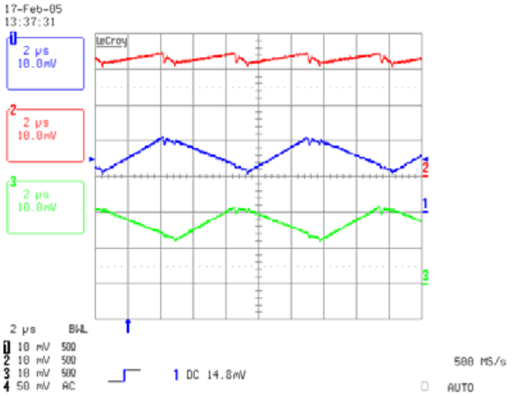

Fig. 5 Inductor Currents 2A/div Vout=8.5V Iout=6.7A

Figure 5 shows the currents of each output inductor. 8.5V equals approximately a duty factor of 0.42 and the AC corposants are almost the reverse of one another and will add up to become close to a pure DC current (the top curve)

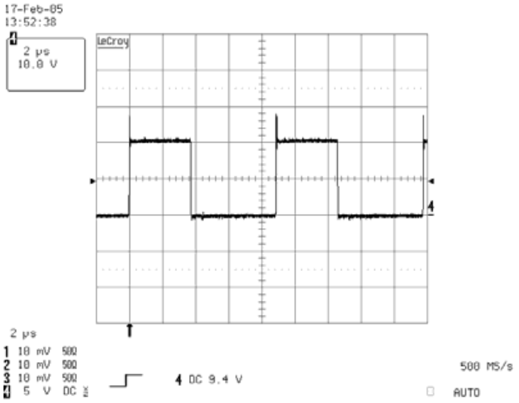

Fig. 6. Drain voltage of one rectifier

Figure 6 shows the drain voltage of one synchronous rectifier. Only a limited high frequency spike is present.

7.3. Loop performance.

The ability to feed current back to the bus when using synchronous rectifiers also has the advantage that the converter does not enter into light mode as a diode rectified converter would do; when turned on, the current will not go to zero but continue negative. The loop is therefore not influenced and do not become highly load dependable as normal converters do when entering light mode

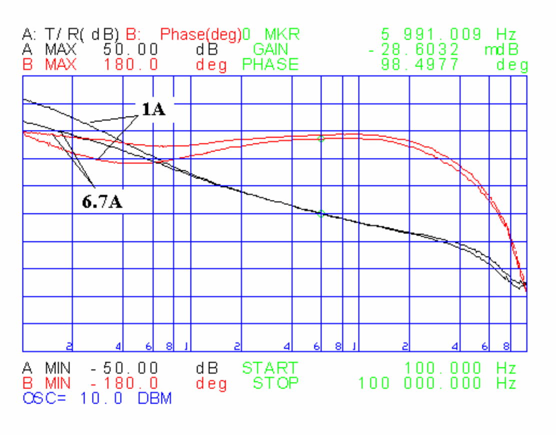

Fig. 7. Loop performance for full load and 1A.
GM = >19dB PM = >95°

The loop performance at 1A, which is deep into normal light mode, is almost the same as for maximum load.

7.4. Efficiency

The measured efficiency is close to the predicted performance at full load. When the output current is decreased the performance is lower than predicted due to the stray inductance do not store sufficient energy for ZVS for lower currents, moreover is the timing trimmed for maximum performance at maximum load. The calculation tool presumes ZVS and perfect timing.

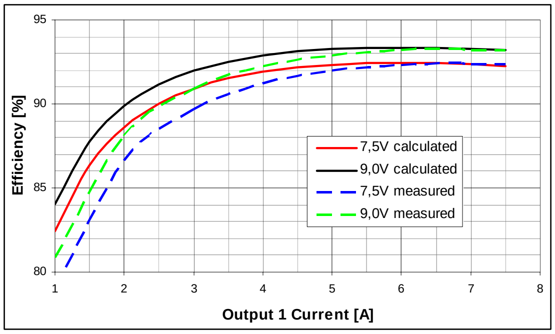

Fig. 8. Efficiency calculated and measured @ 25°C for the full EPC.

8. Pushing efficiency even further.

With the rapidly growth in the need for satellite communication bandwidth and hence power, the customers will in future programs be asking for better and better efficiencies, improving an efficiency of 93% is not an easy task and would require new and innovative solutions. One possible path to follow is described in the following section. This path will require a close interaction between the satellite platform developers and the EPC design groups in development of future design solutions.

8.1. Galvanic isolation

Almost all satellite platforms demands galvanic isolation. When galvanic isolation is chosen some issues will be difficult to deal with. For example the current sense needs to cross the isolation barrier and a current transformer is necessary instead of a simple sense resistor, many other issues also have to be dealt with.

The presented topology using a full-bridge converter with a Hy-bridge rectifier could also be realised as a non-galvanic solution using an Auto transformer solution still based on an integrated magnetic.

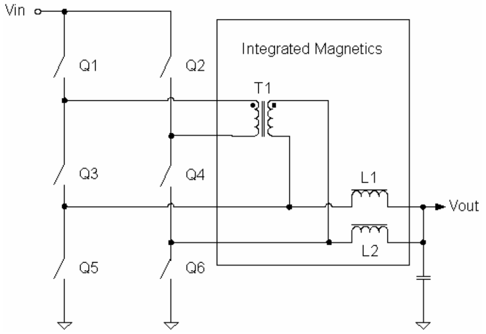

Fig. 9. Non-isolated Hy-bridge configuration.

Calculations of efficiency for a galvanic isolated solution versus none galvanic isolated solution shows.

	Isolated		None Isolated	
Magnetic	0.758W	1.27%	0.488W	0.83%
Bridge	0.714W	1.20%	0.679W	1.15%
Rectifiers	1.042W	1.75%	0.680W	1.15%
Ploss tot.	2.62W	4.4%	1.949W	3.3%
Total η		95.6%		96.7%

Hereby the overall EPC efficiency can be improved from 93% to 94 % or a 15% lowering of the power loss is a substantial improvement! Besides the efficiency improvement, the converter would be simpler, lighter, smaller and cheaper, the development time would be less and the EMC performance could be improved.
Not to consider if there is a really need for galvanic isolation would be a disservice to the performance of the design.

9. Conclusion.

The design rationale behind a 60W EPC fitting a Eurostar 3000 platform has been presented.

The chosen solution fits the power range and fulfils the prioritized parameters to the maximum extend possible. The efficiency has been the main priority throughout the design of the main stage without unacceptably compromising the mass.

An elegant bread board (EBB) has been built to verify the setup and calculations. The EBB is been built from Hi-Rel representative component and layout restrictions to get a verification baseline representative for future flight hardware.

The EBB has been tested towards the specification and the test results has strengthen the calculation baseline and proven the quality in the presented design with a state of the art efficiency performance (>93%) with a total mass less then 185g (shields and housing not included).

If the primes would be willing to enter a discussion regarding for the requirement for galvanic isolation, the efficiency figure for a non-galvanic EPC could be boosted to 94% equal to 15% lower losses.

10. References.

1. US Patent no. 5,335,163, EU Patent no. 0 5557 378.

2. US Patent no. 4,899,271.

3. Peng C., Hannigan M. and Seiersen O., A New Efficient High Frequency Rectifier Circuit, HFPC, June 1991 Proceedings.