

EPC (electronic power conditioner), Low Voltage DC-DC Converter for SSPA (solid state power amplifier) On-Board Military Satellite Poses the Ultimate Challenge in Product Development and Manufacturing

by

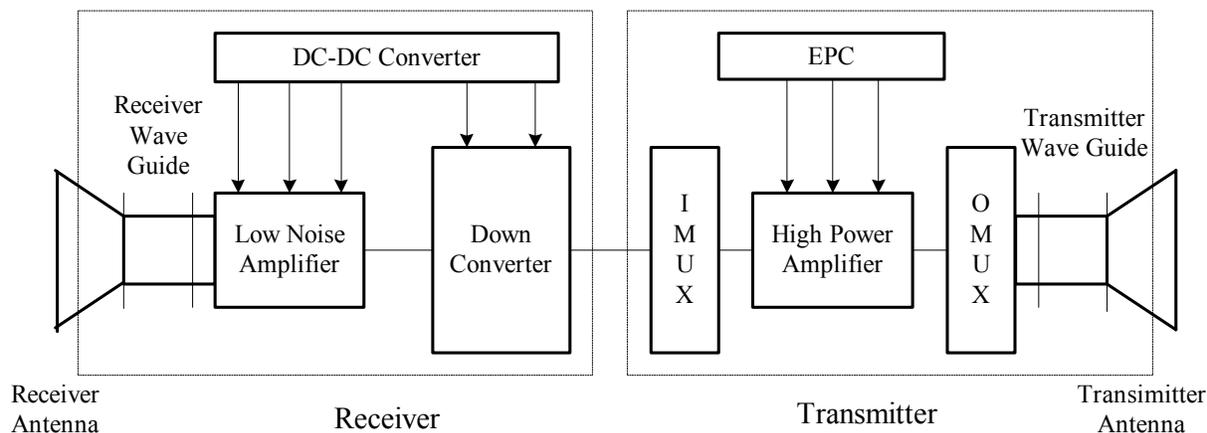
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EPC's for today's military space applications require design solutions and manufacturing processes that provide a reliable product with the highest of confidence. The solution must include radiation-qualified components, proven design heritage and design innovations. Use of hybrid assembly technology is essential in reducing size, weight and cost. Design analyses and computer simulations with actual performance to match are expected. Written procedures for design verification, acceptance tests and manufacturing processes are program standards. All manufacturing processes must be documented and qualified prior to implementation.

Introduction:

In satellite communications, the transponders are the heart of the communication system. They receive, process, amplify, and transmit the received signal back to earth or to another satellite. Refer to Figure 1. SSPA (Solid State Power Amplifier) and TWTA (Traveling Wave Tube Amplifier) in the high power amplifier unit perform the important amplification function. The selection of an SSPA or TWTA for an application is based on several factors. The dominant factors are the downlink carrier frequency and the transmitter power requirements. The TWTA is normally selected over the SSPA for higher power and higher frequency applications. The TWTA is capable of up to about 200W and efficiency can be as high as 60-65%. The SSPA finds its use in the lower frequency bands and lower transmitter power applications. The latest SSPA's are capable of up to 90 watts. While an SSPA is less efficient than a TWTA, in the range of 25-30%, it offers size and mass advantages over a comparable TWTA.

Figure 1. A Very Simplified RF Transponder



Electronic Power Conditioner (EPC) is a generic name for a multiple output DC-DC converter that provides the power to a TWTA or an SSPA from a satellite power bus. The power required by both types of amplifiers is well regulated and normally is from more than one voltage source. The voltage requirements for a TWTA are usually a combination of low and high voltage in the order of a few hundred volts for anode and grid voltage, and in the order of kilo-volts for cathode and collector depending on the type of the TWTA. An SSPA requires a much lower voltage, in the order of 5 to 10VDC for GaAs FET type. The power requirement for an SSPA or a TWTA from an EPC is dictated by the transmitter power requirement and the efficiency of an SSPA/TWTA. For this article, EPC refers to the low voltage DC-DC converter for an SSPA.

Acronyms

| Abbreviation | Meaning |
|--------------|---------------------------------|
| A | Ampere, electrical current |
| BB | Breadboard |
| BOL | Beginning of life |
| C | Centigrade |
| CDR | Critical Design Review |
| CE | Conducted Emission |
| CS | Conducted Susceptibility |
| DC | Direct Current |
| EM | Engineering Model |
| EMC | Electromagnetic Compliance |
| EMI | Electromagnetic Interference |
| EOL | End of Life |
| EPC | Electronic Power Conditioner |
| EQM | Engineering Qualification Model |
| FET | Field Effect Transistor |
| FWHM | Full-Width-Half-Maximum |

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|------|--------------------------------------|
| GaAs | Gallium Arsenide |
| IC | Integrated Circuit |
| HPA | High Power Amplifier |
| MRR | Manufacturing Readiness Review |
| QCI | Quality Conformance Inspection |
| PBA | Power Board Assembly |
| PDR | Preliminary Design Review |
| PWA | Printed Wiring Assembly |
| PWB | Printed Wiring Board |
| RE | Radiated Emission |
| RH | Relative Humidity |
| RLAT | Radiation Lot Acceptance Test |
| RS | Radiated Susceptibility |
| SEB | Single Event Burnout |
| SEE | Single Event Effect |
| SEGR | Single Event Gate Rupture |
| SEL | Single Event Latch-up |
| SEU | Single Event Upset |
| SMT | Surface-Mount Technology |
| SSPA | Solid State Power Amplifier |
| TCE | Temperature Coefficient of Expansion |
| TID | Total Ionizing Dose |
| TWTA | Traveling Wave Tube Amplifier |
| V | Volt, electrical voltage |
| W | Watt, electrical power |

EPC Requirements

Most EPC's for military programs are custom designed to meet specific performance and mechanical configuration requirements. Key requirements are functional performance, cost, size, efficiency, and reliability. Other equally critical requirements are workmanship, parts/material selection and qualification, process qualification and control, configuration management, and radiation hardness assurance. Design reviews, PDR, CDR and MRR are typically required by contract. Other design reviews take place as needed. Deliverable design analyses often include electrical stress and de-rating, worst case, vibration, mechanical shock, mass, reliability prediction, thermal, failure mode effect, radiation, and EMI/EMC.

Performance of an EPC in the radiation environments is dependent on the operational orbit and the mission it serves. For military missions, the radiation requirements are more encompassing than commercial applications though most of the other requirements are similar. The major differences are the requirements for nuclear survivability and tolerance to neutron environments. Table 1 is a partial listing of the key design requirements. For most military programs, the customer requires the contractor to follow their specific in-house design rules, guidelines, hardening and mitigation techniques, components selection, and document/report format, etc.

Table 1. Typical Design Requirements

| Parameter | Typical Requirement |
|-------------------------|---|
| Electrical | |
| Input Voltage | 28V, 50V typical, regulated |
| Input Inrush Current | Required to be compatible with system failure protection scheme |
| Output | Triple outputs for GaAs FET amplifier with output sequencing |
| Output 1 (main) | 5 to 10V, 80-90% of total output power |
| Output 2 | 5 to 15V, 10-15% of total output power |
| Output 3 | -5V, .1 to .5A, a priority output in turn-on and turn-off sequencing |
| Output Regulation | 1% BOL, 3% EOL |
| Total Power | 25W to 250W |
| Output Isolation | Normally required, platform dependent |
| Output Ripple | Out 1: 20-50 mVp-p, 100 MHz BW or 10-15 mVrms in time domain Out 2/3: 5-10 mVp-p, 100 MHz BW or 1-2 mVrms in time domain |
| Efficiency | 88% minimum, most require >90% |
| EMI | CS, CE, RS, RE per MIL-STD-461D/E or unique requirements in accordance with customer specific power bus |
| Over-voltage Protection | Not normally required |
| BusTelemetry | 0-5V, 0-150% load |
| Output Telemetry | Bi-level signal, logic '1' for normal, and logic '0' for abnormal output |
| Temperature Telemetry | 0-5V, full temp range |
| Remote Sense | Required for main output |
| Synchronization | Yes |
| UVLO | Yes |
| On/Off Command | Yes, bi-level or pulse command |
| Output Voltage Adjust | Required for main output with an external analog signal |

| Parameter | Typical Requirement |
|-------------------------------|--|
| Output Sequencing on | Output 3 (-5V output) is designated as the priority output. It is required to turn on and rises (rise time TBD) to within a regulation band of its nominal voltage in no less than 1-50mS before all other outputs reaches 90-95% of their nominal voltage levels. |
| Output Sequencing off | -5V output remains on (within 5-10% of nominal output voltage) for no less than 1- 50mS until all other outputs decay to 10-20% of their nominal voltage levels. |
| Single Point Free Failure | Normally required |
| De-rating | NASA PPL-21/ MIL-STD-1547. Normally dictated by customer design guidelines |
| EOL Aging and Radiation | MIL-STD-975 or per customer design requirements |
| Design Life | 7 to 18 years |
| Mechanical/Environment | |
| Operating Temp | Qualification: -34 to +80°C, program dependent. Design qualification often has a wider temperature range than acceptance requirement of flight hardware. The typical acceptance temperature is -25 to +71°C |
| Storage Temp | -40 to +85C |
| Random Vibration | Dependent of launch platform |
| Pyrotechnic Shock | Dependent of launch platform |
| Acceleration | Dependent of launch platform |
| Humidity | 60-95% RH |
| Explosive Atmosphere | EPC shall not cause ignition |
| Size | Key design requirement |
| Mass | Key design requirement |
| Qualification | Elaborate, program dependent |
| Package Construction | Based on mechanical design, usually is mounted directly to an SSPA as an integral part of the HPA |
| Radiation | |
| Total Dose (TID) | 40 to 100Krad |
| Single Event Effect (SEE) | 40 - 83 MeV, shall not sustain permanent damage from cosmic ray or performance degradation from SEE: no SEU, no SEB, no SEGR, no SEL, no SET |

| Parameter | Typical Requirement |
|--------------------------------------|--|
| Neutron | EPC shall be designed to withstand without permanent performance degradation after exposure to neutron equivalent influence of $\leq 5 \times 10^{12}$ n/cm ² |
| Dose Rate Upset/Recovery | $\leq 10^{11}$ rad(si)/sec, FWHM of 18-100 nS, recover autonomously |
| Dose Rate Survival | EPC shall not sustain permanent damage or permanent performance degradation after exposure to dose rate of $\leq 10^{11}$ rad (si)/sec, FWHM (full-width-half-maximum) of 18-100 nS. |
| Dose Rate Operate Thru | -5V must operate thru after exposure to $\leq 10^{11}$ rad(si)/sec. |
| Electromagnetic Pulse (EMP) | No burnout. |
| System-Generated EMP (SGEMP) Burnout | No burnout. |

Electrical Design Considerations

The basic radiation requirements for an EPC for military space applications are listed in Table 1. Choosing a design topology for the EPC is critical to the success of the design. While efficiency is one of the key performance requirements, the ability of the EPC to meet the design life and to survive and operate through the radiation environments and nuclear events without any performance degradation is equally important. Selection of circuit topology that is appropriate for the required output power and is inherently immune to the radiation dose, SEE and nuclear events is one of the major design considerations.

There are several viable solutions. A full-bridge power stage has been used successfully for output power in the range of 100W or more. The forward converter is optimal for output power of up to 100W. A flyback topology offers size advantage for lower output power that is less than 50W. A forward converter with resonant reset has been used successfully in numerous designs for output power of up to 120 watts with operating temperatures of up to +125°C. For higher output requirements, two similar power stages may be interleaved, each operating 180% out of phase with up to 45% duty cycle to provide twice the power. This design configuration provides power coverage for most EPC requirements for the typical SSPA applications. Both the forward and flyback converters are the topology of choice particularly for prompt dose (dose rate) environments. The series inductor with finite impedance limits the flow of current during the nuclear event and therefore prevents a potential burnout of the power-switching elements due to photocurrent. With proper selection of active devices the same topologies are also suitable for TID, SEE and neutron environments. Similar design considerations must also be given to all

circuitries that are potentially vulnerable to such environments. For circuitries without a series inductor, resistors may be strategically deployed to limit a current flow. Table 2 lists typical mitigation techniques for the radiation requirements.

Table 2. Typical Radiation Hardening Techniques

| Parameter | Typical Mitigation Technique |
|--------------------------------------|--|
| Total Dose (TID) | Parts selection, shielding |
| Single Event Effect (SEE) | Parts selection, power MOSFET's and PWM chip require particular attention. |
| Neutron | Part selection, shielding |
| Dose Rate Upset/Recovery | Circuit design and parts selection |
| Dose Rate Survival | Circuit design and parts selection |
| Dose Rate Operate Thru | Circuit design and parts selection |
| Electromagnetic Pulse (EMP) | Use conformal coating (low atomic number) |
| System-Generated EMP (SGEMP) Burnout | Use suppression diode on sensitive I/O lines. |

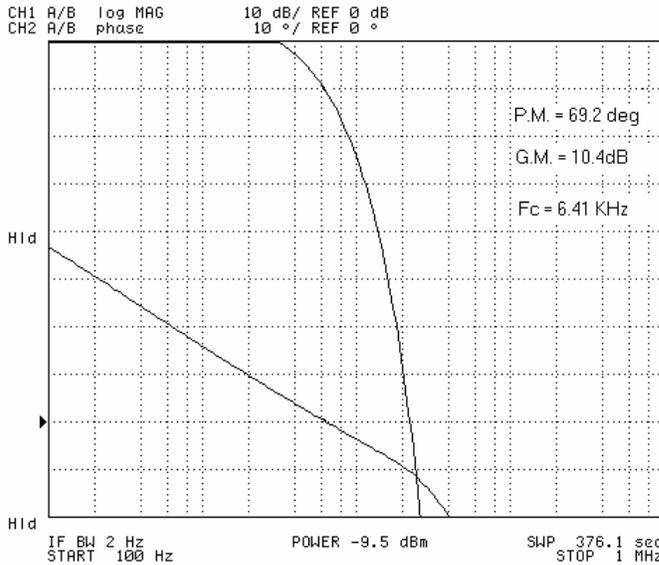
For SSPA applications that use GaAs FET as the amplification element, the -5V output of an EPC is the most critical. Its regulated output must be available at all times while the SSPA is energized, otherwise failure of the device is expected. A separate regulator is normally deployed for each of the outputs to facilitate the output sequencing design.

Use of well-characterized circuitries and discrete devices that have excellent track record in reliability and radiation performance is the most desirable design methodology. Design of control circuitries such as oscillators, PWM controllers, feedback amplifiers, and telemetry and monitoring circuits should be limited to the use of individual discrete devices that are radiation qualified or specifically characterized for the intended design applications. If the use of integrated circuits is necessary, the selection should be limited to operational amplifiers, comparators, MOS gate drivers, logic gates, or only semiconductor devices with known performance characteristics under the required radiation environment. If certain devices fall short and/or design margins inadequate, spot shielding may be deployed. New semiconductor technology should be avoided unless the technology is inherently immune to radiation. RLAT is normally required if reliable data is not available. This design philosophy mitigates design risk and minimizes surprises. Most customers do make their library of components parts available for

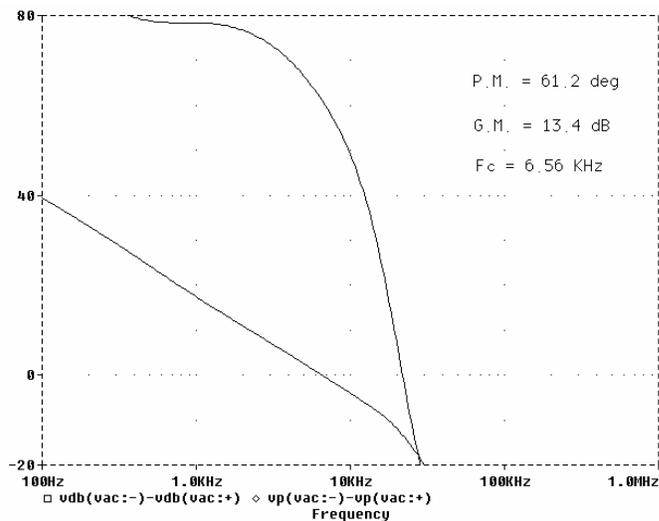
the design selection. Selected components that are not included on the customer's qualified parts list are normally subjected to close scrutiny and approval is required.

Computer simulation of circuit designs has proven to be a tremendous design tool in performance prediction. It assists in design organization and facilitates design optimization. Figure 2 illustrates a computer simulated result and an actual circuit performance.

Figure 2. Measured vs. Simulated Loop Response of an Output of a Converter



Measured Loop Response with Resistive Load, 42.5V input, 8V @ 6.5A Output



Simulated Loop Response with Resistive Load, 42.5V input, 8V @ 6.5A Output

Parts Stress, Component De-Rating and Thermal Analysis

A parts stress analysis is performed for each component in the EPC to verify that no components are exposed to excessive stress levels. Power dissipation of individual components is calculated. In conjunction with the thermal impedance, based on the component location in the assembly, a worst-case junction temperature of individual components is determined. The components junction temperature is then calculated to determine compliance to the design requirement. The parts stress of each component is also compared to the de-rating limits to verify that the de-rating requirements are also met.

Radiation, Reliability Prediction, End of Life (EOL), and Worst-Case Analyses

As with all space programs, radiation, reliability and worst-case analyses are normally required by contract. Established prediction tools are very helpful to insure completeness of the analysis and to enhance the analysis effort. In all cases, a list of individual components must be accounted for. In the case of radiation performance, the RLAT data or hardness level is listed and compared against the design requirements. Refer to Table 2 for sample radiation analysis. For reliability analysis, electrical stress of individual components, power dissipation, thermal impedance, calculated temperature rise of semiconductor junction temperature, and calculated FIT (failure in time) are included.

Table 2. Sample Radiation Analysis

| Part number | Dose Rate Rads(Si)/s | | SEE MeV/(mg/cm ²) | | TID Rads(Si) | | Neutron n/cm ² | | Result |
|-------------|-------------------------|----------|----------------------------------|--------|-----------------|----------|------------------------------|----------|--------|
| | Rated | Reqmnt | Rated | Reqmnt | Rated | Reqmnt | Rated | Reqmnt | |
| 1N4148 | 1.00E+12 | 1.00E+11 | 120 | 40 | 1.00E+06 | 4.00E+04 | 7.00E+13 | 5.00E+12 | Pass |
| 1N752A | 1.00E+12 | 1.00E+11 | 120 | 40 | 1.00E+06 | 4.00E+04 | 7.00E+13 | 5.00E+12 | Pass |
| SC180S060S | 1.00E+12 | 1.00E+11 | 82 | 40 | 5.00E+05 | 4.00E+04 | 5.00E+13 | 5.00E+12 | Pass |
| 2N2222A | 1.00E+12 | 1.00E+11 | 120 | 40 | 5.00E+05 | 4.00E+04 | 7.00E+13 | 5.00E+12 | Pass |
| 2N2907A | 1.00E+12 | 1.00E+11 | 120 | 40 | 5.00E+05 | 4.00E+04 | 7.00E+13 | 5.00E+12 | Pass |
| MPS650 | 1.00E+12 | 1.00E+11 | 82 | 40 | 3.00E+05 | 4.00E+04 | 5.00E+13 | 5.00E+12 | Pass |
| IRHC57260SE | 1.00E+12 | 1.00E+11 | 82 | 40 | 1.00E+05 | 4.00E+04 | 4.00E+13 | 5.00E+12 | Pass |

As for the worst-case analysis (WCA), performance formula including absolute tolerances for initial setting, temperature coefficients, EOL (end of life) drift data, and radiation degradation

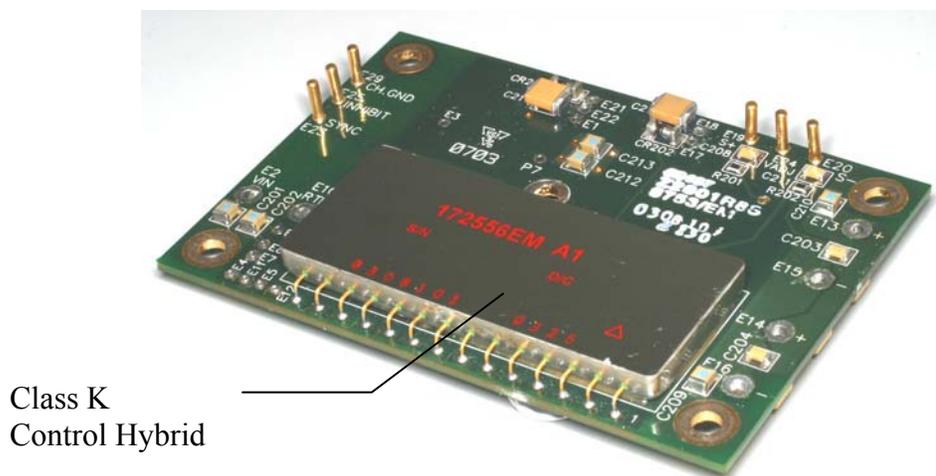
data is established for each of the performance functions. The worst-case performance is then calculated for the temperature extremes to determine compliance to the design requirements.

Packaging and Mechanical Design

Mass budget for a given mechanical design is normally performed early on in the conceptual design phase. Selection of package style for components and materials, i.e., PWB, brackets, standoff, housing, etc. has direct impact on the overall mass, size and cost of the EPC. Design tradeoffs must be made to insure that design (electrical and mechanical) requirements and the cost budget are met. Serious considerations must be given to the sequence of assembly, assembly fixtures/tooling, subassembly tests, and ease of overall assembly and manufacturing processes.

For the last decade, selection of hermetically sealed discrete semiconductors and IC's, has become very limited. The situation deteriorated in the recent years as the low market demand forced the very few remaining vendors to exit the industry. Cost of component screening and QCI processing of the active devices to the quality levels required by the customers, class S for integrated circuits and level S for semiconductors, has been prohibitive. To alleviate the high cost issues, hybridization by packaging a large number of components (approximately 20 to 80 or more in a package) has gained popularity. In addition to reducing component cost, mass and size, hybridization offers improved electrical performance in many design applications. It minimizes parasitic effects and enhances radiation dose hardness. It also offers inherent shielding against electrostatic discharge and EMP. The hybrid-SMT assembly design approach was implemented in some recent designs to reduce cost, size and mass with excellent results. A sample of this design approach is show in Figure 3.

Figure 3. Assembly design using hybrid to reduce cost, size and mass



A sample of a packaging concept is shown in Figure 4. Components of control circuitries and components dissipating very low power (less than 1W) are populated on the top PWA. The PWB

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is a multi-layer copper core board. The thermal paths providing cooling for the components on the board begin with copper vias. Heat transfers from the components through the vias, the inner copper layers, the aluminum standoffs, and down to the base of the housing. All higher power-dissipating devices (greater than 1W) are mounted on the bottom power board. The board material is low TCE aluminum alloy, which provides a low thermal impedance path to the base of the housing to which the power board is bonded. Figure 5 illustrates the PWA and PBA in the EPC housing.

Figure 4. PWA and Power Board Assembly

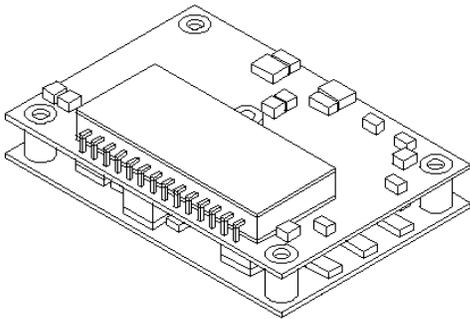
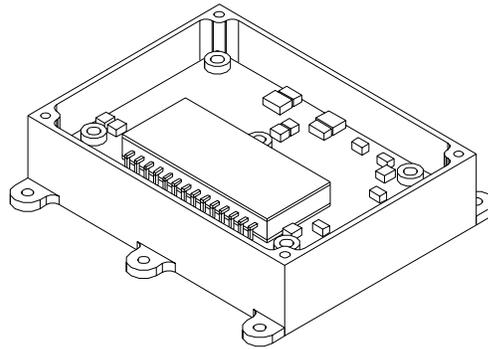


Figure 5. PWA and PBA in EPC Housing



Refer to Figure 6. The package outline for an EPC usually takes the form of a flat rectangular shape with cooling accomplished through the base of the housing. The input/output interface connectors are normally located on the bottom of the case as shown in Figure 7 to provide a direct electrical connection to the SSPA as it is mounted directly on top (cover) of an SSPA housing for heat transfer.

Figure 6. External View of an EPC

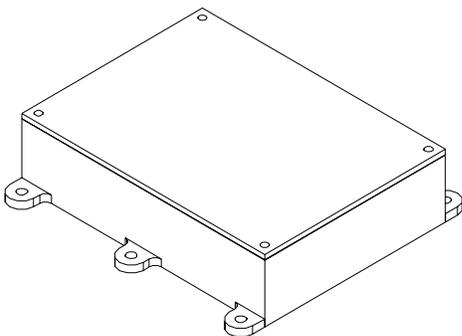
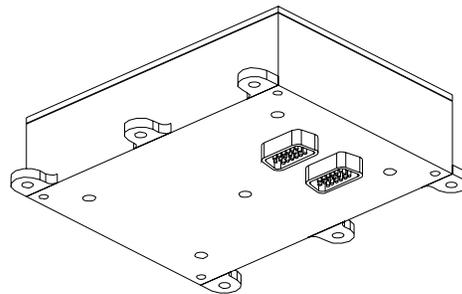


Figure 7. Bottom View of an EPC with I/O Connectors



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Once size and mass are determined to be within the design constraints, a more refined mechanical model is established for the EPC to determine the thermal path and adequate cooling for power dissipating components. Structural analysis of the mechanical model using finite element method is carried out for this effort. Thermal and structural analyses are performed to establish performance baseline, design margin and confidence in the mechanical configuration prior to finalization. Figures 8, 9 and 10 are samples of thermal and structural analyses.

Figure 8. Samples of Thermal Analysis

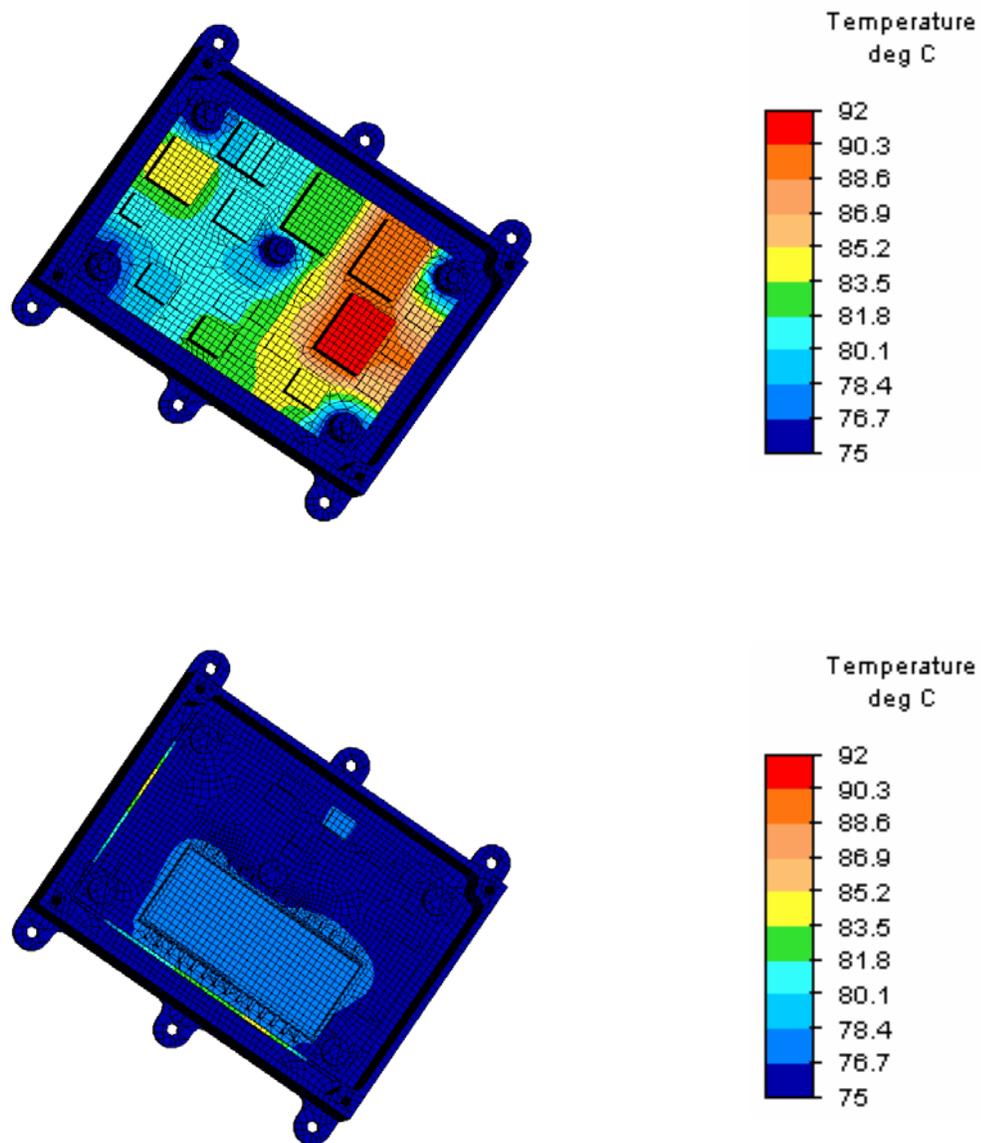
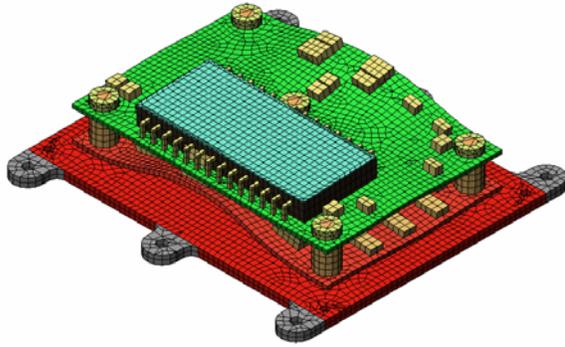
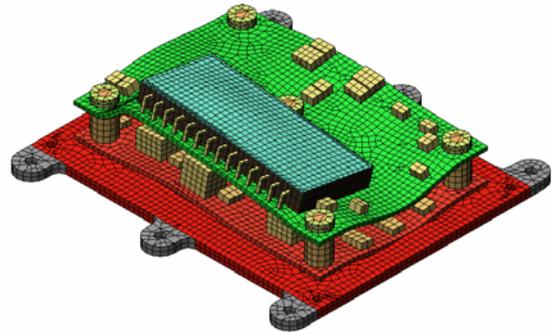


Figure 9. A Sample of Modal Analysis

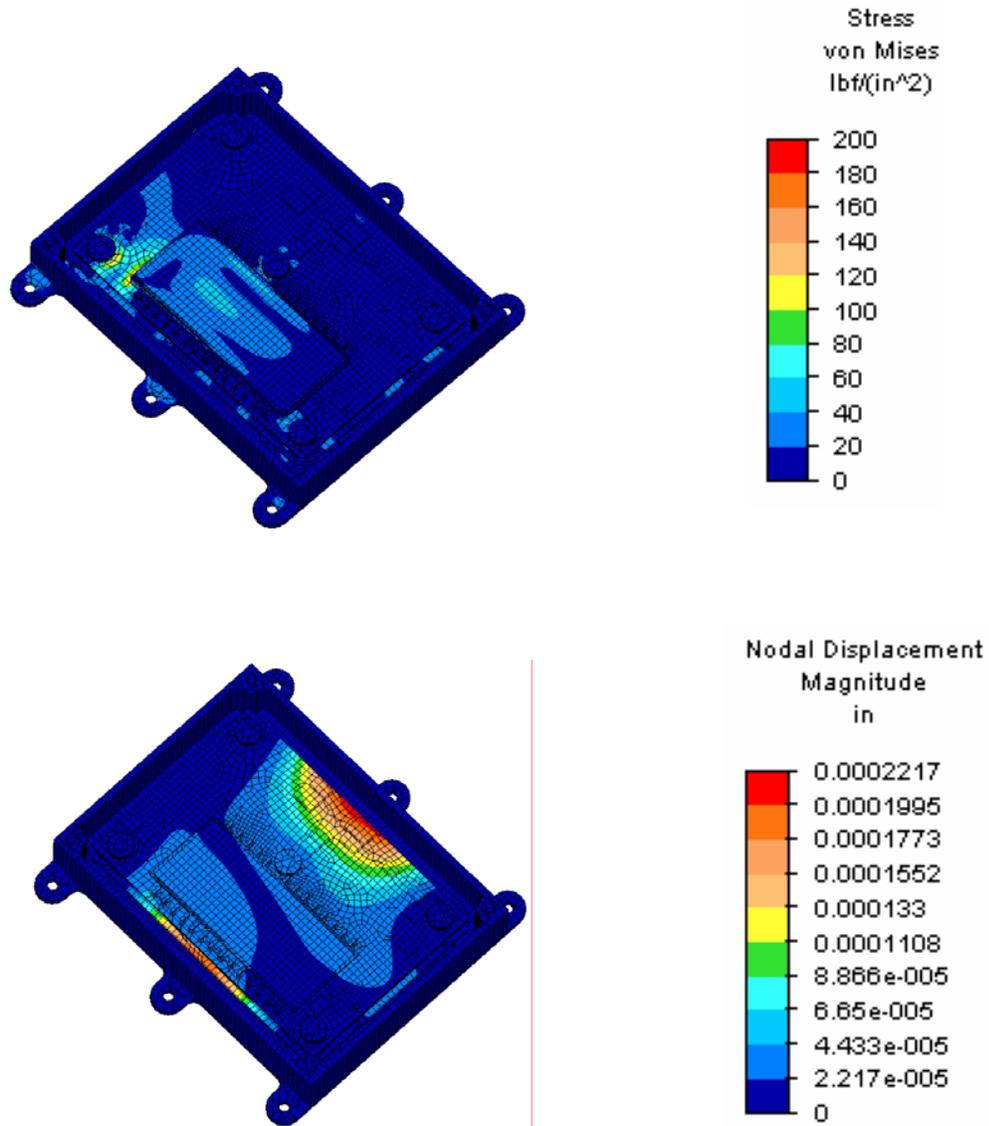


Modal Shape @ 1328 Hz



Modal Shape @ 2022 Hz

Figure 10. Samples of Random Vibration Analysis



Manufacturing Plan, Process and Qualification

Product reliability is the single most critical requirement for electronic equipment designed for space applications. Documentation is extensive and includes minute details for all aspects of the designs down to component and piece part level. For product manufacturing, a manufacturing plan describing the sequence of assembly, inspection and tests and the procedures required is first prepared. A manufacturing traveler is then created delineating each process and assembly

step. The processes and assembly procedures must be clearly detailed and qualified to insure proper execution and repeatability. The same requirements are demanded of the manufacture and assembly of preflight and flight hardware though to a slightly lesser extent for EM. Any assembly, inspection and test fixtures required must be clearly referenced and approved by customer prior to their use.

The low quantity demand of electronic flight hardware is the nature of the military space program. For most programs, the approximate required quantity is 1 to 5 units per ship set, for 1 to 4 ship sets, annually. A program may run 1 to 10 years or longer, but it often requires a performance upgrade in 2 to 4 years. This usually results in a redesign of the EPC and a change in product configuration. It poses tremendous challenges for a manufacturer to design and build an EPC with precision and consistency required to produce a world-class reliability product.

Design Qualification

EPC's designed for military spacecrafts are expected to provide continuous operation when subjected to considerable environmental conditions. They must continue to provide the required performance for a predetermined design life under the prescribed radiation environments and unlikely nuclear events. They must provide expected performances and function harmoniously in the electrical environment unique to the spacecraft system. One or more EQM samples must be subjected to the simulated environmental tests to insure design robustness and mechanical integrity. This qualification process usually takes place prior to design finalization with the design configuration of the EQM being form fit and function to flight hardware.

Environmental requirements are typically dependent of the launch vehicle. The radiation requirements are dependent of the intended orbit and mission. EMI/EMC requirements are unique to the spacecraft electrical power system and other electronics that share the power bus. Actual tests are normally required for environmental qualification and EMI/EMC while analysis usually suffices for radiation qualification for most programs.

Future Challenges

Higher efficiency means less wasted power, which equates to smaller power converters upstream, smaller solar panels, and less fuel on-board the spacecraft for the same design life. All these reductions add up to reduced spacecraft size, weight, and launch cost. The challenges for next generation EPC are to boost the efficiency performance and to reduce size and mass. The design goal is to reach the efficiency of 95% as soon as possible. For this goal to be realized innovations in the following areas are necessary; power circuits, packaging techniques to reduce conduction losses, switching elements, and magnetic materials.

Designers have always strived to reduce size and mass of hardware. Hybrid assembly has been the solution. New designs are incorporating hybrid assemblies. However, further reduction in mass is possible if and when a lighter alloy that has a compatible TCE with silicon is available.

Conclusions

Design and development of EPC's for military space applications require diverse engineering disciplines and extensive resources. Use of heritage designs and radiation-characterized components is the standard design solution. The combination of hybrid and SMT assembly is the new packaging trend to meet the critical size and mass requirements. Design analyses, product testing, product manufacturing, and design qualification require detailed documentation and customer concurrence. All the activities and efforts are designed to produce a highly reliable EPC with the highest level of confidence.

Acknowledgement

I would like to thank the following colleagues for their invaluable input, design and product information, graphics, and design analysis.

Mr. Jun Lu
Mr. Franck Ergas
Mr. Richard Wallstrom
Mr. Bjarne Soderberg
Mr. Lorentz Ou
Mr. Lass Pedersen

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