RIC7S113 TID test report

Total ionizing dose test report

About this document

Scope and purpose

This report provides the results of high dose rate (HDR) total ionizing dose (TID) test of the RIC7S113, rad hard high and low side 400 V MOSFET and IGBT gate drive IC. The test was conducted to determine the sensitivity of the device to the total dose environment. The test also included bias room temperature and high temperature anneal after radiation exposure.

Intended audience

This document is intended for radiation effects engineers who are looking to evaluate the radiation performance of the RIC7S113 for their specific mission.

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1 Part description

RIC7S113 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. It is intended for harsh radiation environments such as space, with electrical parameters specified pre and post-irradiation up to 100 krad(Si) and single effect effects (SEE) characterized up to a linear energy transfer (LET) of 81.9 MeV·cm^2/mg.

RIC7S113 enables high performance from key parameters. The high gate drive strength, low propagation delay and matching timing for high and low side drive help reduce loss in the power switch. Enhanced robustness from Schmitt trigger inputs, high allowable offset supply voltage transient slew rate, separate logic and gate drive supplies and wide voltage range between the various bias power returns help improve noise immunity. RIC7S113 also is flexible to meet a variety of different system requirements, with input pins that are compatible with CMOS logic and external logic shutdown pin. A block diagram of the RIC7S113 is shown in figure 1.

The high voltage support of up to 400 V allows for use in a range of high voltage applications, such as DC/DC converters and motor drive inverters in topologies such as half bridge, full bridge among others.

These devices are specified across the military temperature range of -55°C to 125°C and are available in a 14 lead ceramic dual flatpack, 18 lead ceramic leadless chip carrier (LCC CIC) and 14 lead dual in-line pin style (MO-036AB CIC) package or die form.

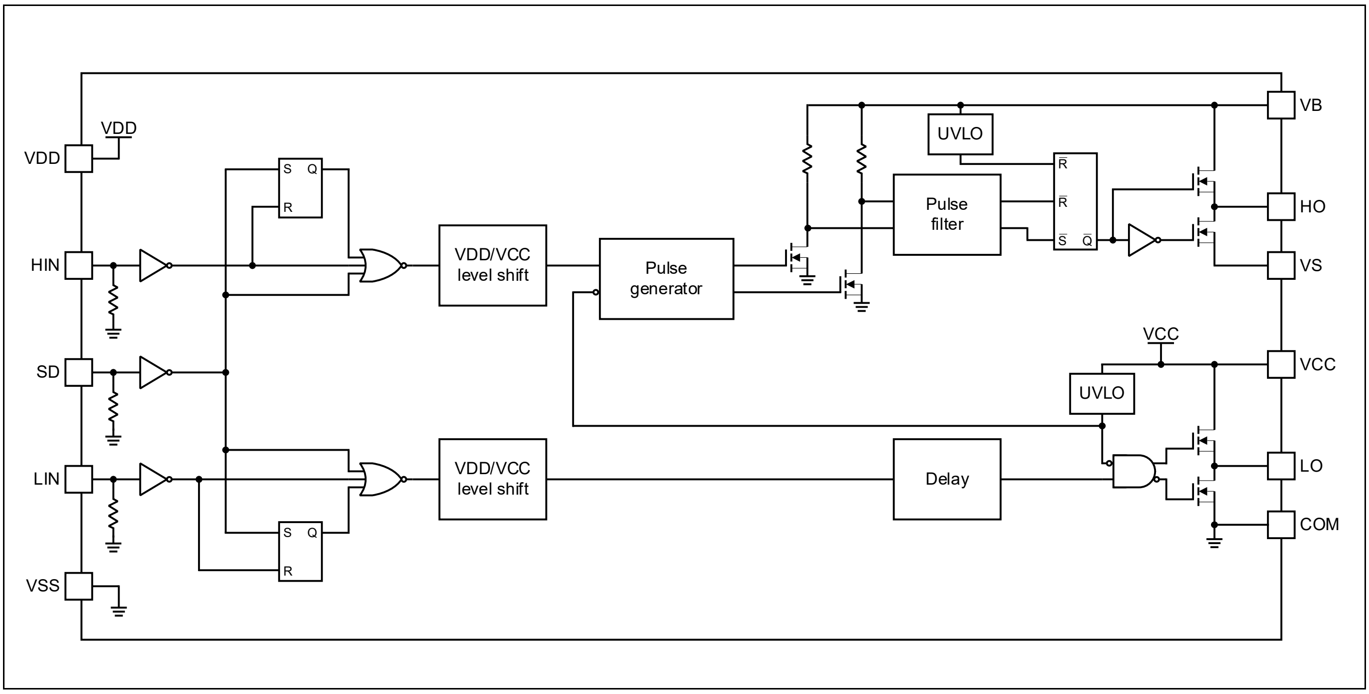

Figure 1 RIC7S113 block diagram

1.1 Related information

For a full list of related documents, visit the RIC7S113 device page.

2 TID test description

The RIC7S113 has been tested in accordance with MIL-STD-883 test method 1019. A total of 40 samples from 10 wafers in lot A991465.1 were assembled in the 18 lead LCC CIC package and screened through dynamic burn-in and static burn-in as required by MIL-STD-883 on January 18th, 2018. Radiation exposure is comprised of two electrical bias conditions, static and dynamic. Two samples from each wafer were biased in the static condition and two samples from each wafer were biased in the dynamic condition during irradiation. Additionally, two devices were used as control units to ensure repeatable data.

The samples were irradiated per the flow chart in 1019-1 of MIL-STD-883 TM1019, which requires an overtest factor of 1.5 of the 100 krad(Si) rating of the product. This allows for parametric failures to be subjected to an annealing process, which allows them to pass for lower dose rate environments (i.e space applications). Annealing was performed with the same bias condition used during irradiation. The conditions and the test flow can be summarized as:

- All samples were exposed to 150 krad(Si) at a dose rate of 105 rad(Si)/s with test down points at 50 krad(Si), 100 krad(Si) and 150 krad(Si)
- Following irradiation all samples were annealed at 25°C for 165 hours
- Lastly, all samples were annealed at 100°C for 168 hours.

The Radiation Hardness Assurance (RHA) program at IR HiRel tests every production wafer using the static and dynamic burn-in condition prior to TID exposure.

2.1 Radiation facility

All the parts were irradiated at the VPT Rad facility in Chelmsford, MA. VPT Rad offers high dose rate irradiation with its TID GC-200 irradiator. The facility meets the requirements of MIL-STD-750 and MIL-STD-883 and has approved source suitability from the Defense Logistics Agency.

2.2 Test schematics

Simplified schematics for the static and dynamic bias circuits are shown below.

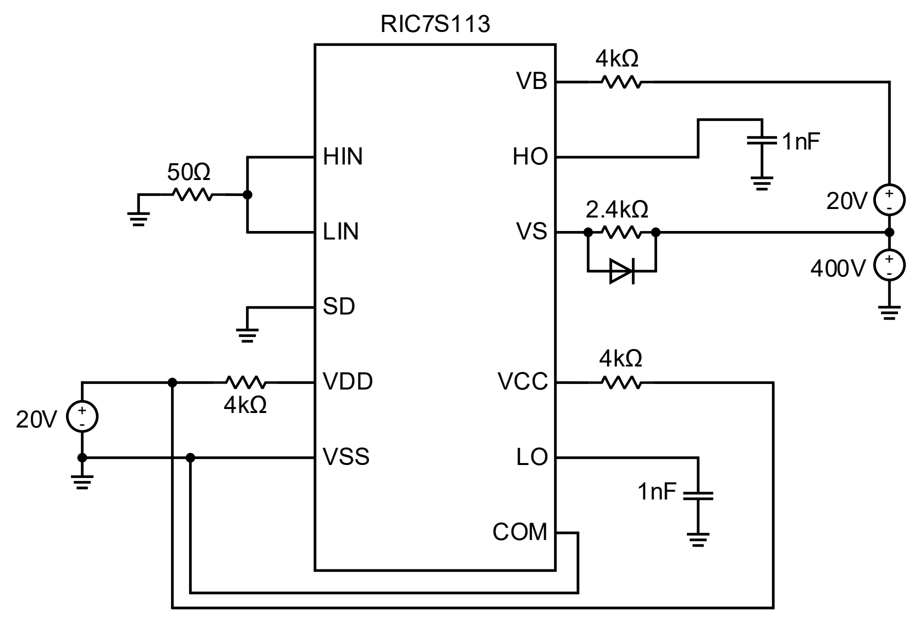

Figure 1 **Static bias condition for total ionizing dose (TID) test**

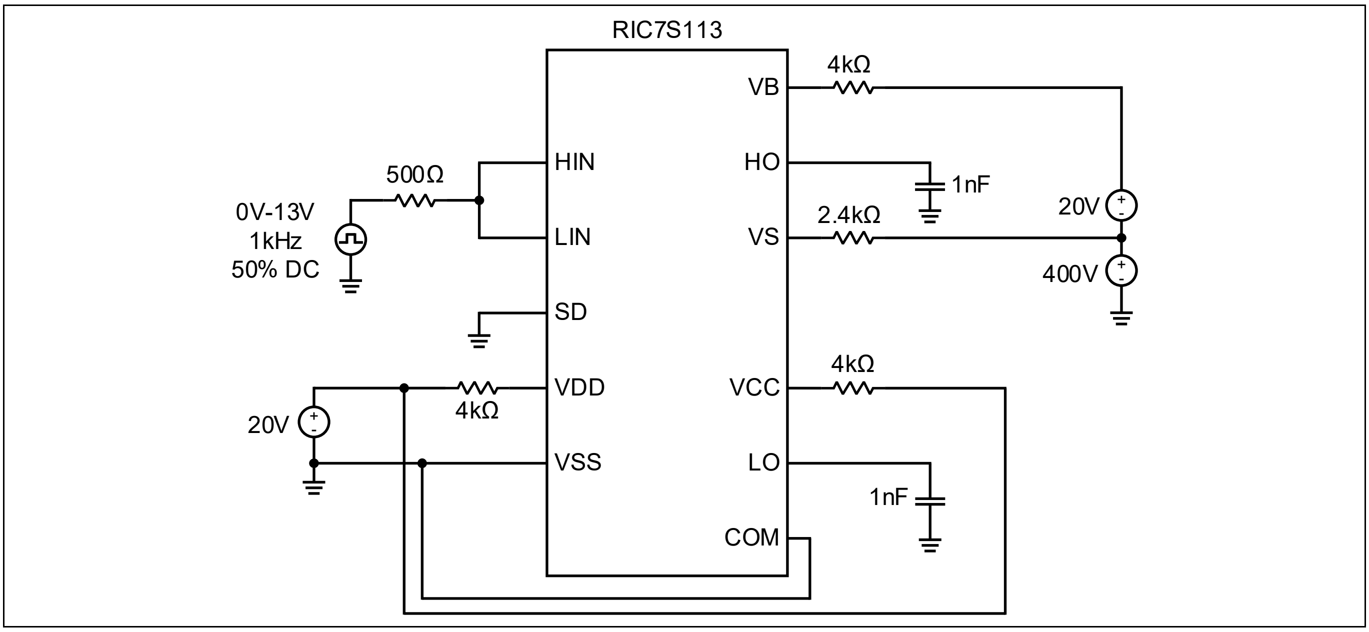

Figure 2 Dynamic bias condition for total ionizing dose (TID) test

2.3 Test equipment

All electrical tests were performed outside the irradiator using the production automated test equipment and production test program with data logging at each down point and after anneal. All electrical tests were performed at 25°C.

3 TID test results

The TID testing results show that some parameters shifted beyond their post radiation electrical limit. However, per test method 1019 paragraph 3.11.2, if the device fails the irradiation and testing, an additional room temperature annealing test may be performed. If the device under test passes electrical performance following the extended room temperature anneal, then the device is considered to have acceptable performance for a very low dose rate environment (i.e. space applications). All samples were annealed at 25°C for 165 hours after irradiation in compliance with test method 1019 and the flow chart in figure 1019-1 of MIL-STD-883 TM1019.

3.1 Attributes data summary

The table below summarizes the attributes data from the TID testing.

Table 1 **Attributes data summary**

Part	Wafer lot	Irradiation date	Dose rate	Bias condition	Sample size	Down point	Pass	Fail
RIC7S113	A991465.1	January 18, 2018	105 rad/s	Dynamic	20	Pre-irradiation	20	0
						50 krad(Si)	0	20
						100 krad(Si)	0	20
						150 krad(Si)	0	20
						25°C anneal	20	0
						100°C anneal	20	0
RIC7S113	A991465.1	January 18, 2018	105 rad/s	Static	20	Pre-irradiation	20	0
						50 krad(Si)	0	20
						100 krad(Si)	0	20
						150 krad(Si)	0	20
						25°C anneal	20	0
						100°C anneal	20	0

3.2 Variables data summary

The following figures plot the response of key electrical parameters of the RIC7S113 at all the irradiation down points and post anneal. The plot shows the mean of the parameters for each of the bias conditions during irradiation and anneal.

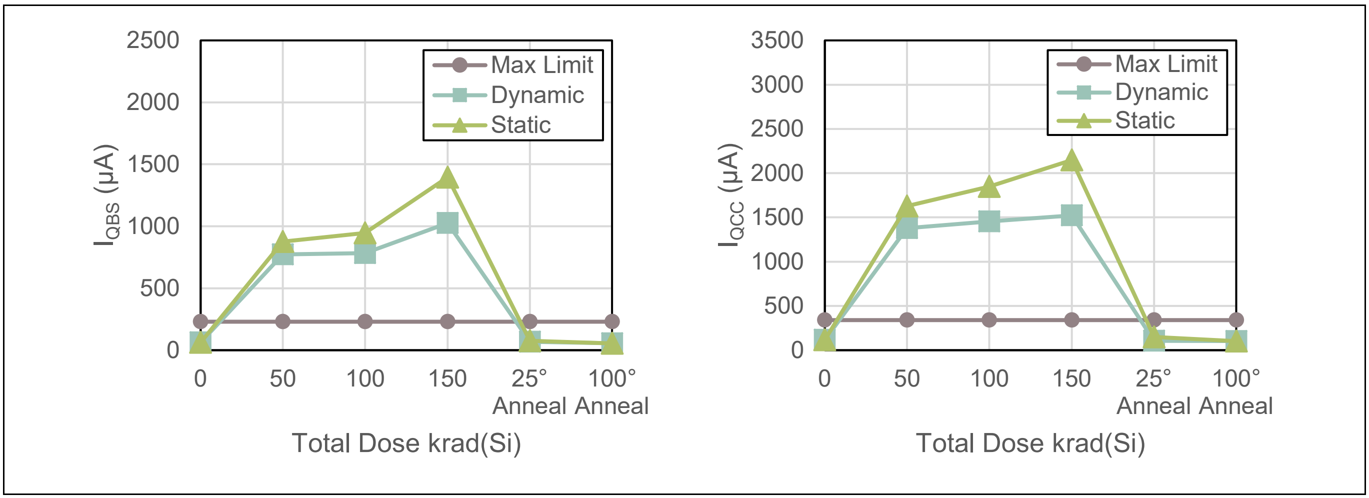

Figure 3 I_{QBS} (V_{BS} supply current) and I_{QCC} (V_{CC} supply current) and as a function of TID and anneal

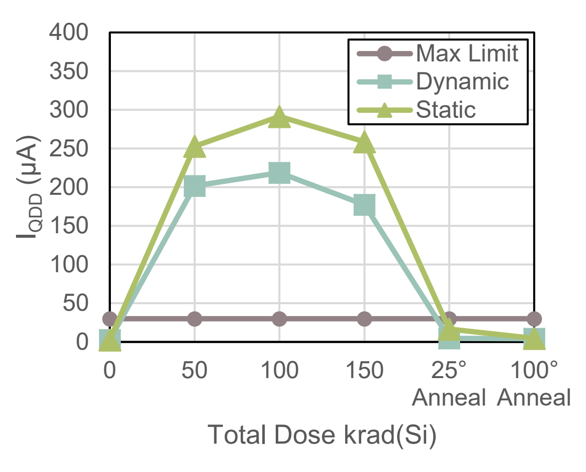

Figure 4 I_{QDD} (V_{DD} supply current) as a function of TID and anneal

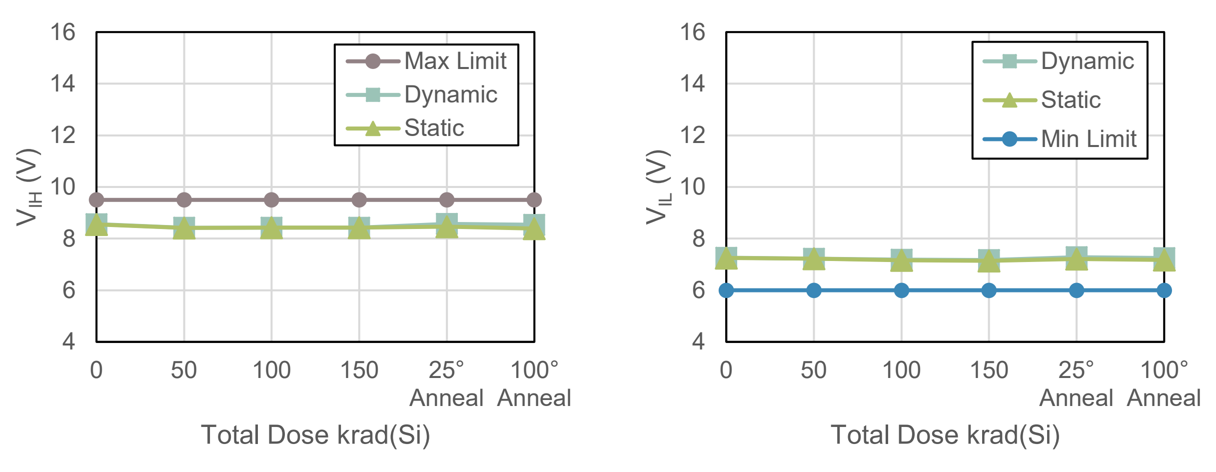

Figure 5 V_{IH} and V_{IL} as a function of TID and anneal

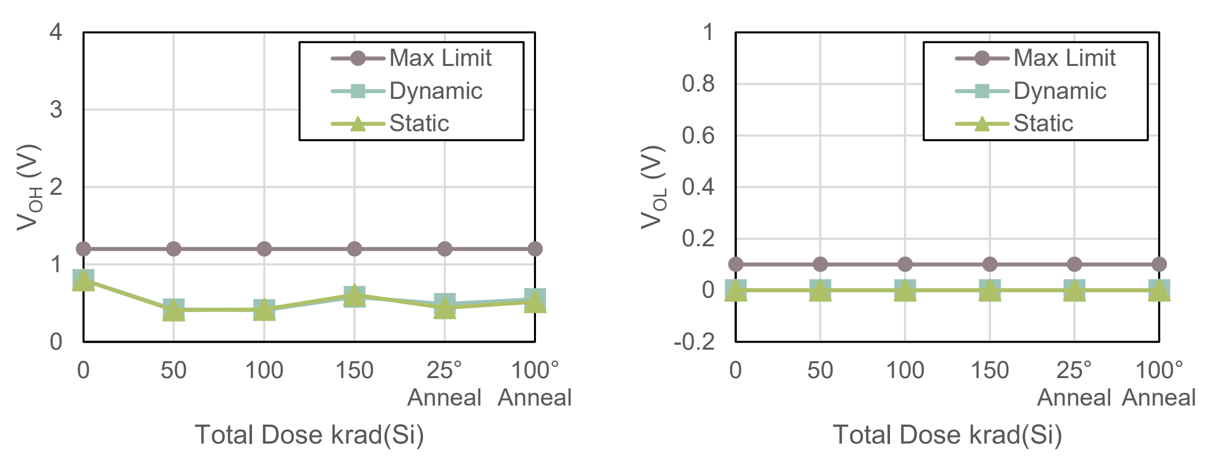

Figure 6 V_{OH} and V_{OL} as a function of TID and anneal

Attention: *In Figure 7, the max limit of I_{LK} is 50µA and is not plotted to show the granular response of I_{LK} as a function of radiation and anneal*

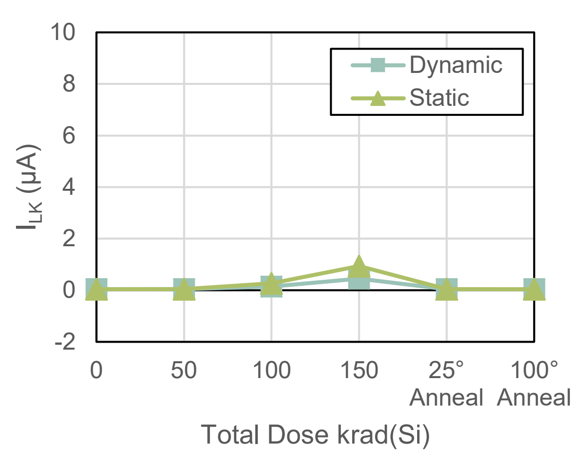

Figure 7 I_{LK}, offset supply leakage current, as a function of TID and anneal

4 Summary

The radiation testing of 40 samples from lot A991465.1 demonstrates the radiation hardness against ionizing radiation and the products suitability for space applications. The testing was conducting in accordance with MIL-STD-883 test method 1019. While some electrical parameters shifted beyond their limits during irradiation, all parameters are within specification limits after 25°C anneal for 165 hours.

Section 3.11.2 of test method 1019 in MIL-STD-883 states that the time of the room temperature anneal shall not exceed t_{max}, where:

$$t_{max} = \frac{D_{spec}}{R_{max}}$$

D_{spec} is the total ionizing dose specification for the part and R_{max} is the maximum dose rate for the intended application. For the RIC7S113 the maximum dose rate can be calculated by setting D_{spec} = 100 krad(Si) and t_{max} = 165 hours. This leads to maximum dose rate of 606 rad/hr which is above the dose rate encountered in most applications. Further annealing is not expected to have significant effect. This is demonstrated by the 100°C anneal which did not show significant change from the room temperature anneal.

5 Appendix

5.1 RIC7S113 post-irradiation test limits

All down point tests during irradiation, as well as anneal tests, are tested to the following limits. For a full list of test limits, including pre-irradiation limits, refer to the electrical characteristics in the RIC7S113 datasheet.

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V and $T_A = T_J$ = -55 to 125°C unless otherwise stated. V_{IN} ($V_{IH,}$ V_{IL}), V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input pins (HIN, LIN and SD). The V_O and I_O parameters are referenced to COM or V_S and are applicable to the respective output pins (HO or LO). **Parameter ratings that are stated post-irradiation apply over a total ionizing dose (TID) of 100 krad(Si) with exposure at a high dose rate (HDR) of 50-300 rad(Si)/s.**

Table 1 Static electrical characteristics

Symbol	Definition	Group A Subgroup[1]	Min	Typ	Max	Units	Test Conditions
Bias power							
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	1	7.5		9.7	V	T_J=25°C, **Post-irradiation**
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	1	7.0		9.4	V	T_J=25°C, **Post-irradiation**
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	1	7.4		9.9	V	T_J=25°C, **Post-irradiation**
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	1	7.0		9.6	v	T_J=25°C, **Post-irradiation**
I_{QBS}	Quiescent V_{BS} supply current	1			230	µA	V_{IN}=0V or VDD, T_J=25°C, **Post-irradiation**
I_{QCC}	Quiescent V_{CC} supply current	1			340	µA	V_{IN}=0V or VDD, T_J=25°C, **Post-irradiation**
I_{QDD}	Quiescent V_{DD} supply current	1			30	µA	V_{IN}=0V or VDD, T_J=25°C, **Post-irradiation**
I_{LK}	Offset supply leakage current	1			50	µA	VB=VS=400V, T_J=25°C, **Post-irradiation**
Input							
V_{IH}	Logic "1" input voltage	1	3.1			V	VDD=5V, T_J=25°C, **Post-irradiation**
		1	6.4			V	VDD=10V, T_J=25°C, **Post-irradiation**
		1	9.5			V	VDD=15V, T_J=25°C, **Post-irradiation**
		1	12.5			V	VDD=20V, T_J=25°C, **Post-irradiation**
V_{IL}	Logic "0" input voltage	1			1.6	V	VDD=5V, T_J=25°C, **Post-irradiation**
V_{IL}	Logic "0" input voltage	1			3.8	V	VDD=10V, T_J=25°C, **Post-irradiation**

Symbol	Definition	Group A Subgroup[1]	Min	Typ	Max	Units	Test Conditions
		1			6.0	V	VDD=15V, T_J=25°C, **Post-irradiation**
V_{IL}	Logic “0” input voltage	1			8.3	V	VDD=20V, T_J=25°C, **Post-irradiation**
I_{IN+}	Logic “1” input bias current	1			40	µA	V_{IN}=V_{DD}, T_J=25°C, **Post-irradiation**
I_{IN-}	Logic “0” input bias current	1			1.0	µA	V_{IN}=0V, T_J=25°C, **Post-irradiation**
Output							
V_{OH}	High level output voltage (V_{CC}-V_{LO}, V_B-V_{HO})	1			1.2	V	V_{IN}=V_{IH}, I_O=0A, T_J=25°C, **Post-irradiation**
V_{OL}	High level output voltage ($V_{LO,}$ V_{HO})	1			0.1	V	V_{IN}=V_{IL}, I_O=0A, T_J=25°C, **Post-irradiation**

[1] Per MIL-STD-883 Method 5005

Revision history

Document version	Date of release	Description of changes
Rev A	10/15/2021	Initial release
Rev B	3/25/2022	Formatting corrections

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