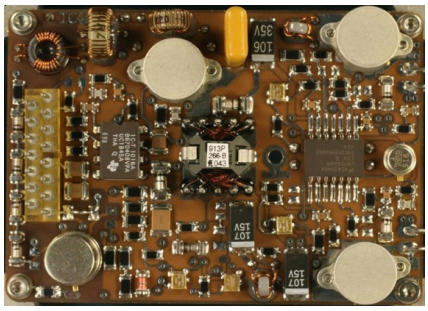
International
IOR Rectifier

PD-97807

HIGH RELIABILITY RADIATION HARDENED LOW POWER DC-DC CONVERTER

ML-SERIES

Nominal Voltage Input , Dual Output



Description

The ML-Series of isolated DC-DC converters for space applications are low power radiation hardened high reliability devices designed for hostile radiation environments such as those encountered by geostationary earth orbit satellites, deep space probes and communication systems. Features include small size, high efficiency, low weight, and a good tolerance to total ionizing dose, single event effects, and environmental stresses such as temperature extremes, mechanical shock, and vibration. All components are fully derated to meet the requirements of EEE-INST-002 (NASA) and ECSS-Q-30-11A (ESA). Extensive documentation including worst case analysis, radiation susceptibility, thermal analysis, stress analysis, and reliability analysis are available.

The ML-Series converter has two outputs – one positive and one negative - each is independently regulated via linear post regulators. The outputs are sequenced during turn-on and turn-off such the negative output comes up first at turn-on and stays up at turn-off until the positive output has decreased. The ML-series converters incorporate a fixed frequency flyback power converter and internal EMI filter that meets the requirements for most major satellite power buses. The converter includes isolated On/Off telecommand with associated status telemetry. The converter also includes input under voltage shut-down functionality.

Due to the linear post regulation of the outputs, the ML-Series is well suited for use in RF-applications where low noise, high output voltage accuracy, and high CS attenuation is required.

Each converter is provided as a complete board assembly for installation into the host equipment chassis. The board is conformal coated (except for mating surfaces) and is mounted in the host chassis using screws. The board outline is L x W x H: 70mm x 50mm x 18mm. The weight is less than 50 grams.

Features

- Total Dose > 100 krad(Si)
- SEE > 82 MeV•cm²/mg
- Low Weight < 50 grams
- DC Input Ranges can be accommodated within an Overall Range from 20V to 100V
- O/P 1: +1.5V to +15V (up to 500mA or 4.0W)
- O/P 2: -1.5V to -15V (up to 100mA or 1.0W)
- Output Sequencing: Output 2 rises first at turn-on and stays up at turn-off
- Output Ripple: < 1mVrms (100Hz - 50MHz)
- CS Rejection Input to Outputs: > 90dB (50Hz - 1.0MHz)
- 10MΩ @ 100VDC Isolation
- Input Under-Voltage Protection
- Meets Conducted Emission Requirements of Major Power Buses:
  100Hz - 100kHz: 80dBuArms
  100kHz - 10MHz: -20dB/decade
  10MHz - 50MHz: 40dBuArms
- Short Circuit and Overload Protection
- Meets Derating Requirements of EEE-INST 002 and ECSS-Q-30-11A
- Isolated On/Off Control via High Level Pulse Command (Latching Relay)
- Status Telemetry (Relay Contact Type)
- Workmanship Per IPC-A610 Class 3
- Board is Coated with ARATHANE-5750

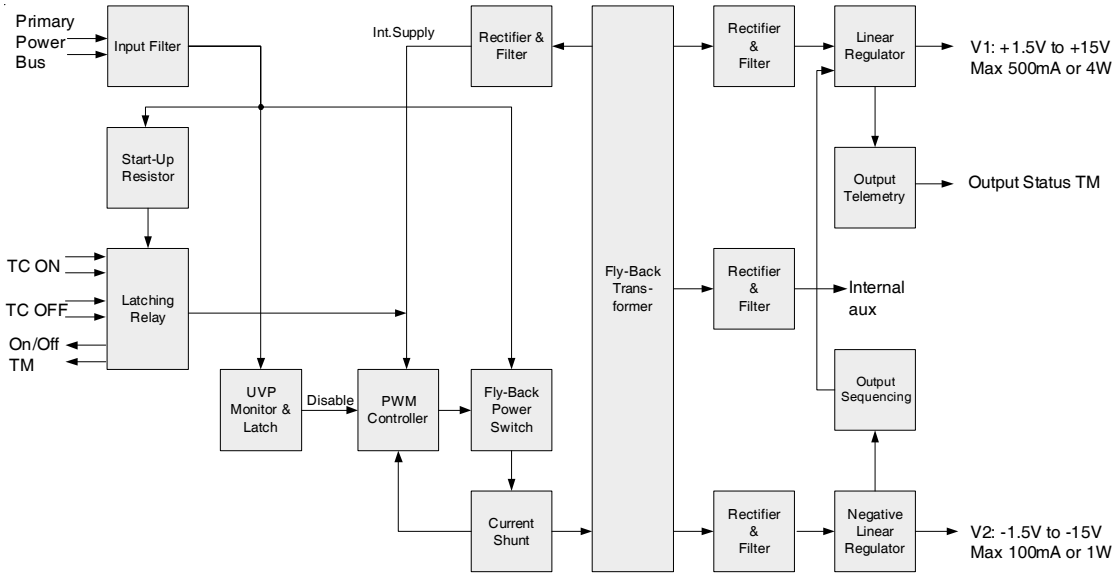
Applications

- Low Power RF Systems (like LNA) on-board Satellites

Non-flight versions of the ML-Series converters are available for system development purposes. Variations in electrical specifications and screening to meet custom requirements can be accommodated

Circuit Description

Fig 1- Block Diagram



Electrical Design Description

General

The ML-Series converters utilize two-stage regulation with a fly-back topology with a fixed switching frequency for primary regulation and linear post regulation in the secondary for each of the outputs.

Output power is limited under any load fault condition to approximately 120% of rated output. An overload condition on the positive output causes the converter output to behave like a constant current source with the output voltage dropping below nominal. An overload condition at the negative output causes both outputs to shut-down in order to protect RF-transistors in the load. The converter will resume normal operation when the load current is reduced below the current limit point.

An under-voltage protection circuit prohibits the converter from operating when the line voltage is too low for safe operation. In case of an under voltage event the converter will not start when the input voltage returns to its nominal level before an Off-command followed by an On-command has been issued.

The isolated On/Off telecommand is made with a latching relay and is intended for use with a 12V or 26V pulse command.

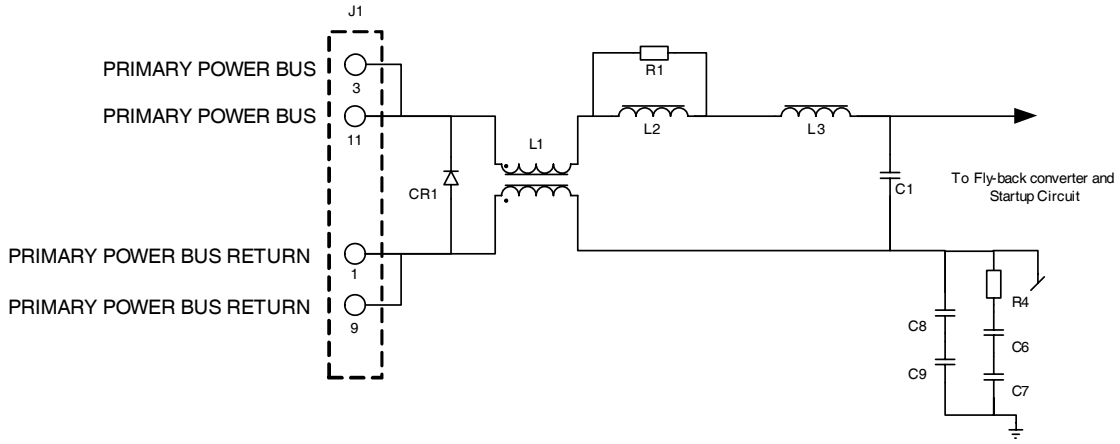
Input Filter

The converter is supplied from the primary bus through an input filter. The input filter selected is a second order resistively damped filter. The filter is chosen in order to provide sufficient damping of the ripple current towards the bus and the ripple voltage towards the converter.

As baseline for the filter dimensioning CE limit at 80dBuArms up to 100kHz decreasing to 40dBuArms at 10MHz, continuing at 40dB above 10MHz has been used. The input filter capacitors are non-redundant ceramic capacitors. The input bus is not protected from S/C faults from the primary side in the converter - protection element assumed implemented upstream the DC-DC converter. The bus is protected from failures on the secondary side by a primary current limiter and over current protection in the linear post regulators. Due to the overload protection on the outputs, failure propagation from the output to the input bus, through the converter, is not possible.

The interface circuit for the input filter is given in the diagram shown in Fig. 2.

Fig 2- Inerface Schematic for Input Filter



Fly-Back Converter

The fly-back converter supplying all the outputs is built up around a standard UC1845A PWM controller. The switching element is a 250V size 1 chip radiation hardened MOSFET from International Rectifier IRHF57214SE. The main transformer is a standard RM4 core.

When the converter is commanded On and is up and running it supplies itself from an extra winding on the power transformer in order to maintain a reasonable efficiency. The converter operates in current mode control; hence it includes inherently a primary current regulation and primary current limitation. Regulation is performed on the internal auxiliary supplying the PWM controller. The fly-back provides two outputs for supplying the functional outputs for the DC-DC. Each output uses diode rectification and is filtered by use of solid tantalum capacitors. Both outputs has an option for a ˜-filter at the inner side of the linear regulator this is to ensure that the converter ripple is removed to the maximum extent possible before entering the noise sensitive areas of the RF-Equipment.

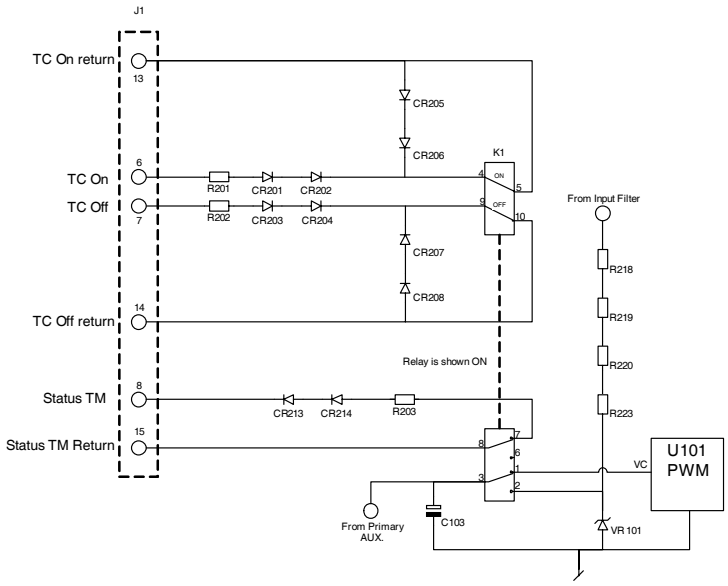
The switching frequency is fixed and set to nominally 140 kHz.

TC, TC Status, Primary Under-Voltage and Start-up

The DC-DC includes a galvanic isolated telecommand interface. The interface is made with a latching relay in a T0-5 package. Free-wheeling diodes are implemented across the On and Off coil to protect from inductive kick-back. The relay controls On/Off switching of the converter by controlling the PWM controller supply voltage. The relay switches only the PWM controller supply voltage (approximately 15V). The relay contacts do therefore not see the full bus voltage.

The interface circuit for the On/Off relay circuit is given in in Fig 3

Fig 3- Interface Schematic for Telecommand Interface



The telemetry is provided as an On/Off status telemetry, this telemetry is provided as an extra set of contacts on the relay. When the DC-DC converter is commanded Off the relay contacts will be open circuit offering more than 10MOhm resistance and when the DC-DC is commanded On, the contacts will be closed presenting a low well-defined resistance. Series diodes are included as an option in the design to ensure compliance to most satellite TM/TC subsystems.

The input UVP circuit senses the bus voltage and compares it to the input UVP-threshold. If the input voltage is below the limit, the circuit gives shut down signal to the PWM.

The UVP shut down function can be configured to be either latching or with automatic re-start. This configuration is set by manufacturer (not user changeable). In case of latching UVP in case of an UVP, the DC/DC will continue to be Off when the input bus returns to its normal range; the trip condition is reset by issuing an Off command followed by an On-command. The UVP trig level includes hysteresis for proper operation.

Linear Regulators

Linear post regulators are used for the outputs to comply with the strict requirements for voltage precision, noise, ripple, and CS rejection.

The linear post regulator is under normal load conditions operating in voltage mode with a high control BW. In case of an overload condition the current control loop will take over providing a constant current limitation.

Both the voltage and the current loop are based on discrete components, a standard quad Op-amp (two amplifiers per linear regulator) and MOSFET transistors as pass elements. This implementation is chosen for size and mass reasons as well as risk mitigation as the design has a very long and broad in-flight heritage.

For the positive output the serial pass element is a radiation hardened MOSFET (IRHF57034) in order to limit the voltage drop at high output current. The voltage loop is built around an op-amp. The constant current limitation when the limit is reached lower the output voltage until the output voltage has reached 0V if necessary.

With careful design of the control circuits and board layout a very high CS attenuation for the combination of fly-back converter and linear regulators is achieved, typically >100dB. The linear regulators also provide high attenuation of the ripple from the fly-back converter giving a low output CE (0.1mVrms) at the switching frequency. This is obtained even with headroom <1V, hereby a reasonable efficiency for the overall converter can be offered. The linear regulators also ensure very high output accuracy better than ±2% at worst case EOL conditions including initial setting, line- and load regulation, temperature variations, ageing, and radiation degradation.

Output Telemetry

A Bi-level status telemetry derived from the positive output is included in the design using a voltage divider with filtering directly from the positive output.

Timing / Sequencing

The linear regulators provide most of the architecture needed to provide timing between the outputs. At turn On, the negative output will come up first. When the negative output is present and in regulation it releases the positive output which hereafter slowly rises. At turn OFF the positive output will stop when the fly-back converter stops, and a small hold up circuit on the negative output ensures that the negative output keeps running after the positive has been discharged by the load. Also if the negative output is shorted the positive outputs will immediately be stopped. All done to ensure safe operation of the RF-electronics which often includes normally-on devices that requires presence of negative bias prior to applying positive voltages.

Mechanical Design

The DC-DC is considered a module forming part of the complete host equipment. The DC-DC is 'open board' ready for installation into the host equipment housing.

The DC-DC is delivered complete with input connections formed as solder pins and output solder terminals ready for installation with screws into the host equipment housing. The board is equipped with 5 mounting holes for M2 screws that serve as mechanical fixation, thermal path, and electrical return connection. The screw positions are hence a result of the mechanical design as well as the thermal analysis and EMC considerations.

The outline of the board is (L x W x H): 70mm x 50mm x 18mm. The mass is less than 50g.

The input bus voltage, telecommand, and status telemetry is provided by 15 wrap around pins supported by a plastic socket. The input pin section is placed in a grid similar to a D-Sub connector thus it is possible to offer a solution with a 15P D-SUB connector for the input power and TM/TC signals.

The output pins are provided using solder pads. The output pad section contains 8 pads allowing access to the outputs from both sides of the board.

The DC-DC converter is conformal coated (except on mating surfaces).

Vibrational Performance

In order to limit the PCB deflections which are critical with respect to fatigue failures of component leads, the basic Eigen frequency is approximately 1.0kHz.

The component mechanical mounting techniques are based upon standards used for similar equipment. Components with need of mechanical support with no natural mounting possibility (axial capacitors, BR40 Capacitors, RM cores etc.) are supported with a two-component epoxy glue (EC2216).

The construction does not include individual components with very high mass hence a distributed fixation of the PCB into the mechanical housing with M2x5 steel screws is satisfactory.

Thermal Design

The DC-DC converter will keep temperature derating as per EEE-INST-002 and ECSS-Q-30-11A up to an interface temperature at the mounting points of +75°C.

In order to respect the required component temperatures, a good thermal conductive path is required from the PCB and to the host equipment. This is achieved by a number of screw connections – one additional screw (compared to the need for mechanical fixing and ground connection) are placed at a critical component location.

Critical components are placed close to the mounting screws of the PCB. The PCB is provided with eight copper layers which, besides establishing the electrical connections, are used also for heat transfer. Additionally, plated through holes (0.5mm diameter) are used for establishing a heat path from the PCB component side to the solder side where needed.

Standard component mounting techniques considering the thermal constraints are used.

Design Methodology

The ML-Series is developed using a proven conservative design methodology, which includes selecting radiation tolerant, and established reliability components and fully derating to the requirements of EEE-INST-002 and ECSS-ST-11A. In addition to verification and qualification testing and full acceptance testing for deliverable units, the performance characteristics are verified by theoretical analysis including worst case analysis including radiation degradation, parts stress analysis, mechanical analysis and thermal analysis. Reliability Assessment per MIL-HDBK-217F2 has also been carried out.

Declared Parts Lists defining the EEE parts technical standard and Declared Materials Lists with material data including outgassing and surface treatment is part of the design standard.

Generic Envelope Data Sheet & Existing Models Listings

The ML-Series is made as a generic design allowing for adaptations to different satellite power buses and TM/TC systems, different output voltages and currents within the overall envelope specification defined for the ML-Series.

For each released variant of the ML-Series detailed data sheet exists with exact data for all parameters. Existing variants are listed in Table 1 below.

A generic envelope data sheet is presented to indicate the envelope specification within which the ML-series can be adapted to specific customer requirements that cannot be met with one of the existing model variants listed in Table 1 below.

Where the generic data sheet lists Min rated or Max rated value, it is necessary to look up the actual parameter in the data sheet for the specific variant in question – for new variants please contact IR HiRel Sales department.

ML-Series Product Variant	Input Voltage	Outputs	Data Sheet	Product Status
ML1000605D	100V (97 - 103V)	+6V, 500mA -5V, 100mA	IRF-551-1-PDS01 LINK AT IRF.COM	ACTIVE
ML50005R105D	50V (45 - 51V)	+5.1V, 850mA -5V, 25mA	IRF-551-2-PDS01 LINK AT IRF.COM	----
ML5000605D	50V (45 - 51V)	+6V, 500mA -5V, 100mA	IRF-551-3-PDS01 LINK AT IRF.COM	----
ML10007D	100V (97 - 103V)	+7V, 500mA -7V, 50mA	IRF-551-4-PDS01 LINK AT IRF.COM	----

Specifications

Absolute Maximum Ratings		Recommended Operating Conditions	
Input voltage range	-0.5Vdc to +Max rated	Input voltage range (Note 9)	+Min rated to +Max rated
Output power	Internally limited	Output power	0 to Max. Rated
Operating mounting point temperature (Note 10)	-55°C to +100°C	Operating mounting point temperature (Note 10)	-40°C to +75°C *
Storage temperature	-55°C to +125°C	Cold start temperature (Note 9)	-55°C

Electrical Performance Characteristics

* Meets full derating

Parameter	Condition	Conditions -40°C ≤ Tc ≤ +75°C $V_{IN} = V_{Nom}$ DC ± 0.5%, C_L = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
Primary Input voltage			Min rated	Nominal	Max rated	V
Output voltage (V_{OUT}) (Out 1 / Out 2)		Note 1				
+V1	1	0% ≤ I_{OUT} ≤ 100% rated load	99.5	100	100.5	%
-V2	1		99.5	100	100.5	
+V1	2	0% ≤ I_{OUT} ≤ 100% rated load	99.0		101.0	%
-V2	2		99.0		101.0	
+V1	3	0% ≤ I_{OUT} ≤ 100% rated load	98.0		102.0	%
-V2	3		98.0		102.0	
Output power (P_{OUT}) (Out 1/ Out 2)						
+V1	1,2,3	V_{IN} = Min rated, Nominal, Max rated			5.0	W
-V2		Either Output			1.0	
Output current (I_{OUT}) (Out 1/ Out 2)						
+V1	1,2,3	V_{IN} = Min rated, Nominal, Max rated	0		500	mA
-V2		Either Output, Note X	0		100	
Line regulation (VR_{LINE}) Each output	1,2,3	V_{IN} = Min rated, Nominal, Max rated I_{OUT} = 10%, 50%, 100% rated	-1.0		1.0	mV
Load regulation (VR_{LOAD}) Each output	1,2,3	V_{IN} = Min rated, Nominal, Max rated I_{OUT} = 10%, 50%, 100% rated	-1.0		1.0	mV
Cross regulation (VR_{CROSS})	1,2,3	V_{IN} = Min rated, Nominal, Max rated , Note 1			1.0	mV
Input current	1,2,3	I_{OUT} = 0, commanded On				
		V_{IN} Min ≥ 50V		10	15	
		V_{IN} Min < 50V		20	30	mA
		Commanded Off			2.0	
Switching frequency (F_S)	1,2,3	Notes 1, 7	Min rated	Nominal	Max rated	kHz
Input under voltage Trig level	1,2,3	0% ≤ I_{OUT} ≤ 100% of rated load	Min rated		Max rated	V
Output Sequencing Turn-on delay O/P 2 to O/P 1 Turn-off delay O/P1 to O/P 2	1,2,3	I_{OUT} ≥ 20% for output 1	2.0 1.0		12 8.0	ms

For Notes to Specifications, refer to page 10

Electrical Performance Characteristics (continued)

Parameter	Condition	Conditions -40°C ≤ Tc ≤ +75°C V_{IN} = V_{Nom} DC ± 0.5%, C_L = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
Output ripple (V_{RIP}) Each output +V1 -V2 +V1 -V2	 1 1,2	V_{IN} = Min rated, Nominal, Max rated I_{OUT} = 100% rated load Frequency domain 100Hz – 50MHz Note 1 Time domain 100Hz – 50MHz Notes 1, 2			 1.0 1.0 Max rated Max rated	 mVrms mVpp
Efficiency (E_{FF}) For combined output power of no greater than 1.0W 2.5W 5.0W	 1,2,3	 I_{OUT} = 20% rated load I_{OUT} = 50% rated load I_{OUT} = 100% rated load	 Min rated Min rated Min rated			 %
Telecommand I/F Pulse Voltage high Nominal 26V Type Nominal 12V type Pulse Voltage low Pulse duration	 1,2,3	 Note 1	 +22 +12 -40 10		 +30 +17 0.5 1000	 V V V ms
Telemetry Converter On Converter Off	 1,2,3		 Min rated 1.0		 Max rated	 Ω MΩ
Current Limit Point Each output +V1 -V2	 1,2,3	 V_{OUT} = 100mV below Nominal	 Min rated Min rated		 Max rated Max rated	 mA
Output response to step load changes (V_{TLD}) +V1 -V2	 1,2,3	 20% to/ from Full Load, Note 3	 Min rated Min rated		 Max rated Max rated	 mV pk
Recovery time, step load changes (T_{TLD}) +V1 -V2	 1,2,3	 20% to/ from Full Load , Notes 3, 4			 2.5 2.5	 ms
Turn-on Response Overshoot (V_{OS}) +V1 -V2 Turn-on Delay (T_{DLY})	 1,2,3	 10% Load, Full Load Note 5	 2.0		 10 10 10	 mV ms
Capacitive Load (C_L) +V1 -V2	 1	 I_{OUT} = 100% rated load No effect on DC performance Notes 1, 6 Each output			 Max rated Max rated	 µF

For Notes to Specifications, refer to page 10

Electrical Performance Characteristics (continued)

Parameter	Condition	Conditions -40°C ≤ Tc ≤ +75°C V_{IN} = V_{Nom} DC ± 0.5%, C_L = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
EMC conducted susceptibility (Line rejection)	1	I_{OUT} = 100% rated load Primary power sine wave injection of 2Vp-p, 100Hz to 1MHz, Note 1	96	110		dB
EMC conducted emission Power Input	1	I_{OUT} = 100% rated load, Notes 1, 7	Max Limit: 100Hz – 100kHz: 80dbµArms 100kHz – 10MHz: 20db/decade 10MHz – 50MHz: 40dbµArms			
EMC conducted emission Power Outputs	1	I_{OUT} = 100% rated load, Note 1	Max Limit: 100Hz – 50MHz: 60dbµVrms			
Isolation	1	Input to Output, any potential to telecommand input and any potential to telemetry output, test @ 100VDC	10			MΩ
Device Weight					50	g
Failure Rate		MIL-HDBK-217F2, SF, 35°C, Note 8			60	FITs

Notes: Specification and Electrical Performance Characteristics Tables

1. Parameter is tested as part of design characterization or after design changes. Thereafter, parameter shall be guaranteed to the limits specified.
2. Guaranteed for a D.C. to 50MHz bandwidth. Tested using a 10.7MHz bandwidth.
3. Load step transition time ≥ 10 µs.
4. Recovery time is measured from the initiation of the transient to where VOUT has returned to within ±1% of its steady state value.
5. Turn-on delay time from application of telecommand pulse to the point where Output 2 = 98% of nominal output voltage.
6. Capacitive load may be any value from 0 to the maximum limit without compromising the output sequencing performance. A capacitive load in excess of the maximum limit may influence the output sequencing performance and start-up time, converter operation and dc performance will remain intact.
7. The switching frequency and 1st and 2nd harmonic of the input ripple is tested on every unit.
8. MIL-HDBK-217F2 stress-dependent method is used with 2 exceptions: For soldering a fixed failure rate at 0.035FIT is used and for power MOSFETs the dissipated power (instead of rated power) is used for the Pr parameter. 1 FIT is 1 failure in 10^9 hours.
9. The converter meets full derating per EEE-INST-002 and ECSS-Q-30-11A with the following exception: For Schottky diode JANS1N5819 a maximum derated junction temperature of +110°C. For EEE-INST-002 it is required that ceramic capacitors with a voltage stress below 10V shall be rated for minimum 100V - in the product such capacitors is rated for 50V minimum.
10. Although operation temperatures between -55°C to +100°C and -40°C to+75°C is guaranteed, no parameter limits are specified.

Electrical Performance Characteristics - Definition of Conditions

Condition	Definition	Comment
1	BOL @ +25°C interface temperature	Initial setting
2	BOL @ -40°C to +75°C interface temperature	Initial setting and worst case temperature variation
3	EOL @ -40°C to +75°C interface temperature	Worst case performance including initial setting, temperature variation, aging and radiation degradation

Grounding and Isolation Scheme

Parameter	Grounding & Isolation Performance
Isolation:	
prim. to secondary:	> 10 MOhm // < 50nF
Telecommand:	Floating
Status TM:	Floating
Grounding:	Secondary return bound to chassis via multiple screw connections

Model Definition and Test Plans

Model Definition

Model	Description	Build Standard
EBB	The EBB is an electrical representative model. The EBB is intended to be used by customers in their proto type at equipment level. EBB models are built at IR's Danish Design Center.	The PCB will be hand soldered by the engineering group. No staking and conformal coating is foreseen Preferably same type of EEE parts as intended for flight, but lower grade will be used for convenience. For resistors and capacitors different types with same basic characteristics may be used
EQM	The EQM is an electrical and mechanical representative model. The EQM is intended to be used by customer in their EQM at equipment level.	Flight standard for processes. Same type of EEE parts as intended for flight, but lower grade may be used for convenience.
FM	Flight standard models.	Full flight standard

Test Plan - A

The EBB must pass the following tests:			
Test No.	**Type of Test**	**Location***	**Remarks**
1	Electrical performance test, room temperature incl. Limited EMC test (CE 50kHz-1MHz)	IRD	Acceptance Test Procedure
2	Electrical performance test in temperature (Q-level)	IRD	Acceptance Test Procedure
3	Electrical performance test, room temperature incl. Limited EMC test (CE 50kHz-1MHz)	IRD	Acceptance Test Procedure
4	Final Inspection	IRD	General inspection Procedure

Test Plan - B

The EQM must pass the following tests:			
Test No.	**Type of Test**	**Location***	**Remarks**
1	Electrical performance test, room temperature incl. Limited EMC test (CE 50kHz-1MHz)	IRSJ	Acceptance Test Procedure
2	Thermal cycling with electrical monitoring of input and outputs (Q-level)	IRSJ	Acceptance Test Procedure 10 cycles
3	Electrical performance test in temperature (Q-level)	IRSJ	Acceptance Test Procedure
4	Random Vibration test in (Q-level)	External test house	Vibration Test Procedure
5	Electrical performance test, room temperature incl. Limited EMC test (CE 50kHz-1MHz)	IRSJ	Acceptance Test Procedure
6	Mechanical Measurements	IRSJ	Acceptance Test Procedure
7	Final Inspection	IRSJ	General inspection Procedure

Test Plan - C

The FM must pass the following tests:			
Test No.	**Type of Test**	**Location***	**Remarks**
1	Electrical performance test, room temperature incl. Limited EMC test (CE 50kHz-1MHz)	IRSJ	Acceptance test procedure
2	Electrical performance test in temperature (A-levels)	IRSJ	Acceptance test procedure
3	Electrical performance test, room temperature incl. Limited EMC test (CE 50kHz-1MHz)	IRSJ	Acceptance test procedure
4	Electrical performance test, room temperature	IRSJ	Acceptance Test Procedure
5	Mechanical Measurements	IRSJ	Acceptance test procedure
6	Final Inspection	IRSJ	General inspection procedure

Note:
Location* - IRD: IR's Danish Design Center, Skovlunde, Denmark
- IRSJ: IR's Site in San Jose, California, USA

Radiation Performance

TID

The TID radiation performance is guaranteed by worst case analysis with radiation degradation data for each radiation sensitive component used in the DC-DC converter. For TID radiation verification testing (RVT) for each wafer lot for all sensitive components is part of the EEE parts requirements per table below.

Component Type	RVT Plan (applicable to all flight lots)
JANS2N2222A	LDRS 0.01 to 0.1 rad up to 200 krad per IR RVT plan
JANS2N2907A	LDRS 0.01 to 0.1 rad up to 200 krad per IR RVT plan
JANSR2N7492T2	RVT by Manufacturer (HDR)
IRHF57214SESCS	RVT by Manufacturer (HDR)
IRHLUB770Z4SCS	RVT by Manufacturer (HDR)
IRHLUB7970Z4SCS	RVT by Manufacturer (HDR)
LM124AWR	RVT by Manufacturer (ELDRS)
IS2-1009RH	RVT by Manufacturer (HDR) LDRS 0.01 to 0.1 rad up to 100 krad per IR RVT plan
UC1845A	LDRS 0.01 to 0.1 rad/s up to 100kRad per IR RVT plan

SEE

The SEE radiation performance is guaranteed by a combination of derating and mitigation at circuit level. For mitigation at circuit level both theoretical analysis and testing with imposed SEE effects are performed. The applicable SEE and mitigation concept is presented in table below.

The maximum output perturbation is 5% of the nominal output voltage during any SEE.

Applicable SEE and Mitigation Methods Table

Component Type	Applicable SEE	Mitigation Concept
RH MOSFET	SEGR	Vds derating in combination with SEE SOA curves from manufacturer data sheet
Op-Amp	SET, 15us perturbation to rail	Mitigation at circuit level (filtering)
Voltage reference	SET, 10us perturbation to rail	Mitigation at circuit level (filtering)
PWM	SET, 15us perturbation to rail	Mitigation at circuit level (filtering)
	Double Pulses	Mitigation at circuit level (filtering, no saturation of magnetic parts)
	Missing Pulses	Mitigation at circuit level (filtering, no saturation of magnetic parts)

EEE Parts Technical Standard

Component Screening

Component Class	Component Type	Specification	Quality / Screening Level (minimum)
Capacitors	BR40	ESCC 3001/030	ESCC Level B
	CDR31-34 BP	MIL-PRF-55681	MIL-S
	CDR31-34BX	MIL-PRF-55681	MIL-S
	CWR29	MIL-PRF-55365	Weibull C, surge current option B
Diodes	1N6640US	MIL-PRF-19500/609	JANS
	1N5806US	MIL-PRF-19500/477	JANS
	1N5819UR-1	MIL-PRF-19500/586	JANS
Relays	J422-26M Shock resistant	TR-HiRel-1/422	See Note 1
Inductors	MPP toroids product specific	MIL-STD-981	See Note 2
	Ferrite toroids product specific	MIL-STD-981	See Note 2
Bipolar Junction Transistors	2N2222A	MIL-PRF-19500/255	JANS
	2N2907A	MIL-PRF-19500/291	JANS
Power MOSFET	IRHLUB770Z4	MIL-PRF-19500/744	JANS
	IRHLUB7970Z4	MIL-PRF-19500/745	JANS
	IRHF57034	MIL-PRF-19500/703	JANS
	IRHF57214SE	MIL-PRF-19500/703	JANS
Resistors	RM1005B	MIL-PRF-55342	MIL-R
	RM1206B	MIL-PRF-55342	MIL-R
	RWR81	MIL-PRF-39007	MIL-S
Transformers	Ferrite RM4, product specific	MIL-STD-981	See Note 2
ICs	IS2-1009	MIL-PRF-38535	QML V
	LM124A	MIL-PRF-38535	QML V
	UC1845A	MIL-PRF-38535	QML V
Zeners	1N4109UR-1	MIL-PRF-19500/435	JANS

Notes:

1. Screening as per MIL-PRF- 9016 with additional screening as per Teledyne test specification 0-40-837 rev B
2. Custom magnetics (chokes and transformers) screening is as per MIL-STD-981 with exception for: Radiographic inspection, monitoring during last thermal shock cycle, power burn-in

DPA Rules

Component Class	Component Type	Specification	Quality / Screening Level (minimum)
Capacitors	Ceramic, solid tantalum	3 pcs / value /datecode	
Diodes	QPL-listed	3 pcs / datecode	No precap CSI
IC's	QPL-listed	3 pcs / datecode	No precap CSI
Relays		3 pcs / datecode	
Resistors		None	
Transistors	QPL-listed	3 pcs / datecode	No precap CSI
	Non-QPL	3 pcs / datecode	Precap CSI (except for IR MOSFETs, tested to be SCS parts)

Pin Designation Tables

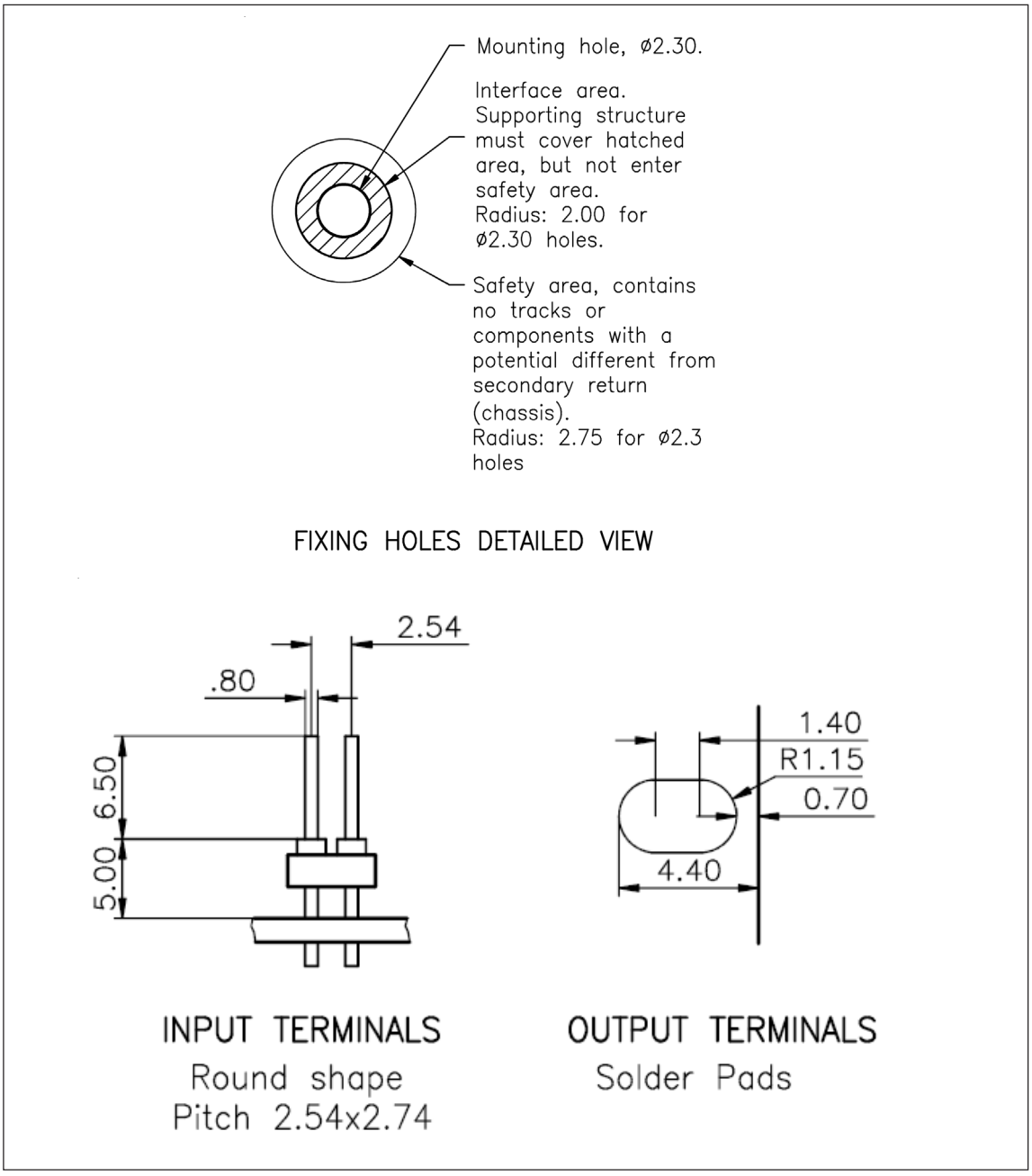
Input Terminals Assignment List		
Indent.: Input Terminals (Solder, Pins, Straight)		
Pin #	Pin #	Function
	1	Input Power Return
9		Input Power Return
	2	Rerserved
10		Rerserved
	3	Input Power
11		Input Power
	4	Chasis (Ground)
12		Voltage TM
	5	Chasis (Ground)
13		TC On Return
	6	TC On
14		TC Off Return
	7	TC Off
15		TM Status Return
	8	TM Status

Output Terminals Assignment List		
Indent.: Output Terminals (Solder Pads)		
Pin #	Pin #	Function
1	2	V1 (Positive Output)
3	4	Chasis (Ground)
5	6	Chasis (Ground)
7	8	V2 (Negative Output)

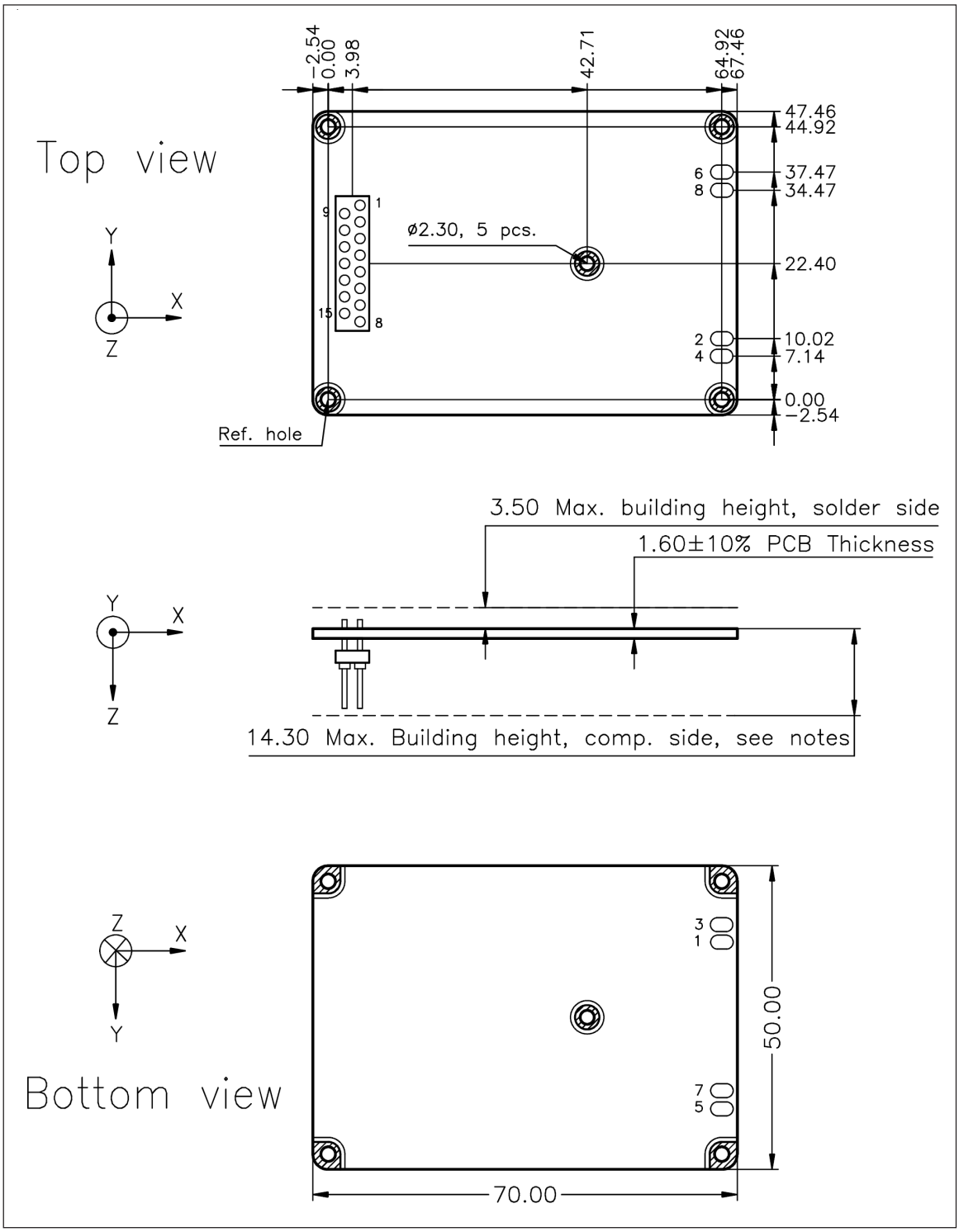
Recommended Mounting Stud Design

It is foreseen with a mounting stud design with circular mounting studs made out of aluminum with a diameter of 4.0mm and a treaded hole support mounting with M2 screws.

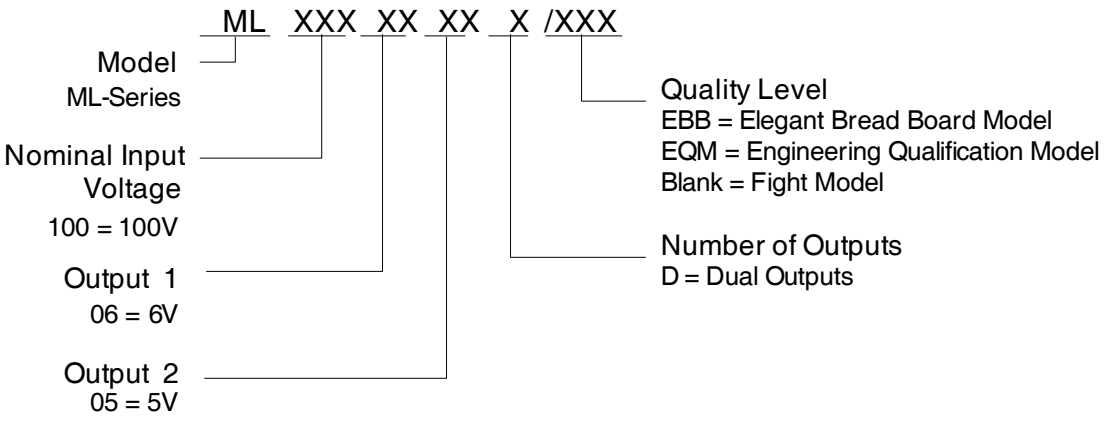
5pcs M2 screws are used for mounting the board. Mounting torque shall be 30Ncm ± 5.0Ncm.



Mechanical Diagram



Part Numbering



Application Information

Standard Documentation

- Interface Control Drawing
- Users's Manual
- End Item Data Package with Coc, Applicable Configuration, MIP Photo and Test Results

Design Justification Documentation

The following documentation can be made available upon request:

- Worst Case Analysis
- Parts Stress Analysis
- Thermal Analysis
- Mechanical Analysis
- FMECA
- Reliability Assessment
- Declared Components List
- Declared Materials List
- Declared Process List

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Data and specifications subject to change without notice. 04/2013