The E series of electronic power condition (EPC) modules have been specifically designed to facilitate use in RF equipment especially solid state power amplifiers (SSPAs) and transmitters on board a spacecraft. For that purpose the EPC is a three output DC-DC converter with unique output sequencing required by GaAs FET commonly used in the SSPA designs. The E series has three output power platforms. They are 60W, 100W and 170W. The EA series 60W output power rating is the lowest power rating for the E series. The main output delivers a user programmable output voltage of 7.5 to 9V typically the drain supply for the GaAs FET. The +5V output is a low noise supply for logic and pre-amplifier stages of the SSPA. And finally the negative 5V output is a low noise output for supplying logic and gate bias for the RF-transistor. These are the standard voltages. Consult factory for other output voltage requirements.

The EA incorporates two design patents which enable the efficiency performance to exceed 90%. In addition to its world class efficiency the EA EPC is equipped with numerous functional features commonly required by today's state-of-the-art space design requirements. They include ULVO, over-voltage protection, pulse on/off command, output status, input current telemetry, and in-orbit programmable main output.

E series converters are designed specifically for operations in radiation environments that are presented to commercial, military and scientific satellites operating in long term GEO, MEO and LEO orbits. They have been created to complement the spectrum of electrical and radiation performance available in the International Rectifier's ART, S, LS, M3G, and Z series converters.
Design Patents

IR Denmark design expertise also features two US patents, the Hybridge Rectification Concept and the Integrated Magnetic Design. The E-series incorporates these design patents which boost the efficiency performance of the E-series design platform to be the highest in the industry. A block diagram of the patented design topology is shown below.