IOR International Rectifier

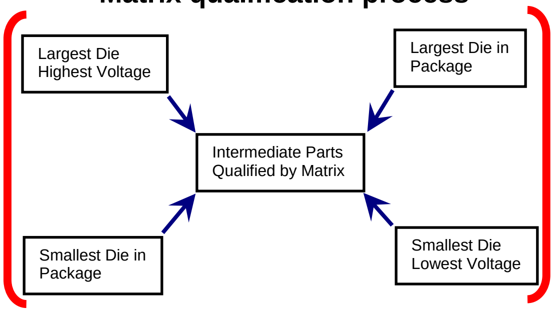
Reliability & Quality Engineering

Tests & Reliability

Completed and Qualified to Spec

- ✓ Solder standoff trials
- ✓ Screen aperture design
- ✓ Placement force
- ✓ Solder vendors
- ✓ Substrate bend strength measurements
- ✓ Package parasitics
- ✓ Shock/drop testing
- ✓ Vibration testing
- ✓ Temperature/power cycling on IMS
- ✓ Temperature/power cycling on ceramic
- ✓ Temperature/power cycling on Pb-free solder
- ✓ High frequency parasitic evaluation
- ✓ HTRB, HTGB, THB
- ✓ Moisture absorption

Matrix qualification process


Largest Die Highest Voltage

Largest Die in Package

Intermediate Parts Qualified by Matrix

Smallest Die in Package

Smallest Die Lowest Voltage

“The worst and best case parts **bracket** the rest of the part types within the family for a given test”. This statement holds only if the family members have been chosen well. Thus there are three key factors in the matrix qualification process:
- select the families and family members correctly
- identify critical devices attributes
- choose appropriate reliability tests for best and worst case part types

http://www.irf.com/product-info/hexfet/dfreliability.html

Key factors in Die level reliability estimation

1. Field Distortion

Cause: polar molecules (i.e. water and ionic contaminants) on passivation surface and die’s edge

Effect: increased local leakage current and thermal runaway due to distorted electric field when high voltage is applied.

The failure rate is accelerated by HTRB & HTB test conditions. The best case is the device with the lowest voltage rating type in the family. The worst case device types are those that produce the highest field strengths.

2. Oxide Defects

Cause: defects in the gate oxide

Effect: lead to failures in the form of a gate-to-source short circuit

They can be activated by high-temperature gate-stress/bias (HTGS or HTGB) testing. The worst case device is subjected to the greatest field strength at the highest temperature.

Key factors in Package level reliability estimation

1. Die Attach Fatigue

Cause: different in thermal expansion coefficients of silicon and the header material causing differential movement.

Effect: cracking or separation of the die or voiding of the die attach, resulting in degraded-on-resistance and/or thermal fatigue.

The susceptibility of a given die attach to thermal fatigue is normally ascertained with power cycling or unbiased temperature cycling. The best case device has the weakest internal physical stress, thus the smallest die size. The worst case device is the largest die size in the family.

2. Metal Corrosion

Cause: ingression of water into the chip surface, forming external surface leakage paths. Further, internal package stresses can promote moisture ingression allowing moisture paths to occur.

Effect: excessive drain current and eventually parametric failure.

An open circuit can result from the cathodic corrosion of the source pad when a reverse bias voltage is applied (with Vgs=0). The best case device has the smallest die with the lowest voltage rating. The worst case device has the largest die with the highest voltage rating.

Preconditioning and MSL level

Preconditioning: consisting of temperature and humidity soak followed by reflow

- MSL level 1 represents the most extreme levels of preconditioning, and hence the best resistance to moisture and other atmospheric conditions.
- If a package cannot attain MSL level 1, then it is downgraded to MSL level 2 or less.
- Low MSL levels require the package to be dry-packed (highly undesirable from a manufacturing).
- The increased temperatures of lead-free reflow profiles could lead to reduction in the MSL level of power components.
- The other qualification tests, like HTRB, HTGB,THB are carried out after the components have gone through preconditioning.

Temp cycle performance

Substrate	Pb/PbF	TC range	Mean R_{dson} shift	Normalized R_{dson} shift over >1000 cycles
FR4	Pb	-40°C/+125°C	130 μΩ	1.0
FR4	Pb-free	-40°C/+125°C	180 μΩ	1.3
FR4	Pb-free	-55°C/+150°C	380 μΩ	2.8
AlSiC/Cu IMS	Pb	-40°C/+125°C	260 μΩ	1.9
AlSiC/Cu IMS	Pb-free	-40°C/+125°C	190 μΩ	1.4
AlSiC/Cu IMS	Pb	-55°C/+150°C	270 μΩ	2.0
AlSiC/Cu IMS	Pb-free	-55°C/+150°C	310 μΩ	2.3
FR4 with C.Coat	Pb	-40°C/+125°C	300 μΩ	2.3
FR4 with underfill	Pb	-40°C/+125°C	3 μΩ	0.02

IPC/JEDEC J-STD-20 MSL Classifications

	Floor Life		Soak Requirements			
			Standard		Accelerated	
Level	**Time**	**Cond °C/%RH**	**Time (hrs)**	**Cond °C / %RH**	**Time (hrs)**	**Cond °C /%RH**
1	unlimited	<=30/85%	168 +5/-0	85/85	n/a	n/a
2	1 year	<=30/60%	168 +5/-0	85/60	n/a	n/a
2a	4 weeks	<=30/60%	696 +5/-0 **(2)**	30/60	120 +1/-0	60/60
3	168 hours	<=30/60%	192 +5/-0 **(2)**	30/60	40 +1/-0	60/60
4	72 hours	<=30/60%	96 +2/-0 **(2)**	30/60	20 +0.5/-0	60/60
5	48 hours	<=30/60%	72 +2/-0 **(2)**	30/60	15 +0.5/-0	60/60
5a	24 hours	<=30/60%	48 +2/-0 **(2)**	30/60	10 +0.5/-0	60/60
6	TOL (1)	<=30/60%	TOL	30/60	n/a	60/60

http://www.irf.com/product-info/hexfet/dfrdson.html

Standard criteria is less than 20% degradation of thermal impedance.
For DirectFET a more sensitive test is a 20% shift of R_{ds}.
20% of 3.4 milliohm (IRF6607) = 680 μΩ.
The table shows, the worst case is ½ of that level.