

**HIGH RELIABILITY,  
RADIATION HARDENED,  
LOW POWER,  
DC-DC CONVERTER**

**DH5001R803R3P**  
**50V Input, Regulated Dual Outputs**

**Description**

The DH-Series of DC-DC converters are low power radiation hardened, high reliability devices designed for hostile radiation environments such as those encountered by geostationary earth orbit satellites, deep space probes and communication systems. Features include small size, high efficiency, low weight, and a good tolerance to total ionizing dose, single event effects, and environmental stresses such as temperature extremes, mechanical shock, and vibration. All components are fully derated to meet the requirements of EEE-INST-002 and MIL-STD-1547B. Extensive documentation including worst case analysis, radiation susceptibility, thermal analysis, stress analysis, and reliability analysis are available.

The DH-Series converters have two outputs, each is independently regulated. Two versions exist; One version providing two positive outputs and one version providing one negative and one positive output. The DH-Series converters incorporate a fixed frequency flyback power converter and internal EMI filter that meets the requirements for most major satellite power buses. The converters can be remotely turned on and off via an inhibit pin. Additional inhibit pins are also included to control the outputs individually. This feature facilitates turn-on outputs sequencing if desired. Each converter is encased in a cold rolled steel hermetic package. The package measures 1.80"L x 1.40"W x 0.42"H and weighs less than 55 grams. The package utilizes rugged ceramic feed-through copper pins and is hermetically sealed using parallel seam welding. Two package options are available. Please refer to page 8 for I/O configurations.

Environmental screening includes temperature cycling, constant acceleration, fine and gross leak, and burn-in as specified by MIL-PRF-38534 for class K hybrids.

Non-flight versions of the DH-Series converters are available for system development purposes. Variations in electrical specifications and screening to meet custom requirements can be accommodated.

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**Features**

- Total Dose > 100k Rad(Si)
- SEE > 82MeV.cm<sup>2</sup>/mg
- Low Weight < 55 grams
- 26V to 55V DC Input Range
- Up to 10W Output Power
- Independently Regulated Outputs:  
+1.8V and +3.3V
- -55°C to +80°C Operating Temperature Range
- 100MΩ @ 100VDC Isolation
- Input Under-Voltage Protection
- Meets Conducted Emission Requirements of Most Major Power Buses:  
100Hz - 100kHz: 80dBμArms  
100kHz - 10MHz: Log-linear Decrease  
10MHz - 50MHz: 40dBμArms
- Short Circuit and Overload Protection
- Meets the Derating Requirements of EEE-INST-002 and MIL-STD-1547B
- On/Off Control via Converters's Inhibit Pin and Individual Output's Inhibit Pin
- High CS Damping

**Applications**

- Launch Vehicles
- Communication Systems
- Geostationary or Low Earth Orbit Satellites

## DH5001R803R3P (50V Input, Regulated Dual Outputs)

### Circuit Description

The DH-Series DC-DC converters utilize two-stage regulation with a flyback topology with a switching frequency of 250kHz for primary regulation and linear post regulation in the secondary for each of the outputs.

Output power is limited under any load fault condition to approximately 110% of rated output. An overload condition causes the converter output to behave like a constant current source with the output voltage dropping below nominal. The converter will resume normal operation when the load current is reduced below the current limit point.

This protects the converter from both overload and short circuit conditions. There are no latching elements to eliminate the possibility of falsely triggering the protection circuits during single event radiation exposure.

An under-voltage protection circuit prohibits the converter from operating when the line voltage is too low for safe operation. The converter will not start until the line voltage rises to approximately 24V.

An inhibit pin is provided to control converter operation. This inhibit pin is intended for operation with an open collector transistor drive or a relay closure to the input return. The pin may be left open for normal operation and has a nominal open circuit voltage of 7V. Also provided are the individual output on/off control pins (Pin 10-Output 1 Inhibit and Pin 9-Output 2 Inhibit).

### Design Methodology

The DH-Series is developed using a proven conservative design methodology, which includes selecting radiation tolerant and established reliability components and fully derating to the requirements of EEE-INST-002 and MIL-STD-1547B. Heavy derating of the radiation-hardened power MOSFET virtually eliminates the possibility of SEGR and SEB.

**Specifications**

Absolute Maximum Ratings		Recommended Operating Conditions	
Input voltage range	-0.5Vdc to +80Vdc	Input voltage range (Note 13)	26Vdc to 55Vdc
Output power	Internally limited	Output power	0 to Max. Rated
Lead temperature	+300°C for 10sec	Operating temperature	-55°C to +115°C
Operating case temperature (Note 12)	-55°C to +125°C	Operating temperature, derated (Note 13)	-55°C to +80°C
Storage temperature	-55°C to +135°C		

**Electrical Performance Characteristics**

Parameter	Group A Subgroup	Conditions -55°C ≤ T <sub>C</sub> ≤ +85°C V <sub>IN</sub> = 50V DC ± 5%, C <sub>L</sub> = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
Input Voltage			26	50	55	V
Output voltage (V <sub>OUT</sub> ) (Out 1/Out 2)	1	I <sub>OUT</sub> = 100% rated load				V
1.8V	1					
3.3V	1					
(Out 1/Out 2)						
1.8V	2,3		1.746	1.800	1.854	V
3.3V	2,3		3.200	3.300	3.399	
Output power (P <sub>OUT</sub> )		V <sub>IN</sub> = 26, 50, 55V, Notes 2,11 Either Output				W
1.8V	1,2,3					
3.3V						
Output current (I <sub>OUT</sub> )		V <sub>IN</sub> = 26, 50, 55V, Notes 2, 11 Either Output				A
1.8V	1,2,3					
3.3V	1,2,3					
Line regulation (VR <sub>LINE</sub> )	1,2,3	V <sub>IN</sub> = 26, 50, 55V I <sub>OUT</sub> = 0%, 50%, 100% rated	-0.2		0.2	%
Load regulation (VR <sub>LOAD</sub> )	1,2,3	I <sub>OUT</sub> = 0%, 50%, 100% rated V <sub>IN</sub> = 26, 50, 55V	-0.5		1.5	%
Cross regulation (VR <sub>CROSS</sub> )	1,2,3	V <sub>IN</sub> = 26, 50, 55V, Note 1			5.0	mV
Input current (I <sub>IN</sub> )		I <sub>OUT</sub> = 0, Pin 6 open Pin 6 connected to Pin 2				mA
	1,2,3					
Output ripple (V <sub>RIP</sub> ) Each Output		V <sub>IN</sub> = 26, 50, 55V I <sub>OUT</sub> = 100% rated load Note 3				mV p-p
1.8V	1,2,3					
3.3V						
Output ripple @ switch frequency		V <sub>IN</sub> = 26, 50, 55V I <sub>OUT</sub> = 100% rated load, Note 1				mV rms
1.8V	1,2,3					
3.3V						

For Notes to Electrical Performance Characteristic Table, refer to page 5

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**Electrical Performance Characteristics (continued)**

Parameter	Group A Subgroup	Conditions -55°C ≤ T <sub>C</sub> ≤ +85°C V <sub>IN</sub> = 50V DC ± 5%, C <sub>L</sub> = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
Efficiency (E <sub>FF</sub> )	1,2,3	I <sub>OUT</sub> = 100% rated load	45	49		%
Inhibit Input Open circuit voltage Drive current (sink) Voltage range		Note 1			7.0 600 50	V μA V
Current Limit Point Each output 1.8V 3.3V	1,2,3	V <sub>OUT</sub> = 90% of Nominal Note 10	105 105		145 145	%
Power dissipation load fault (P <sub>D</sub> )	1,2,3	Short Circuit, Overload, Note 5			24	W
Output response to step load changes (V <sub>TLD</sub> ) 1.8V 3.3V	4,5,6	Half Load to/ from Full Load, Note 6	-15 -15		15 15	mV pk
Recovery time, step load changes (T <sub>TLD</sub> )	4,5,6	Half Load to/from Full Load, Notes 6, 7			500	μs
Recovery time, step line changes (T <sub>TLN</sub> )	4,5,6	26V to/from 55V I <sub>OUT</sub> = 100% rated load, Notes 1, 7, 8			100	μs
Capacitive Load (C <sub>L</sub> )	1	I <sub>OUT</sub> = 100% rated load No effect on DC performance Each Output, Notes 1, 4			220	μF
Turn-on Response Overshoot (V <sub>OS</sub> ) Turn-on Delay (T <sub>DLY</sub> )	4,5,6	10% Load, Full Load Note 9			25 10	mV ms
Enable Input (Inhibit) Open circuit voltage Drive current (sink) Voltage range	1,2,3	Note 1	0		10 100 0.4	V μA V

For Notes to Electrical Performance Characteristic Table, refer to page 5

**Electrical Performance Characteristics (continued)**

Parameter	Group A Subgroup	Conditions $-55^{\circ}\text{C} \leq T_C \leq +85^{\circ}\text{C}$ $V_{IN} = 50\text{V DC} \pm 5\%$ , $C_L = 0$ unless otherwise specified	Limits			Unit
			Min	Nom	Max	
EMC conducted susceptibility (Line rejection)	1	$I_{OUT} = 100\%$ rated load Primary power sine wave injection of 2Vp-p, 100Hz to 50MHz, Note 1	80	90		dB
Electromagnetic Interference (EMI), conducted emission (CE)	1	$I_{OUT} = 100\%$ rated load, Note 1	Limits per Figure 1			
Isolation	1	Input to Output or Any Pin to Case except pin 3, test @ 100 VDC	100			MΩ
Device Weight					55	g
MTBF		MIL-HDBK-217F2, SF, 35°C	100.000			Hours

**Notes: Specification and Electrical Performance Characteristics**

- Parameter is tested as part of design characterization or after design changes. Thereafter, parameter shall be guaranteed to the limits specified.
- Parameter verified during line and load regulation tests.
- Guaranteed for a D.C. to 20MHz bandwidth. Tested using a 20KHz to 10MHz bandwidth.
- Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit may interfere with the proper operation of the converter's overload protection, causing erratic behavior during turn-on.
- Overload power dissipation is defined as the device power dissipation with the load set such that both outputs are in a short circuit mode.
- Load step transition time  $\leq 10 \mu\text{sec}$ .
- Recovery time is measured from the initiation of the transient to where  $V_{OUT}$  has returned to within  $\pm 1\%$  of its steady state value.
- Line step transition time  $\leq 100 \mu\text{sec}$ .
- Turn-on delay time from either a step application of input power or a logic low to a logic high transition on the inhibit pin (pin 6) to the point where  $V_{OUT} = 90\%$  of nominal.
- Current limit point expressed as a percentage of full rated load current.
- For models with two positive outputs the envelope specification for the design is that each output voltage is limited to the range 1V to 5V.
- Although operation at temperatures between  $+85^{\circ}\text{C}$  and  $+125^{\circ}\text{C}$  is guaranteed, no parameter limits are specified.
- Meets the derating requirements of EEE-INST-002 and MIL-STD-1547B – except for ceramic capacitors with voltage stress below 10V will minimum be rated at 50V and a minimum load of 20mA on each output.

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**Device Screening**

Test / Inspection	Method	/EM Suffix	Flight (No Suffix)
Element Evaluation	MIL-STD-38534 Class K equivalent with SEM	N/A	X
Nondestructive Bond Pull	MIL-STD-883, Method 2023	N/A	X
Internal Visual	MIL-STD-883, Method 2017	N/A	X
Temperature Cycling	MIL-STD-883, Method 1010	N/A	Condition C
Constant Acceleration	MIL-STD-883, Method 2001, Y1 Axis	N/A	3000 G's
PIND	MIL-STD-883, Method 2020	N/A	A
Burn-in (2 x 220 hours)	MIL-STD-883, Method 1015	48 Hours @ 115°C	440 Hours @ 115°C
Final Electrical (Group A)	In accordance with device specification	X	X
Seal	MIL-STD-883, Method 1014	Condition A	
Fine Leak			A1
Gross Leak			C
Radiographic	MIL-STD-883, Method 2012	N/A	N/A
External Visual	MIL-STD-883, Method 2009	Note 1	X

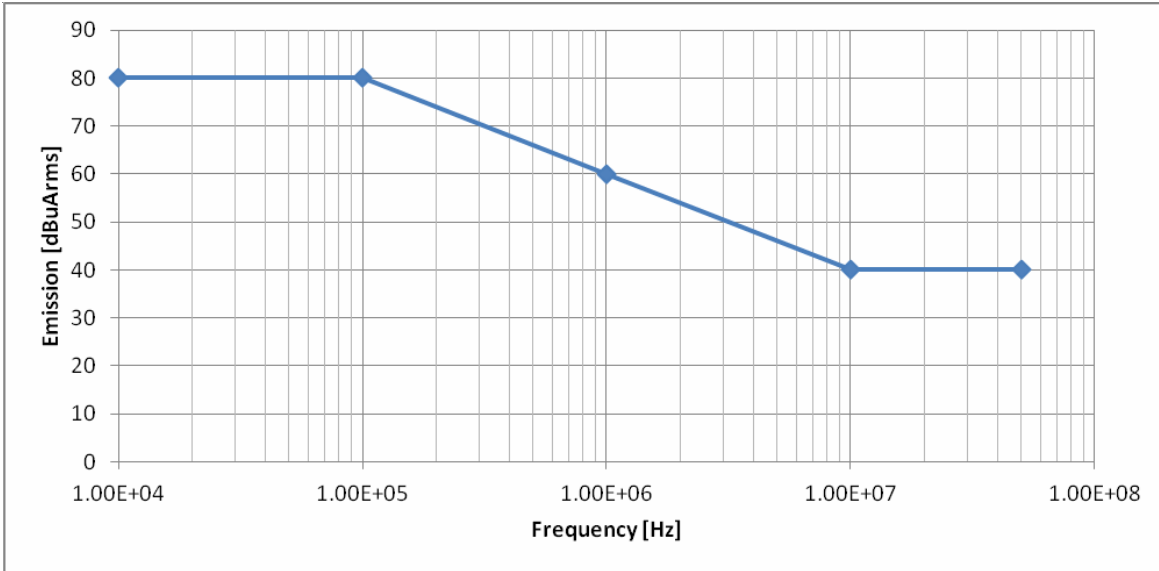
Note 1: Best commercial practice.

**Radiation Performance Characteristics**

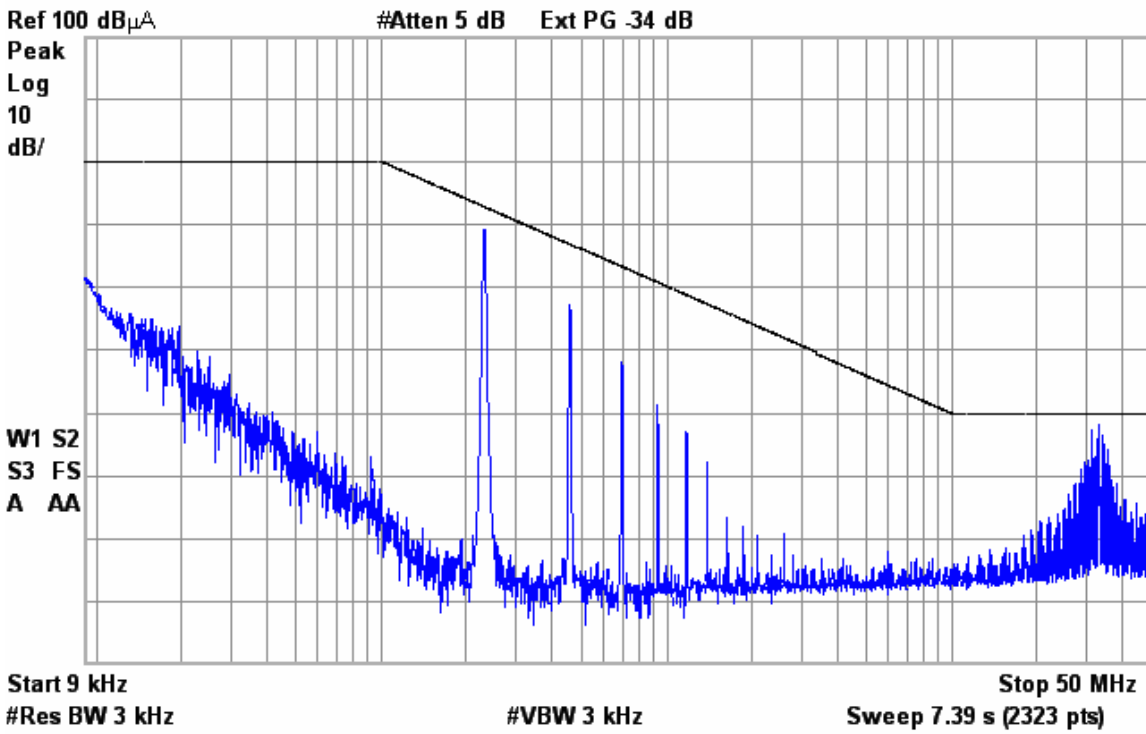
Test	Conditions	Min	Unit
Total Ionizing Dose (Gamma)	MIL-STD-883, Method 1019.5 Operating bias applied during exposure, Full Rated Load, $V_{IN} = 50V$	100	KRads (Si)
Single Event Effects * SEU, SEL, SEGR, SEB	Heavy Ions (LET) Operating bias applied during exposure, Full Rated Load, $V_{IN} = 26, 50, 55V$	82	MeV·cm <sup>2</sup> /mg

\* Test performed at TAMU

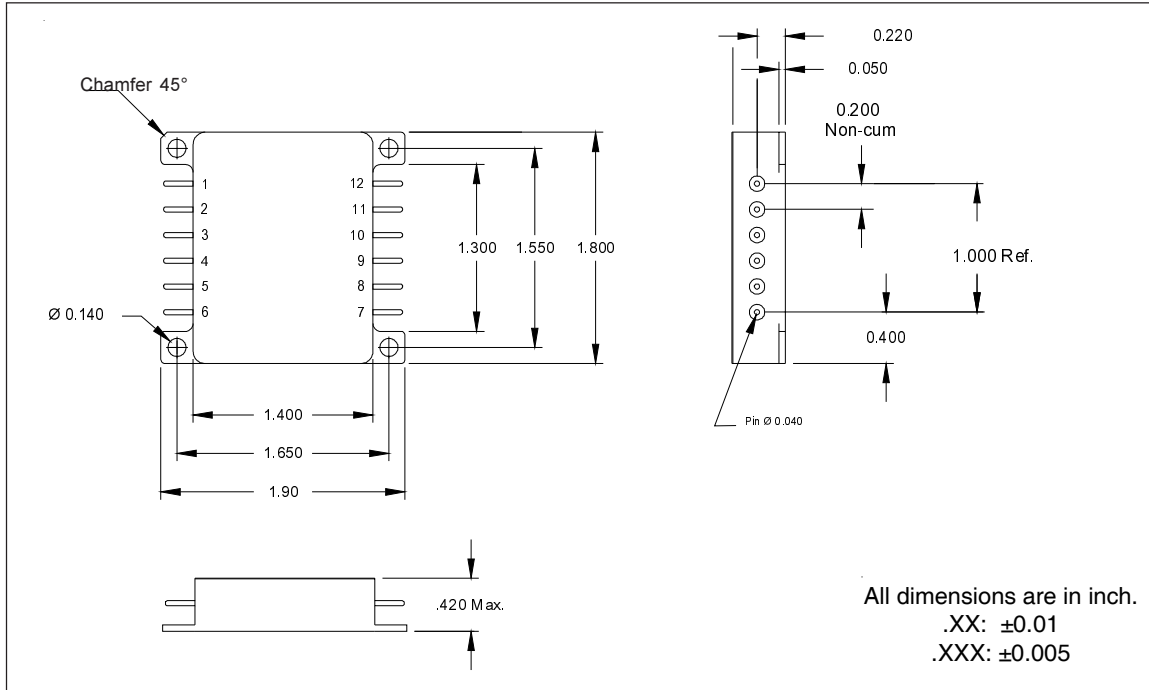
**Fig. 1 - EMI Conducted Emission Performance Limit**



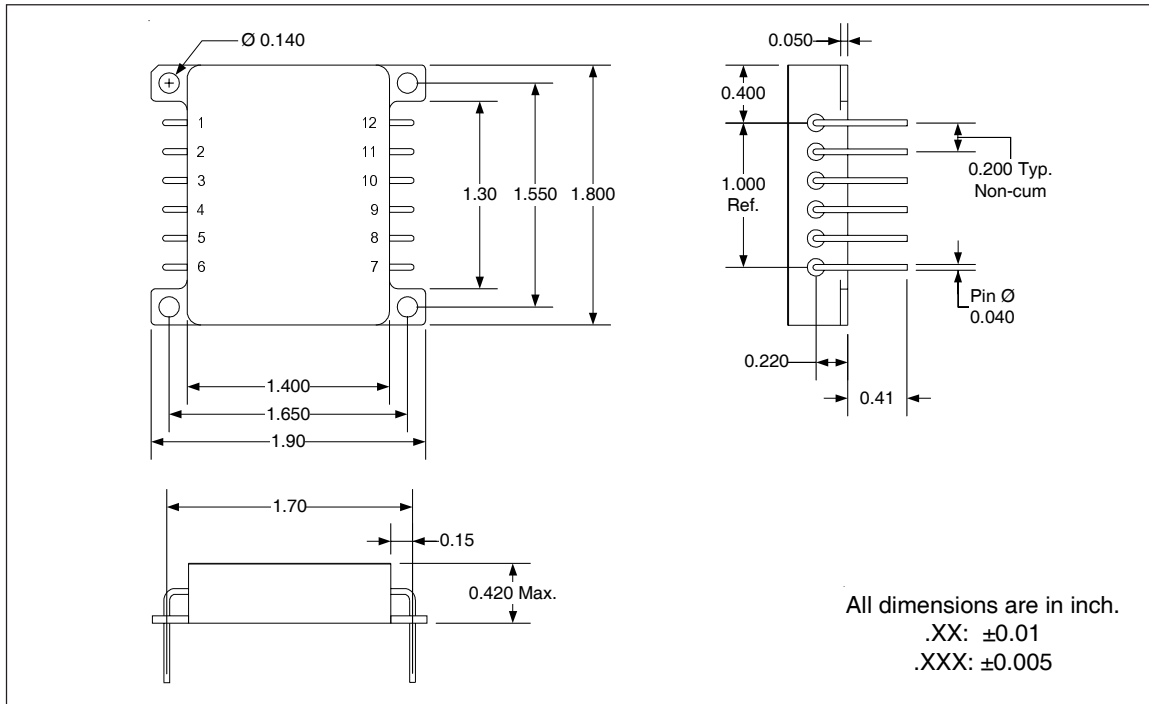
**Fig. 2 - A Typical input EMI Conducted Emission Performance**



**Mechanical Outline - Option A (Straight Pins)**

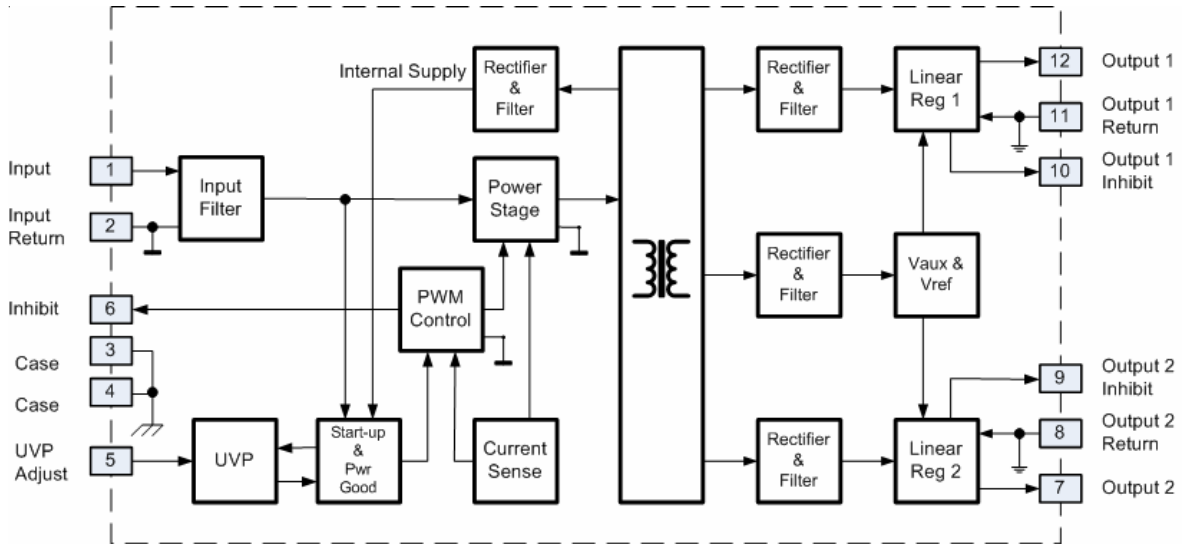


**Mechanical Outline - Option B (Down Pins)**





**Block Diagram**



Note: Pins 8 and 11 are internally connected. Pins 3 and 4 are tied to case and are isolated from both primary and secondary circuit grounds.

**Pin Designation**

Pin #	Name
1	Input
2	Input Return
3	Case
4	Case
5	UVP Adjust
6	Inhibit
7	Output 2
8	Output 2 Return
9	Output 2 Inhibit
10	Output 1 Inhibit
11	Output 1 Return
12	Output 1

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**Part Numbering**

