

**ADVANCED ANALOG
HYBRID - HIGH RELIABILITY
RADIATION HARDENED DC/DC CONVERTER**

ART28XXT SERIES

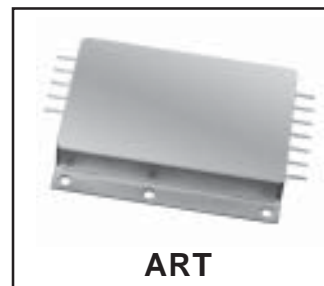
28V Input, Three Output

Description

The ART Series of three output DC/DC converters are designed specifically for use in the hostile radiation environments characteristic of space and weapon systems. The extremely high level of radiation tolerance inherent in the ART design is the culmination of extensive research, thorough analysis and testing and of careful component specification. Many of the best circuit design features characterizing the Advanced Analog standard product line were adapted for incorporation into the ART topology. Capable of uniformly high performance over long term exposures in radiation intense environments, this series sets the standard for distributed power systems demanding high performance and reliability.

The ART converters are hermetically sealed in a rugged, low profile package utilizing copper core pins to minimize resistive DC losses. Long-term hermeticity is assured through use of parallel seam welded lid attachment along with Advanced Analog's rugged ceramic pin-to-package seal. Axial orientation of the leads facilitates preferred bulkhead mounting to the principal heat-dissipating surface.

Manufactured in a facility fully qualified to MIL-PRF-38534, these converters are fabricated utilizing DSSC qualified processes, and are fully compliant to Class H while being fully processed to the requirements of Class K. Complete PI & CI testing has been completed including Group C life test. Variations in electrical, mechanical and screening specifications can be accommodated. Contact Advanced Analog for special requirements.



Features

- Total Dose > 100KRad (Si), 2:1margin
- SEE hard to LET = 83 Mev.cm² /mg
- Designed to MIL-PRF-38534 for Class K
- Derated per MIL-STD-975 & MIL-STD-1547
- Output Power Range 3 to 30 Watts
- 19 to 50 Volt Input Range
- Input Undervoltage Lockout
- High Electrical Efficiency > 80%
- Full Performance from -55°C to +125°C
- Continuous Short Circuit Protection
- 12.8 W / in³ Output Power Density
- True Hermetic Package
- External Inhibit Port
- Externally Synchronizable
- Fault Tolerant Design
- 5V, ±12 or ±15 Volts Outputs Available

SPECIFICATIONS

Absolute Maximum/Minimum Ratings Note 1 Recommended Operating Conditions Note 2

| | | | |
|------------------------|--------------------------------------|-----------------------|---|
| Input Voltage | -0.5V to 80V | Input Voltage Range | 19V to 60V |
| Minimum Output Current | 5% maximum rated current, any output | Input Voltage Range | 19V to 50V for full derating to MIL-STD-975 |
| Soldering Temperature | 300°C for 10 seconds | Output Power Range | 3W to 30 W |
| Storage Temperature | -65°C to +135°C | Operating Temperature | -55°C to +125°C |
| | | | -55°C to +85°C for full derating to MIL-STD-975 |

Electrical Performance $-55^{\circ}\text{C} \leq T_{\text{CASE}} \leq +125^{\circ}\text{C}$, $V_{\text{IN}}=28\text{V}$, $C_{\text{L}}=0$ unless otherwise specified.

| Parameter | Symbol | Conditions | Min | Max | Units |
|------------------------------|---------------------|---|------------------------------------|------------------------------------|-------------------------|
| Output voltage accuracy | V_{OUT} | $I_{\text{OUT}} = 1.5\text{A dc}$, $T_{\text{C}} = +25^{\circ}\text{C}$ (main) $I_{\text{OUT}} = \pm 250\text{mA dc}$, $T_{\text{C}} = +25^{\circ}\text{C}$ ART2812(dual) $I_{\text{OUT}} = \pm 250\text{mA dc}$, $T_{\text{C}} = +25^{\circ}\text{C}$ ART2815(dual) | 4.95 ± 11.50 ± 14.50 | 5.05 ± 12.50 ± 15.15 | Vdc |
| Output power Note 5 | P_{OUT} | $19\text{ Vdc} < V_{\text{IN}} < 50\text{Vdc}$ | 3 | 30 | W |
| Output current Note 5 | I_{OUT} | $19\text{ Vdc} < V_{\text{IN}} < 50\text{Vdc}$ (main) (dual) | 150 75 | 3000 750 | mAdc |
| Line regulation Note 3 | VR_{LINE} | $150\text{ mA dc} < I_{\text{OUT}} < 3000\text{ mA dc}$ (main) $19\text{ Vdc} < V_{\text{IN}} < 50\text{Vdc}$ $\pm 75\text{ mA dc} < I_{\text{OUT}} < \pm 750\text{ mA dc}$ (dual) | -15 -60 | +15 +60 | mV |
| Load regulation Note 4 | VR_{LOAD} | $150\text{ mA dc} < I_{\text{OUT}} < 3000\text{ mA dc}$ (main) $19\text{ Vdc} < V_{\text{IN}} < 50\text{Vdc}$ $\pm 75\text{ mA dc} < I_{\text{OUT}} < \pm 750\text{ mA dc}$ (dual) | -180 -300 | +180 +300 | mV |
| Cross regulation Note 8 | VR_{CROSS} | (main) $19\text{ Vdc} < V_{\text{IN}} < 50\text{Vdc}$ (dual) | -10 -500 | +10 +500 | mV |
| Total regulation | VR | All conditions of Line, Load, Cross Regulation, Aging, Temperature and Radiation (main) ART2812(dual) ART2815(dual) | 4.8 ± 11.1 ± 13.9 | 5.2 ± 12.9 ± 16.0 | V |
| Input current | I_{IN} | $I_{\text{OUT}} = \text{minimum rated}$, Pin 3 open Pin 3 shorted to pin 2 (disabled) | | 250 8 | mA |
| Output ripple voltage Note 6 | V_{RIP} | $19\text{ Vdc} < V_{\text{IN}} < 50\text{Vdc}$ $I_{\text{OUT}} = 3000\text{ mA dc}$ (main), $\pm 500\text{ mA dc}$ (dual) | | 100 | mV_{pp} |
| Input ripple current Note 6 | I_{RIP} | $19\text{ Vdc} < V_{\text{IN}} < 50\text{Vdc}$ $I_{\text{OUT}} = 3000\text{ mA dc}$ (main), $\pm 500\text{ mA dc}$ (dual) | | 150 | mA_{pp} |
| Switching frequency | F_{S} | Synchronization input open. (pin 6) | 225 | 275 | KHz |
| Efficiency | Eff | $I_{\text{OUT}} = 3000\text{ mA dc}$ (main), $\pm 500\text{ mA dc}$ (dual) | 80 | | % |

For Notes to SPECIFICATIONS, refer to page 3

Electrical Performance (Continued)

| Parameter | Symbol | Conditions | Min | Max | Units |
|--|------------------|--|--------------------------------|---------------------------|----------------------------------|
| Enable Input open circuit voltage drive current (sink) voltage range | | | 3.0 -0.5 | 5.0 0.1 50.0 | V mA V |
| Synchronization Input frequency range pulse high level pulse low level pulse rise time pulse duty cycle | | External clock signal on Sync. input (pin 4) | 225 4.5 -0.5 40 20 | 310 10.0 0.25 80 | KHz V V V/ μ S % |
| Power dissipation, load fault | P _D | Short circuit, any output | | 7.5 | W |
| Output response to step load changes <i>Notes 7, 11</i> | V _{TLD} | 10% Load to/from 50% load 50% Load to/from 100% load | -200 -200 | 200 200 | mV _{PK} |
| Recovery time from step load changes <i>Notes 11, 12</i> | T _{TLD} | 10% Load to/from 50% load 50% Load to/from 100% load | | 200 200 | μ S |
| Output response to step line changes <i>Notes 10, 11</i> | V _{TLN} | I _{OUT} = 3000 mAdc (main) V _{IN} = 19 V to/from 50 V I _{OUT} = \pm 500 mAdc (dual) | -350 -1050 | 350 1050 | mV _{PK} |
| Recovery time from step line changes <i>Notes 10, 11, 13</i> | T _{TLN} | I _{OUT} = 3000 mAdc (main) V _{IN} = 19 V to/from 50 V I _{OUT} = \pm 500 mAdc (dual) | | 500 500 | μ S |
| Turn on overshoot | V _{OS} | I _{OUT} = minimum and full rated (main) (dual) | | 500 1500 | mV |
| Turn on delay <i>Note 14</i> | T _{DLY} | I _{OUT} = minimum and full rated | 5 | 20 | mS |
| Capacitive load <i>Notes 9, 10</i> | CL | No effect on DC performance (main) (dual) | | 500 100 | μ F |
| Isolation | ISO | 500VDC Input to Output or any pin to case (except pin 12) | 100 | | M Ω |

Notes to SPECIFICATIONS

1. Operation outside absolute maximum/minimum limits may cause permanent damage to the device. Extended operation at the limits may permanently degrade performance and affect reliability.
2. Device performance specified in Electrical Performance table is guaranteed when operated within recommended limits. Operation outside recommended limits is not specified.
3. Parameter measured from 28V to 19 V or to 50V while loads remain fixed.
4. Parameter measured from nominal to minimum or maximum load conditions while line remains fixed.
5. Up to 750 mA is available from the dual outputs provided the total output power does not exceed 30W.
6. Guaranteed for a bandwidth of DC to 20MHz. Tested using a 20KHz to 2MHz bandwidth.
7. Load current is stepped for output under test while other outputs are fixed at half rated load.
8. Load current is fixed for output under test while other output loads are varied for any combination of minimum to maximum.
9. A capacitive load of any value from 0 to the specified maximum is permitted without compromise to DC performance. A capacitive load in excess of the maximum limit may interfere with the proper operation of the converter's short circuit protection, causing erratic behavior during turn on.
10. Parameter is tested as part of design characterization or after design or process changes. Thereafter, parameters shall be guaranteed to the limits specified in the table.
11. Load transient rate of change, di/dt \leq 2 A/ μ Sec.
12. Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within \pm 1% of its steady state value.
13. Line transient rate of change, dv/dt \leq 50 V/ μ Sec.
14. Turn on delay time is for either a step application of input power or a logical low to high transition on the enable pin (pin 3) while power is present at the input.

ART28XXT Series

International
IRF Rectifier

Group A Tests $V_{IN} = 28\text{Volts}$, $C_L = 0$ unless otherwise specified.

| Test | Symbol | Conditions unless otherwise specified | Group A Subgroups | Min | Max | Units |
|--|-----------|---|-------------------|-------------|-------------|-------------------|
| Output voltage accuracy | V_{OUT} | $I_{OUT} = 1.5 \text{ Adc}$ (main) | 1, 2, 3 | 4.95 | 5.05 | V |
| | | $I_{OUT} = \pm 250\text{mAdc}$ ART2812(dual) | 1, 2, 3 | ± 11.70 | ± 12.30 | |
| | | $I_{OUT} = \pm 250\text{mAdc}$ ART2815(dual) | 1, 2, 3 | ± 14.50 | ± 15.15 | |
| Output power <i>Note 1</i> | P_{OUT} | $V_{IN} = 19 \text{ V}, 28\text{V}, 50 \text{ V}$ | 1, 2, 3 | 3 | 30 | W |
| Output current <i>Note 1</i> | I_{OUT} | (main) | 1, 2, 3 | 150 | 3000 | mA |
| | | (dual) | 1, 2, 3 | 75 | 500 | |
| Output regulation <i>Note 4</i> | VR | $I_{OUT} = 150, 1500, 3000\text{mAdc}$ (main) | 1, 2, 3 | 4.8 | 5.2 | V |
| | | $V_{IN} = 19 \text{ V}, 28\text{V}, 50 \text{ V}$ | | | | |
| | | $I_{OUT} = \pm 75, \pm 310, \pm 625\text{mAdc}$ 2812(dual) | 1, 2, 3 | ± 11.1 | ± 12.9 | |
| | | $I_{OUT} = \pm 75, \pm 250, \pm 500\text{mAdc}$ 2815(dual) | 1, 2, 3 | ± 14.0 | ± 15.8 | |
| Input current | I_{IN} | $I_{OUT} = \text{minimum rated, Pin 3 open}$ | 1, 2, 3 | | 250 | mA |
| | | Pin 3 shorted to pin 2 (disabled) | 1, 2, 3 | | 8 | |
| Output ripple <i>Note 2</i> | V_{RIP} | $V_{IN} = 19 \text{ V}, 28\text{V}, 50 \text{ V}$ $I_{OUT} = 3000\text{mA main, } \pm 500\text{mA dual}$ | 1, 2, 3 | | 100 | $\text{mV}_{p,p}$ |
| Input ripple <i>Note 2</i> | I_{RIP} | $V_{IN} = 19 \text{ V}, 28\text{V}, 50 \text{ V}$ $I_{OUT} = 3000\text{mA main, } \pm 500\text{mA dual}$ | 1, 2, 3 | | 150 | $\text{mA}_{p,p}$ |
| Switching frequency | F_S | Synchronization pin (pin 6) open | 4, 5, 6 | 225 | 275 | KHz |
| Efficiency | Eff | $I_{OUT} = 800\text{mA main, } \pm 500\text{mA dual}$ | 1 2, 3 | 80 78 | | % |
| Power dissipation, load fault | P_D | Short circuit, any output | 1, 2, 3 | | 7.5 | W |
| Output response to step load changes <i>Notes 3, 5</i> | V_{TL} | 10% Load to/from 50% load | 4, 5, 6 | -200 | 200 | mV_{pk} |
| | | 50% Load to/from 100% load | 4, 5, 6 | -200 | 200 | |
| Recovery time from step load changes <i>Notes 5, 6</i> | T_{TL} | 10% Load to/from 50% load | 4, 5, 6 | | 200 | μS |
| | | 50% Load to/from 100% load | 4, 5, 6 | | 200 | |
| Turn on overshoot | V_{OS} | (main) | 4, 5, 6 | | 500 | mV |
| | | $I_{OUT} = \text{minimum and full rated}$ (dual) | 4, 5, 6 | | 1500 | |
| Turn on delay <i>Note 7</i> | T_{DLY} | $I_{OUT} = \text{minimum and full rated}$ | 4, 5, 6 | 5 | 20 | mS |
| Isolation | ISO | 500VDC Input to output or any pin to case (except pin 12) | 1 | 100 | | $\text{M}\Omega$ |

Notes to Group A Test Table

- Parameter verified during dynamic load regulation tests.
- Guaranteed for DC to 20 MHz bandwidth. Test conducted using a 20KHz to 2MHz bandwidth.
- Load current is stepped for output under test while other outputs are fixed at half rated load.
- Each output is measured for all combinations of line and load. Only the minimum and maximum readings for each output are recorded.
- Load step transition time $\geq 10\mu\text{S}$.
- Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within $\pm 1\%$ of its steady state value.
- Turn on delay time is tested by application of a logical low to high transition on the enable pin (pin 3) with power present at the input.
- Subgroups 1 and 4 are performed at $+25^\circ\text{C}$, subgroups 2 and 5 at -55°C and subgroups 3 and 6 at $+125^\circ\text{C}$.

Radiation Performance

The radiation tolerance characteristics inherent in the ART28XXT converter are the direct result of a carefully planned ground-up design program with specific radiation design goals. After identification of the general circuit topology, a primary task of the design effort was selection of appropriate elements from the list of devices for which extensive radiation effects data was available. By imposing sufficiently large margins on those electrical parameters subject to the degrading effects of radiation, designers were able to select appropriate elements for incorporation into the circuit. Known radiation data was utilized for input to PSPICE and RadSPICE in the generation of circuit performance verification analyses. Thus, electrical performance capability under all environmental conditions including radiation was well understood before first application of power to the inputs.

A principal design goal was a converter topology that, because of large design margins, had radiation performance essentially independent of normal elemental lot radiation

performance variations. In the few instances where such margins were not assured, element lots were selected from which die were fabricated (and characterized) as radiation hard devices so that realization of the design goals could be assured.

Completion of first article fabrication, screening and standard environmental testing was followed by radiation testing to confirm design goals. All design goals were met handily and in most cases exceeded by large margin. These test samples were built with elements that, with the foregoing exceptions, were *not* screened for radiation characteristics. Additional radiation tests on subsequent ART28XXT manufacturing lots provide continued confirmation of the soundness of the design goals as well as justification for the element selection criteria.

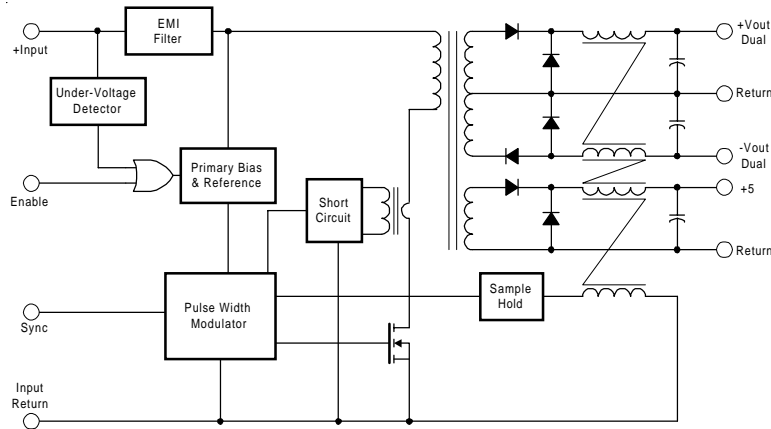
The following table specifies guaranteed minimum radiation exposure levels tolerated while maintaining specification limits.

Radiation Specification $T_{case} = 25^{\circ}C$

| Test | Conditions | Min | Typ | Max | Unit |
|---|--|-------------|-----|-----|-----------------------------|
| Total Ionizing Dose (2:1 Margin) | MIL-STD-883, Method 1019.4 Operating bias applied during exposure | 100 | 500 | | KRads (Si) |
| Dose Rate Temporary Saturation Survival | MIL-STD-883, Method 1021 | 1E8 1E11 | | | Rads (Si)/sec |
| Neutron Fluence | MIL-STD-883, Method 1017.2 | 3E12 | | | Neutron /cm ² |
| Heavy Ions (Single event effects) | BNL Tandem Van de Graaff Generator | 83 | | | MeV• cm ² /mg |

ART28XXT Circuit Description

Figure I. ART Block Diagram



Circuit Description and Application Information

The ART28XXT series of converters have been designed using a single ended forward switched mode converter topology. (refer to Figure I.) Single ended topologies enjoy some advantage in radiation hardened designs in that they eliminate the possibility of simultaneous turn on of both switching elements during a radiation induced upset; in addition, single ended topologies are not subject to transformer saturation problems often associated with double ended implementations.

The design incorporates an LC input filter to attenuate input ripple current. A low overhead linear bias regulator is used to provide bias voltage for the converter primary control logic and a stable, well regulated reference for the error amplifier. Output control is realized using a wide band discrete pulse width modulator control circuit incorporating a unique non-linear ramp generator circuit. This circuit helps stabilize loop gain over variations in line voltage for superior output transient response. Nominal conversion frequency has been selected as 250 KHz to maximize efficiency and minimize magnetic element size.

Output voltages are sensed using a coupled inductor and a patented magnetic feedback circuit. This circuit is relatively insensitive to variations in temperature, aging, radiation and manufacturing tolerances making it particularly well suited to radiation hardened designs. The control logic has been designed to use only radiation tolerant components, and all current paths are limited with series resistance to limit photo currents.

Other key circuit design features include short circuit protection, undervoltage lockout and an external synchronization port permitting operation at an externally set clock rate.

Operating Guidelines

The circuit topology used for regulating output voltages in the ART28XXT series of converters was selected for a number of reasons. Significant among these is the ability to simultaneously provide adequate regulation to each output voltage while maintaining modest circuit complexity. These attributes were fundamental in retaining the high reliability and insensitivity to radiation that characterizes device performance. Use of this topology dictates that the user maintain a minimum load on each output as specified in the electrical tables. Attempts to operate any output without a load will result in peak charging to a voltage level well above the specified voltage regulation limits, potentially in excess of ratings, and should be avoided. In most practical applications, this lower bound on the load range does not present a serious constraint. Output loads that are lighter than the specified minimums will result in regulation performance exceeding the limits presented in the specification tables. Regulation curves illustrating representative performance characteristics are shown in Figures VII, VIII and IX.

Thermal Considerations

The ART series of converters is capable of providing relatively high output power from a package of modest volume. The power density exhibited by these devices is obtained by combining high circuit efficiency with effective methods of heat removal from the die junctions. Good design practices have effectively addressed this requirement inside the device. However when operating at maximum loads, significant heat generated at the die junctions must be carried away by conduction from the base. To maintain case temperature at or below the specified maximum of 125°C, this heat can be transferred by attachment

to an appropriate heat dissipater held in intimate contact with the converter base-plate.

Effectiveness of this heat transfer is dependent on the intimacy of the baseplate-heatsink interface. It is therefore suggested that a heat transferring medium possessing good thermal conductivity is inserted between the baseplate and heatsink. A material utilized at the factory during testing and burn-in processes is sold under the trade name of Sil-Pad[®] 400¹. This particular product is an insulator but electrically conductive versions are also available. Use of these materials assures optimum surface contact with the heat dissipater by compensating for minor surface variations. While other available types of heat conducting materials and thermal compounds provide similar effectiveness, these alternatives are often less convenient and are frequently messy to use.

A conservative aid to estimating the total heat sink surface area ($A_{\text{HEAT SINK}}$) required to set the maximum case temperature rise (ΔT) above ambient temperature is given by the following expression:

$$A_{\text{HEAT SINK}} \approx \left\{ \frac{\Delta T}{80P^{0.85}} \right\}^{-1.43} - 5.94$$

where

ΔT = Case temperature rise above ambient

$$P = \text{Device dissipation in Watts} = P_{\text{out}} \left\{ \frac{1}{\text{Eff}} - 1 \right\}$$

As an example, assume that it is desired to maintain the case temperature of an ART2815T at +65°C or less while operating in an open area whose ambient temperature does not exceed +35°C; then

$$\Delta T = 65 - 35 = 35^\circ\text{C}$$

From the Specification Table, the worst case full load efficiency for this device is 80%; therefore the maximum power dissipation at full load is given by

$$P = 30 \cdot \left\{ \frac{1}{.80} - 1 \right\} = 30 \cdot (0.25) = 7.5\text{W}$$

and the required heat sink area is

$$A_{\text{HEAT SINK}} = \left\{ \frac{35}{80 \cdot 7.5^{0.85}} \right\}^{-1.43} - 5.94 = 31.8 \text{ in}^2$$

¹Sil-Pad is a registered Trade Mark of Bergquist, Minneapolis, MN

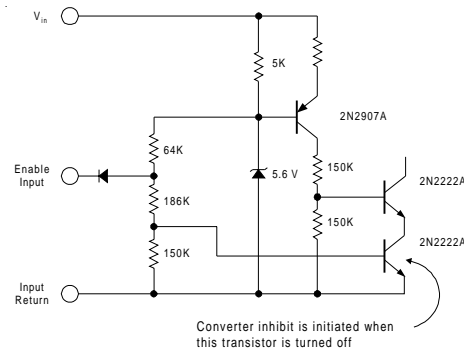
Thus, a total heat sink surface area (including fins, if any) of approximately 32 in² in this example, would limit case rise to 35°C above ambient. A flat aluminum plate, 0.25" thick and of approximate dimension 4" by 4" (16 in² per side) would suffice for this application in a still air environment. Note that to meet the criteria, both sides of the plate require unrestricted exposure to the ambient air.

Inhibiting Converter Output

As an alternative to application and removal of the DC voltage to the input, the user can control the converter output by providing an input referenced, TTL compatible, logic signal to the enable pin 3. This port is internally pulled "high" so that when not used, an open connection on the pin permits normal converter operation. When inhibited outputs are desired, a logical "low" on this port will shut the converter down. An open collector device capable of sinking at least 100 μA connected to enable pin 3 will work well in this application.

A benefit of utilization of the enable input is that following initial charge of the input capacitor, subsequent turn-on commands will induce no uncontrolled current inrush.

Figure II. Enable Input Equivalent Circuit

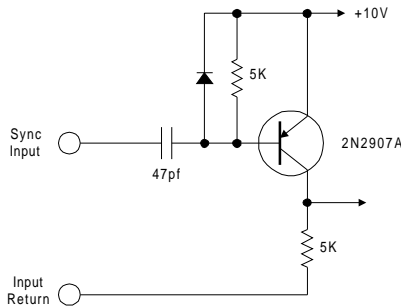


Synchronization

When using multiple converters, system requirements may dictate operating several converters at a common system frequency. To accommodate this requirement, the ART28XXT type converter provides a synchronization input port (pin 4). Circuit topology is as illustrated in Figure III.

The sync input port permits synchronization of an ART converter to any compatible external frequency source operating in the band of 225 to 310 KHz. The synchronization input is edge triggered with synchronization initiated on the negative transition. This input signal should be a negative going pulse referenced to the input return and have a 20% to 80% duty cycle. Compatibility requires the negative transition time to be less than 100 ns with a minimum pulse amplitude of +4.25 volts referred to the input return. In the event of failure of an external synchronization source, the converter will revert to its own internally set frequency. When external synchronization is not desired, the sync in port may be left open (unconnected) permitting the converter to operate at its' own internally set frequency.

Figure III. Synchronization Input Equivalent Circuit



Output Short Circuit Protection

Protection against accidental short circuits on any output is provided in the ART28XXT converters. This protection is implemented by sensing primary switching current and, when an over-current condition is detected, switching action is terminated and a restart cycle is initiated. If the short circuit condition has not been cleared by the time the restart cycle has completed, another restart cycle is initiated. The sequence will repeat until the short circuit condition is cleared at which time the converter will resume normal operation. The effect is that during a shorted condition, a series of narrow pulses are generated at approximately 5% duty cycle which periodically sample the state of the load. Thus device power dissipation is greatly reduced during this mode of operation.

Parallel Operation

Although no special provision for forced current sharing has been incorporated in the ART28XXT series, multiple units may be operated in parallel for increased output power applications. The 5 volt outputs will typically share to within approximately 10% of their full load capability and the dual (± 15 volt) outputs will typically share to within 50% of their full load. Load sharing is a function of the individual impedance of each output and the converter with the highest nominal set voltage will furnish the predominant load current.

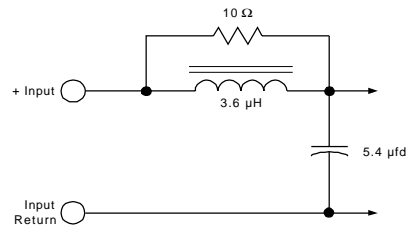
Input Undervoltage Protection

A minimum voltage is required at the input of the converter to initiate operation. This voltage is set to a nominal value of 16.8 volts. To preclude the possibility of noise or other variations at the input falsely initiating and halting converter operation, a hysteresis of approximately 1.0 volts is incorporated in this circuit. The converter is guaranteed to operate at 19 Volts input under all specified conditions.

Input Filter

To attenuate input ripple current, the ART28XXT series converters incorporate a single stage LC input filter. The elements of this filter comprise the dominant input load impedance characteristic, and therefore determine the nature of the current inrush at turn-on. The input filter circuit elements are as shown in Figure IV.

Figure IV. Input Filter Circuit

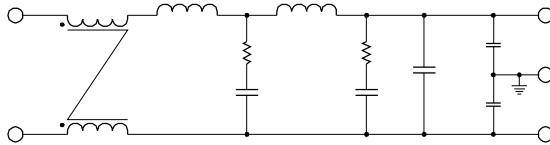


Additional Filtering

Although internal filtering is provided at both input and output terminals, some applications may require additional filtering in order to accommodate system requirements.

While the internal input filter of Figure IV. keeps input ripple current below 100 mA_{p-p}, an external filter may be applied to further attenuate this ripple to a level below the CE03 limits imposed by MIL-STD-461B. Figure V. describes a filter providing that attenuation.

Figure V. External Input EMI Filter

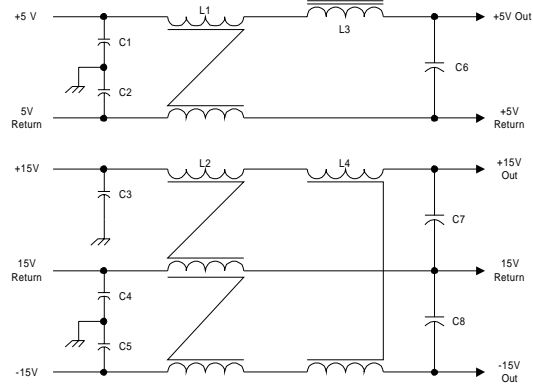


This circuit shown in Figure V has been constructed on copper clad board using the materials listed and tested in the laboratory.

An external filter may also be added to the output where circuit requirements dictate extremely low output ripple noise. The output filter described by Figure VI has been characterized with the ART2815T using the values shown in the associated material list.

It is important to be aware that when filtering high frequency noise, parasitic circuit elements can easily dominate filter performance. Therefore, it is incumbent on the designer to exercise care when preparing a circuit layout for such devices. Wire runs and lengths should be minimized, high frequency loops should be avoided and careful attention paid to the construction details of magnetic circuit elements. Tight magnetic coupling will improve overall magnetic performance and reduce stray magnetic fields.

Figure VI. External Output Filter



- L1 7 turns AWG21 bifilar on Mag Inc. core PN YJ-41305-TC or equivalent.
- L2 7 turns AWG24 trifilar on Mag Inc. core PN YJ-41305-TC or equivalent.
- L3 4 turns AWG21 on Mag Inc. core PN MPP55048 or equivalent.
- L4 5 turns AWG21 bifilar on Mag Inc. core PN MPP55048 or equivalent.
- C1-C5 2200pF type CKR ceramic capacitor.
- C6 170µF, 15V M39006/22-0514 Tantalum.
- C7, C8 25µF, 50V M39006/22-0568 Tantalum.

Measurement techniques can impose a significant influence on results. All noise measurements should be measured with test leads as close to the device output pins as physically possible. Probe ground leads should be kept to a minimum length.

Performance Characteristics (Typical @ 25°C)

Figure VII. Efficiency vs Output Power for Three Line Voltages.

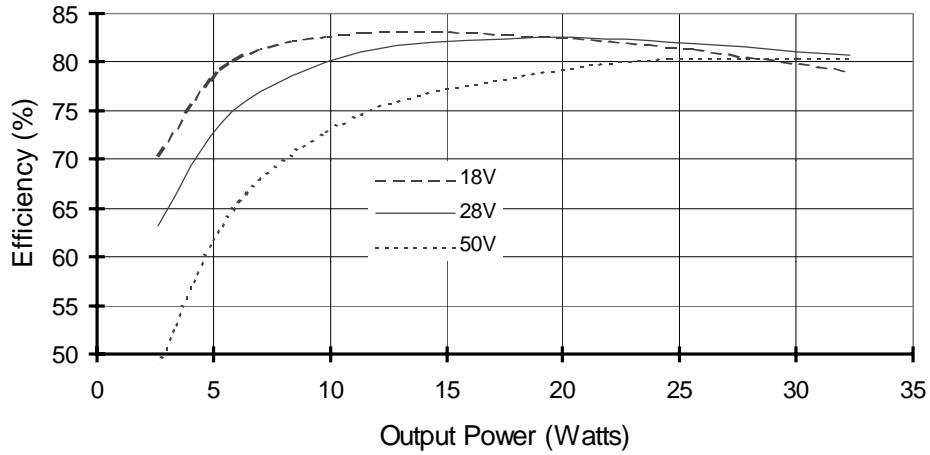
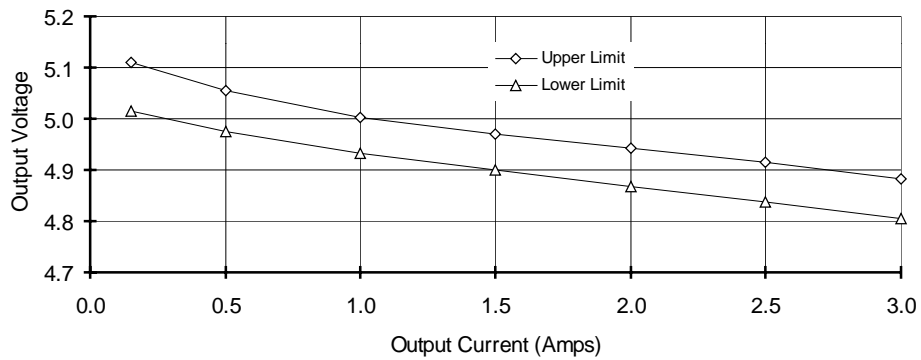


Figure VIII. 5V Output Regulation Limits Including all conditions of Line, Load and Cross Regulation.



Performance Characteristics (Typical @ 25°C) (Continued)

Figure IX. ± 15 V Regulation Curves

For Three conditions of Load on the 5 Volt Output.

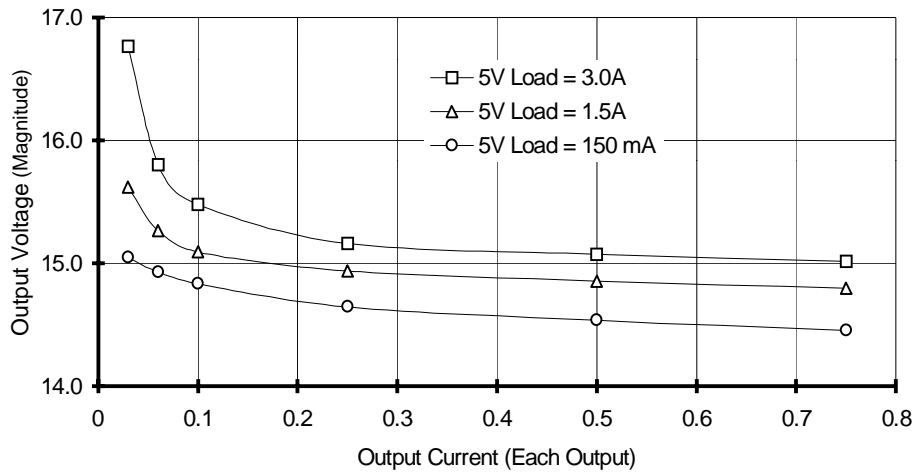
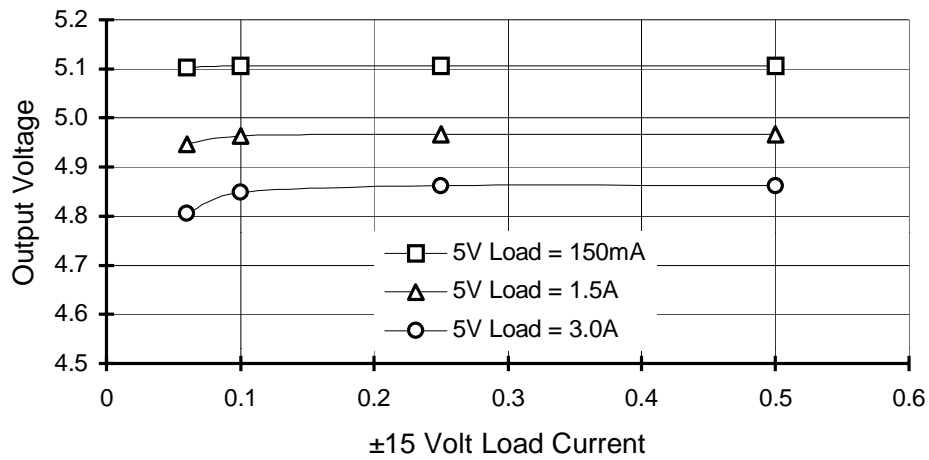


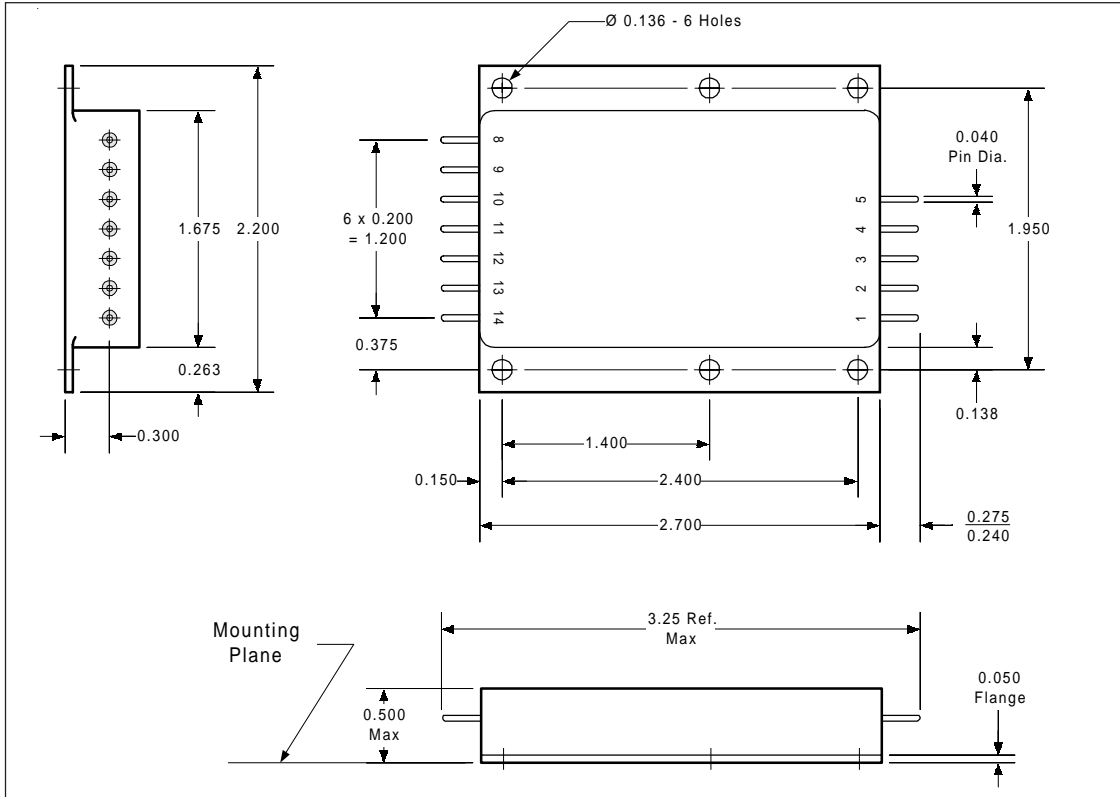
Figure X. Cross Regulation Curves

5 Volt Output as a function of 15 Volt Load Current for Three 5 Volt Loads.



ART28XXT Physical & Interface Characteristics

ART28XXT Case Outline

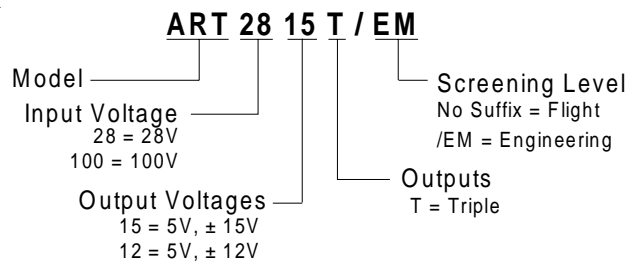


- Note:
1. Dimensions are in inches.
 2. Base Plate Mounting Plane Flatness 0.003 maximum.
 3. Unless otherwise specified, tolerances are
 - \angle = $\pm 2^\circ$
 - .XX = $\pm .01$
 - .XXX = $\pm .005$
 4. Device Weight - 120 grams maximum.

Pin Designation

| Pin # | Signal |
|-------|----------------------|
| 1 | + V input |
| 2 | Input return |
| 3 | Enable |
| 4 | Sync In |
| 5 | No connection |
| 8 | No connection |
| 9 | - 15 Vdc output |
| 10 | 15 Vdc output return |
| 11 | + 15 Vdc output |
| 12 | Chassis |
| 13 | + 5 Vdc output |
| 14 | 5 Vdc output return |

Part Numbering



Note:
Radiation performance not specified for /EM screened device type.

Standard Process Screening for ART28XXT Series

| Requirement | MIL-STD-883 Method | /EM Limits | Flight Limits (Class K) |
|--|----------------------------------|------------------|----------------------------------|
| Temperature Range | | -55°C to +125°C | -55°C to +125°C |
| Element Evaluation | | N/A | MIL-PRF-38534 |
| Non-destructive Bond Pull | 2023 | N/A | 100% |
| Internal Visual | 2017 | ✓ | ✓ |
| Temperature Cycle | 1010 | ✓ | Cond C |
| Constant Acceleration | 2001, | 500 g | Cond A |
| PIND | 2020 | N/A | Cond A |
| Burn-in Interim Electrical @ 160 hrs | 1015 | 160 hrs @ 125°C | 320 hrs @ 125°C (2 x 160 hrs) |
| Final Electrical (Group A) Read & Record Data | MIL-PRF-38534 & Specification | -55, +25, +125°C | -55, +25, +125°C |
| PDA (25°C, interim to final) | | N/A | 2% |
| Radiographic Inspection | 2012 | N/A | ✓ |
| Seal, Fine & Gross | 1014 | ✓ | Cond A, C |
| External Visual | 2009 | ✓ | ✓ |

Standard Periodic & Conformance Inspections on ART28XXT Series

| Inspection | Application | Quantity |
|------------|---|----------|
| Group A | Part of Screening on Each Unit | 100% |
| Group B | Each Inspection Lot | *5 units |
| Group C | First Inspection Lot or Following Class 1 Change | 10 Units |
| Group D | In Line (Part of Element Evaluation) | |

* Group B quantity for Option 2 End of Line QCI. No Group B samples required for Option 1, In-line.