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Bulletin I27180 19 - Sept

PIIPM30P06D009

iNTERO

Programmable Isolated IPM

PI-IPM Features:

- **Power Module:**
  - NPT IGBTs 30A, 600V
  - 10us Short Circuit capability
    - Square RBSOA
    - Low $Vce_{(on)}$ (2.05Vtyp @ 30A, 25°C)
    - Positive $Vce_{(on)}$ temperature coefficient
  - Gen III HexFred Technology
    - Low diode V_F (1.34Vtyp @ 30A, 25°C)
    - Soft reverse recovery
  - 5mΩ sensing resistors on all phase outputs
    - Thermal coefficient < 50ppm/°C

- **Embedded driving board**
  - Programmable 40 Mips DSP
  - Current sensing feedback from two phases
  - Full protection from ground and line to line faults
  - UVLO, OVLO on DCbus voltage
  - Embedded flyback smps for floating stages (single 15Vdc @ 300mA input required)
  - Asynchronous isolated 2.5Mbps serial port for DSP communication and/or programming
  - Synchronous isolated 10Mbps serial port for DSP communication and/or programming
  - IEEE standard 1149.1 (JTAG port interface) for program downloading and debugging
  - Separated turn on / turn off outputs for IGBTs di/dt control
  - Hall effect sensors, sin/cos and quadrature encoder interfaces
  - On board 64kbits I^2C EEprom

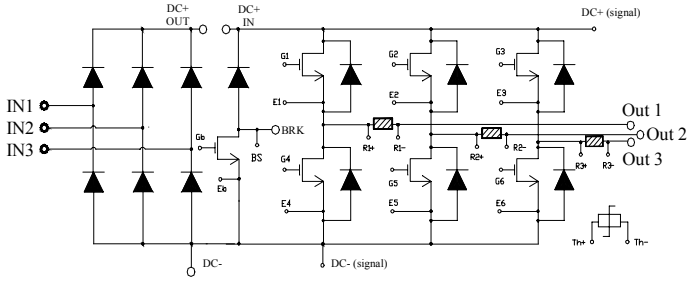
Description

The PIIPM30P06D009 is a fully integrated Intelligent Power Module for high performances Servo Motor Driver applications.
The device core is a state of the art DSP, the TMS320LF2406A at 40 Mips, interfaced with a full set of peripherals designed to handle all analog feedback and control signals needed to correctly manage the power section of the device. A 64kbits EEPROM is also available to store calibration data. The PIIPM has been designed and tailored to implement internally all functions needed to close the current, speed and position loops of a high performances servo motor driver.
The use of the flash memory version of the DSP and the JTAG port connector allows the user to easily develop and download his own proprietary algorithm.

Package:

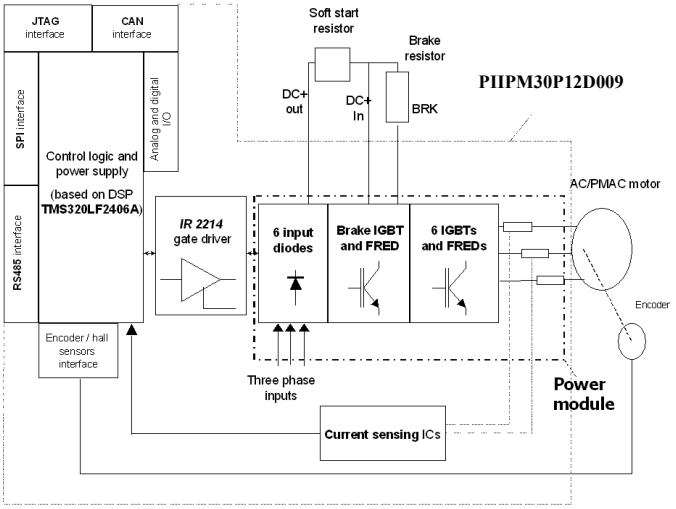
PIIPM – BBI (EconoPack 2 outline compatible)

Power Module schematic:



Input bridge, brake and three phases inverter (BBI) with current sensing resistors on all output phases and thermistor

PIIPM30P06D009 System Block Schematic:



The device comes in the EMP™ package, fully compatible in length, width and height with the popular EconoPack 2 outline

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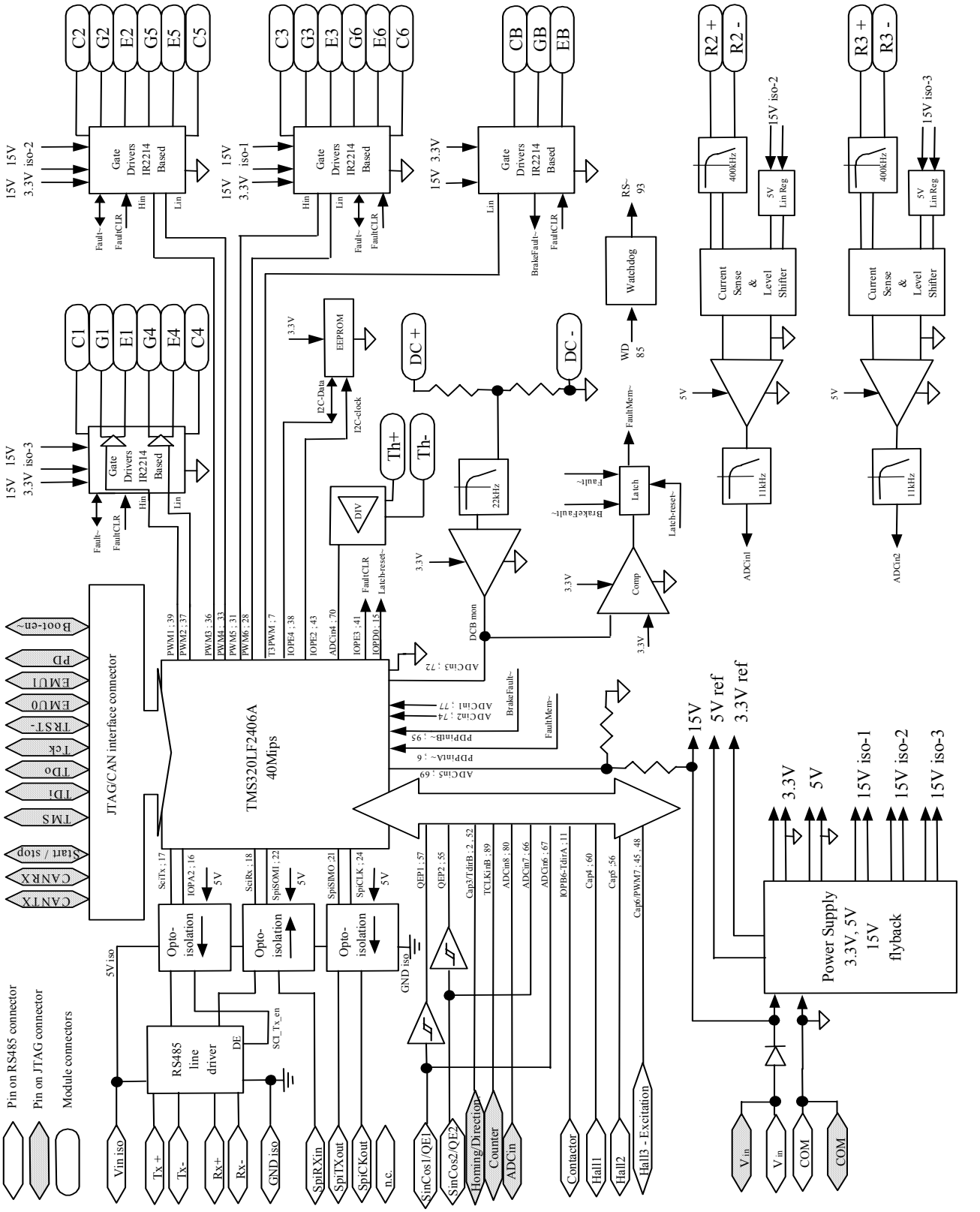
Embedded driving board block schematic



Signal pins on RS485 connector

Symbol	Lead Description	State	Connector pin number
Tx+	RS485 Trasmitter Non inverting Driver Output	Output	1
Tx-	RS485 Trasmitter Inverting Driver Output	Output	2
Rx-	RS485 Receiver Inverting Driver Input	Input	3
Rx+	RS485 Receiver Non inverting Driver Input,	Input	4
SpiCKout	SPI clock output (GND iso referenced)	Output	5
Vin iso	External 5V supply voltage for opto-couplers and line driver supply	Input	6
GND iso	Extenal 5V supply ground reference for opto-couplers and line driver supply	Input	7
SpiTXout	SPI transmitter output (GND iso referenced)	Output	8
SpiRXin	SPI receiver input (GND iso referenced)	Input	10
SinCos1 / QE1	SinCos encoder input 1 / Quadrature encoder input 1	Input	11
SinCos2 / QE2	SinCos encoder input 2 / Quadrature encoder input 2	Input	12
Contactor	General purpose I/O	I/O	13
Hall1	Hall effect sensor input 1	Input	14
Hall2	Hall effect sensor input 2	Input	15
Hall3 / Excitation	Hall effect sensor input 3 / Resolver excitation	I/O	16
Vin	External 15V supply voltage. Internally referred to DC bus minus pin (DC -)	Input	17-18
COM	External 15V supply ground reference. This pin is directly connected to DC -	Input	19-20

Signal pins on IEEE1149.1 JTAG connector

CAUTION: DO NOT APPLY DC BUS VOLTAGE WHEN JTAG INTERFACE IS CONNECTED, SEVERE DAMAGE MAY OCCUR ON POWER MODULE AND ON YOUR EQUIPMENT!

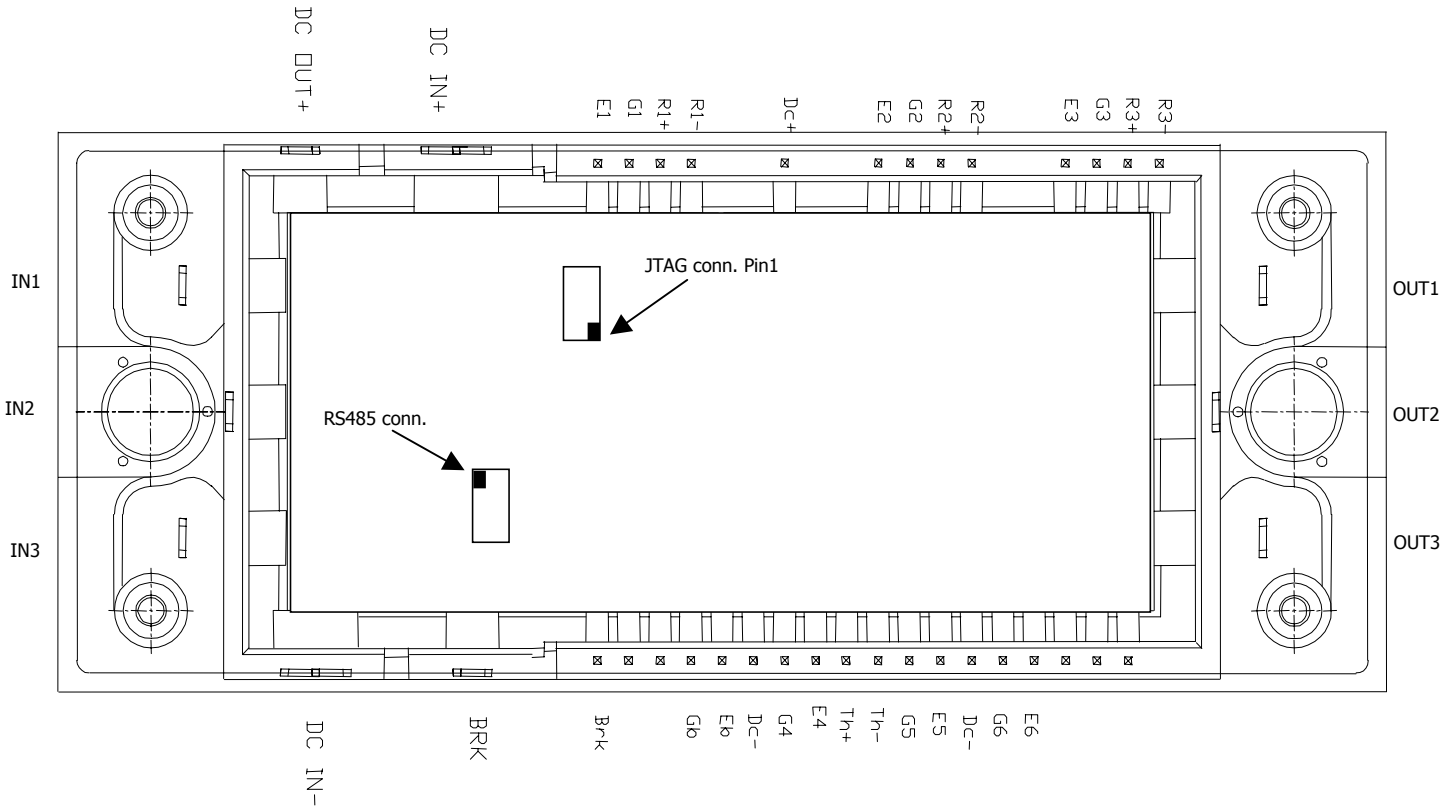
Symbol	Lead Description	State	Connector pin number
PD	Presence detect. Indicates that the emulation cable is connected and that the PIIPM logic is powered up. PD is tied to the DSP 3.3V supply through a 1k resistor.	Output	3
Homing / Direction	Homing signal / Counter direction	Input	4
Start/Stop	Start/Stop signal	Input	5
CAN Tx	CAN transmitter signal	Output	6
CAN Rx	CAN receiver signal	Input	7
EMU1/OFF~	Emulation pin 1	I/O	8
Counter	Counter signal	Output	9
EMU0	Emulation pin 0	I/O	10
TRST~	JTAG test reset	Input	13

TMS	JTAG test mode select	Input	14
TDO	JTAG test data output	Output	15
TDI	JTAG test data input	Input	16
TCKRET	JTAG test clock return. Test clock input to the emulator. Internally short circuited to TCK.	Output	17
TCK	JTAG test clock. TCK is a 10MHz clock source from the emulation pod. This signal can be used to drive the system test clock.	Input	18
Boot-En~	Boot ROM enable. This pin is sampled during DSP reset, pulling it low enables DSP boot ROM through SCI serial line at 40Mhz operation (Flash versions only). 47k internal pull up.	Input	19
ADCin	General purpose analog input	Input	20
COM	External 15V supply ground reference. This pin is directly connected to DC -	input	1-11
Vin	External 15V supply voltage. Internally referred to DC bus minus pin (DC-)	Input	2-12

Following pins are intended for signal communication between driving board and power module only, though here described for completeness, they are on purpose not available to the user.

Symbol	Lead Description	Pin number
DC +	DC Bus plus input signal	**Lateral connectors on embedded driving board**
DC -	DC Bus minus input signal (internally connected to COM)	
Th +	Thermal sensor positive input	
Th -	Thermal sensor negative input (internally connected to COM)	
Sh +	DC Bus minus series shunt positive input (Kelvin point)	
Sh -	DC Bus minus series shunt negative input (Kelvin point)	
G1/2/3	Gate connections for high side IGBTs	
E1/2/3	Emitter connections for high side IGBTs (Kelvin points)	
R1/2/3 +	Output current sensing resistor positive input (IGBTs emitters 1/2/3 side, Kelvin points)	
R1/2/3 -	Output current sensing resistor negative input (Motor side, Kelvin points)	
G4/5/6	Gate connections for low side IGBTs	
E4/5/6	Emitter connections for low side IGBTs (Kelvin points)	
Gb	Gate connections for brake IGBT	
Eb	Emitter connection for brake IGBT (Kelvin point)	
Brk	Collector connection for brake IGBT (Kelvin point)	

Power Module Frame Pins Mapping



Absolute Maximum Ratings (T_C=25ºC)

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur.
All voltage parameters are absolute voltages referenced to V_{DC-}, all currents are defined positive into any lead.
Thermal Resistance and Power Dissipation ratings are measured at still air conditions.

	Symbol	Parameter Definition			Min.	Max.	Units
Inverter and Brake	V_{DC}	DC Bus Voltage			0	500	V
	V_{CES}	Collector Emitter Voltage			0	600	
	$I_{C\,@\,100°C}$	IGBTs continuous collector current (T_C = 100 °C, fig. 1)				25	A
	$I_{C\,@\,80°C}$	IGBTs continuous collector current (T_C = 80 °C,fig 1)				30	
	$I_{C\,@\,25°C}$	IGBTs continuous collector current (T_C = 25 °C,fig 1)				45	
	I_{CM}	Pulsed Collector Current (Fig. 3, Fig. CT.5)				90	
	$I_{F\,@\,100°C}$	Diode Continuous Forward Current (T_C = 100 °C)				25	
	$I_{F\,@\,25°C}$	Diode Continuous Forward Current (T_C = 25 °C)				45	
	I_{FM}	Diode Maximum Forward Current				90	
	V_{GE}	Gate to Emitter Voltage			-20	+20	V
	$P_{D\,@\,25°C}$	Power Dissipation (One transistor)				138	W
	$P_{D\,@\,100°C}$	Power Dissipation (One transistor, T_C = 100 °C)				55	
Bridge	V_{RRM}	repetitive peak reverse voltage (T_j = 150 °C)				1400	V
	V_{RSM}	non repetitive peak reverse voltage				1500	
	I_o	Diode Continuous Forward Current (T_C = 100 °C, 120° Rect conduction angle)				45	A
	I_{FSM}	One-cycle forward. Non-repetitive on state surge current (t=10ms, Initial T_j =150°C)	100% V_{RRM} reapplied			225	
			No voltage reapplied			270	
	I^2t	Current I^2t for fusing (t=10ms, Initial T_j =150°C)	100% V_{RRM} reapplied			253	A^2s
			No voltage reapplied			365	
	$I^2\sqrt{t}$	Current $I^2\sqrt{t}$ for fusing (t=0.1 to 10ms, no voltage reapplied, Initial T_j = 150°C)				3650	$A^2\sqrt{s}$
Embedded Driving Board	V_{in}	Non isolated supply voltage (DC- referenced)			-20	20	V
	$V_{in\text{-}iso}$	Isolated supply voltage (GND iso referenced)			-5	5.5	
	Rx	RS485 Receiver input voltage (GND iso referenced)			-7	12	
	$T_{A\text{-}EDB}$	Operating Ambient Temperature Range			-25	+70	ºC
	$T_{STG\text{-}EDB}$	Board Storage Temperature Range			-40	+125	
	$V_{ISO\text{-}CONT}$ RS232	Input-Output Continuous Withstand Voltage (RH ≤ 50%, -40°C ≤ T_A ≤ 85°C)			AC DC	800 1000	V
	$V_{ISO\text{-}TEMP}$ RS232	Input-Output Momentary Withstand Voltage (RH ≤ 50%, t = 1 min, T_A = 25°C)		RMS	2500		
Power Module	MT	Mounting Torque				3.5	Nm
	T_J	Operating Junction Temperature			-40	+150	ºC
	T_{STG}	Storage Temperature Range			-40	+125	
	Vc-iso	Isolation Voltage to Base Copper Plate			-2500	+2500	V

Electrical Characteristics: Inverter and Brake

For proper operation the device should be used within the recommended conditions.
T_J = 25°C (unless otherwise specified)

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions	Fig.
$V_{(BR)CES}$	Collector To Emitter Breakdown Voltage	600			V	V_{GE} = 0V, I_C = 250µA	
$\Delta V_{(BR)CES} / \Delta T$	Temperature Coeff. of Breakdown Voltage		0.67		V/°C	V_{GE} = 0V, I_C = 1mA (25 - 125 °C)	
$V_{CE(on)}$	Collector To Emitter Saturation Voltage		1.91	2.2	V	I_C = 25A, V_{GE} = 15V	5, 6
			2.46	2.87		I_C = 45A, V_{GE} = 15V	7, 9
			2.19	2.55		I_C = 25A, V_{GE} = 15V, T_J = 125 °C	10, 11
$V_{GE(th)}$	Gate Threshold Voltage	4	4.46	5	V	V_{CE} = V_{GE}, I_C = 250µA	12
$\Delta V_{GE(th)} / \Delta Tj$	Temp. Coeff. of Threshold Voltage		-10		mV/°C	V_{CE} = V_{GE}, I_C = 1mA (25 – 125 °C)	
g_{fe}	Forward Trasconductance		18		S	V_{CE} = 50V, I_C = 30A	
I_{CES}	Zero Gate Voltage Collector Current			250	µA	V_{GE} = 0V, V_{CE} = 600V	
			368	580		V_{GE} = 0V, V_{CE} = 600V, T_J = 125 °C	
				2000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150 °C	
V_{FM}	Diode Forward Voltage Drop		1.29	1.48	V	I_C = 25A	8
			1.25	1.5		I_C = 25A, T_J = 125 °C	
I_{GES}	Gate To Emitter Leakage Current			±100	nA	V_{GE} =± 20V	
R1/2/3	Sensing Resistors	4.95	5	5.05	mΩ		

Electrical Characteristics: Bridge

For proper operation the device should be used within the recommended conditions.
T_J = 25°C (unless otherwise specified)

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions		Fig.
V_{FM}	Forward Voltage Drop			1.45	V	t_p = 400µs, I_{pk} = 45A		24
$V_{F(TO)}$	Threshold voltage		0.78		V	T_J = 125 °C		
I_{rm}	Reverse Leakage Current			5	mA	T_J = 125 °C	V_R = 1200V	

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Switching Characteristics: Inverter and Brake

For proper operation the device should be used within the recommended conditions.
T_J = 25°C (unless otherwise specified)

Symbol	Parameter Definition	Min	Typ	Max	Units	Test Conditions	Fig.
Q_g	Total Gate Charge (turn on)		102	153	nC	I_C = 30A V_{CC} = 400V V_{GE} = 15V	23 CT1
Q_{ge}	Gate – Emitter Charge (turn on)		14	21			
Q_{gc}	Gate – Collector Charge (turn on)		44	66			
E_{on}	Turn on Switching Loss		0.469	0.779	mJ	I_C = 30A, V_{CC} = 400V, T_J = 25 °C	CT4
E_{off}	Turn off Switching Loss		0.338	0.507		V_{GE} = 15V, R_G =10Ω, L = 800µH	WF1
E_{tot}	Total Switching Loss		0.807	1.281		Tail and Diode Rev. Recovery included	WF2
E_{on}	Turn on Switching Loss		0.631	0.946	mJ	I_C = 30A, V_{CC} = 400V, T_J = 125 °C	13, 15 CT4 WF1 WF2
E_{off}	Turn off Switching Loss		0.604	0.906		V_{GE} = 15V, R_G =10Ω, L = 800µH	
E_{tot}	Total Switching Loss		1.235	1.852		Tail and Diode Rev. Recovery included	
td (on)	Turn on delay time		101	152	ns	I_C = 30A, V_{CC} = 400V, T_J = 125 °C V_{GE} = 15V, R_G =10Ω, L = 800µH	14,16 CT4 WF1 WF2
Tr	Rise time		25	38			
td (off)	Turn off delay time		130	195			
Tf	Fall time		105	156			
C_{ies}	Input Capacitance		1750		pF	V_{CC} = 30V V_{GE} = 0V f = 1MHz	22
C_{oes}	Output Capacitance		160				
C_{res}	Reverse Transfer Capacitance		60				
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T_J = 150 °C, I_C =90A, V_{GE} = 15V to 0V V_{CC} = 500V, V_p = 600V, R_G = 10Ω	4 CT2
SCSOA	Short Circuit Safe Operating Area	10			µs	T_J = 150 °C, V_{GE} = 15V to 0V V_{CC} = 360V, Vp= 600V, R_G = 10Ω	CT3 WF4
E_{REC}	Diode reverse recovery energy		925	1165	µJ	T_J = 125 °C	17,18 19,20 21 CT4 WF3
Trr	Diode reverse recovery time		77		ns	I_F= 30A, V_{CC} = 400V, V_{GE} = 15V, R_G =10Ω, L = 800µH	
Irr	Peak reverse recovery current		62	93	A		
Rth_{J-C_T}	Each IGBT to copper plate thermal resistance		0.806	0.9	°C/W	See also fig. 25 and 26	
Rth_{J-C_D}	Each Diode to copper plate thermal resistance		1.06	1.22	°C/W		
Rth_{C-H}	Module copper plate to heat sink thermal resistance. Silicon grease applied = 0.1mm		0.03		°C/W		
Pdiss	Total Dissipated Power		23		W	I_C = 3.3A, V_{DC} = 300V, fsw = 8kHz, T_C = 55 °C	PD1
			40			I_C = 6A, V_{DC} = 300V, fsw = 8kHz, T_C = 55 °C	PD2
			61			I_C = 6A, V_{DC} = 300V, fsw = 16kHz T_C = 55 °C,	PD3
			95			I_C = 14A, V_{DC} = 300V, fsw = 4kHz, T_C = 55°C	

Electrical Characteristics: Embedded Driving Board (EDB) communication ports

For proper operation the device should be used within the recommended conditions.
Vin = 15V, Vin-iso = 5V, T_A = 0 to 55°C, T_C = 75°C (unless otherwise specified)

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions	Type	Conn.
Vin	EDB Input supply Voltage	12	15	18	V		Non isolated Suppy	RS485
Isupp	EDB Input Supply Current		150	250	mA	V_{DC} = 350V, f_{PWM} = 16kHz		
Vin iso	EDB isolated supply voltage	4.5	5	5.5	V		Isolated supply	
Iq. iso	EDB isolated quiescent supply current		9	15	mA	Rx+ = +5V, Rx- = 0V SPIRxIn open		
Isupp. iso	EDB isolated supply current	10	15	22	mA	SPIRxIn low Rx+ = 0V, Rx- = +5V Tx+ and Tx- open		
		50	55	62	mA	SPIRxIn low Rx+ = 0V, Rx- = +5V Tx+ and Tx- on 120Ω		
V_{DO-TX}	Differential Driver Output Voltage	2			V	Rload = 120 Ω	RS485 port	
V_{CO-TX}	Driver Common mode output voltage			3	V			
V_{DI-RX}	Receiver Input Differential Threshold Voltage	- 0.2		0.2	V	- 7V ≤ V_{CM} ≤ +12V		
R_{IN-RX}	Receiver Input Resistance		120		Ω			
f_{MAX}	RS485 maximum data rate			2.5	Mbps			
SpiRxIn	Logic High Input Voltage	3.8			V		SPI port	
	Logic Low Input Voltage			1.0	V			
	Logic Low Input Current			-5	mA			
SpiTxOut SpiCkOut	Logic Low Output Voltage			0,8	V	Iout = -510µA		
				1,2	V	Iout = -1,2mA		
	Logic High Output Voltage	2.4			V	Iout = 3mA		
TMS,TDI,TDO TCK,TRST- EMU0 EMU1/OFF~ PD	JTAG interface pins (**CAUTION: DO NOT APPLY DC BUS VOLTAGE WHEN JTAG INTERFACE IS CONNECTED, SEVER DAMAGE MAY OCCUR ON POWER MODULE AND ON YOUR EQUIPMENT!**)	Please see TMS320LF2406A datasheet from Texas Instruments and V_{PD} specifications				Directly connected from DSP to connector pins. EMU0 and EMU1 with 4.7k internal pull up.	JTAG	JTAG
V_{PD}	Presence detect voltage	3.2	3.3	3.4	V	I_{PD} = -100µA	JTAG	
$V_{Boot\ En\sim}$	Boot ROM enable input voltage			0.5	V	Active low	JTAG	
$I_{Boot-En\sim}$	Boot ROM enable input current			- 100	µA			
CAN Tx	Logic Low Output Voltage			0.8	V	Iout = - 780µA	CAN port	
	Logic High Output Voltage	2.4			V	Iout = 860µA		
CAN Rx	Logic Low Input Voltage			0.8	V			
	Logic High Input Voltage	2.4			V			

~ indicates active low signals

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AC Electrical Characteristics: Embedded Driving Board (EDB)
DSP pins mapping

For proper operation the device should be used within the recommended conditions.
Vin = 15V, Vin-iso = 5V, T_A = 0 to 55°C, T_C = 75°C (unless otherwise specified)

Symbol	Parameter Definition		Min.	Typ.	Max.	Units	Test Conditions	DSP name; pin N
V_{DCgain}	DC bus voltage feedback partition coefficient		5.27	5.47	5.57	mV/V		ADCIN03 ; 72
V_{DCpole}	DC bus voltage feedback second order filter		-	22	-	kHz		
$V_{DC-OVth}$	DC bus voltage over-voltage threshold		385	410	435	V		PDPINTA~ ; 6
V_{TH25C}	Thermal sensor voltage feedback at 25 °C (Fig. TF1)		2.65	2.75	2.85	V		ADCIN04 ; 70
V_{TH100C}	Thermal sensor voltage feedback at 100 °C (Fig. TF1)		1.04	1.09	1.14	V		
Vin-gain	Input voltage feedback partition coefficient		125	128	131	mV/V		ADCIN05 ; 69
Vin-pole	Input voltage feedback filter pole		1600	1700	1800	Hz		
Iph-GAIN	Current feedback gain		39	40	41	mV/A	all two phases	ADCIN01: 77 ADCIN02: 74
Iph-pole	Current feedback filter pole		9.8	10.9	12	kHz		
Iph-LAT	Current feedback signal delay				5	µs		
Iph-Zero	Zero current input voltage level		1.62	1.65	1.68	V		
Vce_sc	Vce Short Circuit Threshold detection			7.4		V	all phases	PDPINTA~ ; 6
I_{SC-DEL}	Short Circuit detection delay time			3	6	µs		
WD	External watchdog timeout (see also RS~ signal)		0.9	1.6	2.5	Sec		IOPC1 ; 85
ADCin	Generic purpose analog Input		0		3.3	V		ADCIN08 ; 80
	Generic purpose analog input filter pole			4.13		kHz		
SinCos1/QE1	Analog input 1 for sincos resolver		0		3.3	V	See also QEP1 signal	ADCIN06 ; 67
	Analog input for sincos resolver filter pole			4.13		kHz		
	QEP1: internal digital signal of QE1	High level threshold	2.4			V		QEP1 ; 57
		Low level threshold			1	V		
SinCos2/QE2	Analog input 2 for sincos resolver		0		3.3	V	See also QEP2 signal	ADCIN07;66
	Analog input for sincos resolver filter pole			4.13		kHz		
	QEP2: internal digital signal of QE2	High level threshold	2.4			V		QEP2 ; 55
		Low level threshold			1	V		
COM	DSP Ground		3, 5, 13, 14, 19, 26, 27, 29, 32, 34, 46, 53,55, 58, 63, 65, 68, 71, 73, 75, 76, 78,79, 81, 84, 90, 97					
3.3V	DSP 3.3V supply		4, 10, 20, 30, 35, 47, 54, 59, 64, 91, 98					
Floating	Not connected to anything		12, 23, 88, 25, 42, 44, 51					

~ indicates active low signals

Other DSP pins mapping to the connector

Symbol	Signal Definition	DSP name ; pin N	Comments	Connector
Hall1	Hall effect sensor input 1	CAP4/QEP3/IOPE7 ; 60	Digital Input. See elec. characteristic of I/O pins	RS485
Hall2	Hall effect sensor input 2	CAP5/QEP4/IOPF0 ; 56	Digital Input. See elec. characteristic of I/O pins	
Hall3 / Excitation	Hall effect sensor input 3 / Resolver excitation	PWM7/IOPE1, CAP6/IOPF1 ; 45, 48	Digital I/O, Output is type G3. See electrical characteristics of I/O pins	
Contactor	General purpose I/O	IOPB6 ; 11	Digital I/O, Output is type G3. See electrical characteristics of I/O pins	
CAN Tx	CAN transmit data	CANTX ; 50	Not isolated	JTAG
CAN Rx	CAN receive data	CANRX ; 49	Not isolated	
Homing/Direction	Homing signal/ Counter direction	TDIRB/IOPF4, CAP3/IOPA5 ;2, 52	Avoid electrical conflicts beetwen these two pins	
Start/Stop	Start/Stop signal	IOPF6 ; 92	Digital Input. See elec. Characteristic of I/O pins	
Boot En~	Boot ROM enable signal	BOOT_EN~ ; 86	See also EDB electrical characteristics	
Counter	Counter signal	TCLKINB ; 89	Digital Input. See elec. Characteristics of I/O pins	

These signals are internal only

Symbol	Signal Definition	DSP name ; pin N	Comments
PWM1	Out 1 high side IGBT gate drive signal	PWM1; 39	DSP Event Manager A output
PWM2	Out 1 low side IGBT gate drive signal	PWM2 ; 37	DSP Event Manager A output
PWM3	Out 2 high side IGBT gate drive signal	PWM3 ; 36	DSP Event Manager A output
PWM4	Out 2 low side IGBT gate drive signal	PWM4 ; 33	DSP Event Manager A output
PWM5	Out 3 high side IGBT gate drive signal	PWM5 ; 31	DSP Event Manager A output
PWM6	Out 3 low side IGBT gate drive signal	PWM6 ; 28	DSP Event Manager A output
Brake	Brake IGBT gate drive signal	IOPF2 ; 7	DSP Event Manager B output
SpiTXout	SpiTx output	SPISIMO ; 21	These signal are optically isolated. See also EDB electrical characteristics
SpiRXout	SpiRx input	SPISOMI ; 22	
SpiCKout	SpiClk output	SPICLK ; 24	
Ref3.3V	3.3V reference voltage	VREFHI, VCCA ; 82, 83	3.3V reference and supply voltage for ADC converter
5V supp.	Flash programming voltage pin	VCCP ; 40	Supplied by the embedded flyback regulator
Tx	SCI transmit data	SCITXD ; 17	Drives Tx+ and Tx- through the opto-isolator and the line driver
Rx	SCI receive data	SCIRXD ; 18	Driven by Rx+ and Rx- through the opto-isolator and the line driver
SCI_Tx_en	SCI transmitter enable	IOPA2 ; 16	Enable a line driver through an opto-isolator
Latch-reset~	System general fault output reset signal	IOPD0 ; 15	LFAULT Reset signal, to be activated via software after a fault or system boot, active low.
FaultCLR	Gate driver fault output reset signal	IOPE3 ; 41	Gate driver reset, to be activated via software after a short-circuit or system boot

RS~	DSP reset input signal (see also WD signal)	RS~ ; 93	Forces a DSP reset if WD signal holds too long (see also EDB electrical char.)
Xtal1	PLL oscillator input pin	XTAL1 ; 87	A 10Mhz oscillator at 100ppm frequency stability feeds this pin.
PLLF1	PLL filter input 1	PFFL ; 9	PLL filter for 40Mhz DSP clock frequency
PLLF2	PLL filter input 2	PLLF2 ; 8	PLL filter for 40Mhz DSP clock frequency
FaultMem~	System general fault input	PDPINTA~ ; 6	Activated by short circuits on output phases or brake IGBTand by DC bus over-voltage comparator. Latched signal, see also Latch-reset
BrakeFault~	Brake Protection Interrupt signal	PDPINTB~ ; 95	Activated by short circuits on brake
QEP1	Square wave of SinCos1/QE1	QEP1 ; 57	Internal Schmitt trigger, see also AC electrical characteristic
QEP2	Square wave of SinCos2/QE2	QEP2 ; 55	Internal Schmitt trigger, see also AC electrical characteristic
WD	Output signal for external watchdog	IOPC1 ; 85	WD = high impedance, external watchdog is disabled WD = high or WD = low, external watchdog is enabled and WD has to be periodically triggered by positive or negative transition. When the supervising system fails to retrigger the ext. watchdog within the time shown on AC electrical Characteristics, RS~ signal becomes active.

~ indicates active low signals

64kbits I^2C EEprom (please see Microchip 24LC4 for more specifications)

Symbol	Signal Definition	DSP name ; pin N	Comments
I^2C - Clock	I^2C - Clock	IOPE2 ; 43	Connected to the I^2C EEPROM
I^2C - Data	I^2C - Clock	IOPE4 ; 38	Connected to the I^2C EEPROM

Electrical characteristic of digital inputs and outputs.

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions
Input: VIH	Logic high,generic input voltage	2.4			V	
Input: VIL	Logic low, generic input voltage			0.8	V	
Output Type G1(*)	VOH	2.4			V	Iout = 700µA
	VOL			0.8	V	Iout = - 700µA
Output Type G2(*)	VOH	2.4			V	Iout = 850 µA
	VOL			0.8	V	Iout = - 850 µA
Output Type G3(*)	VOH	2.4			V	Iout = 950 µA
	VOL			0.8	V	Iout = -950 µA

(*) Please refer to TMS320LF2406A datasheet from Texas Instruments for more specifications.

Fig. 1 – Maximum DC collector Current vs. case temperature

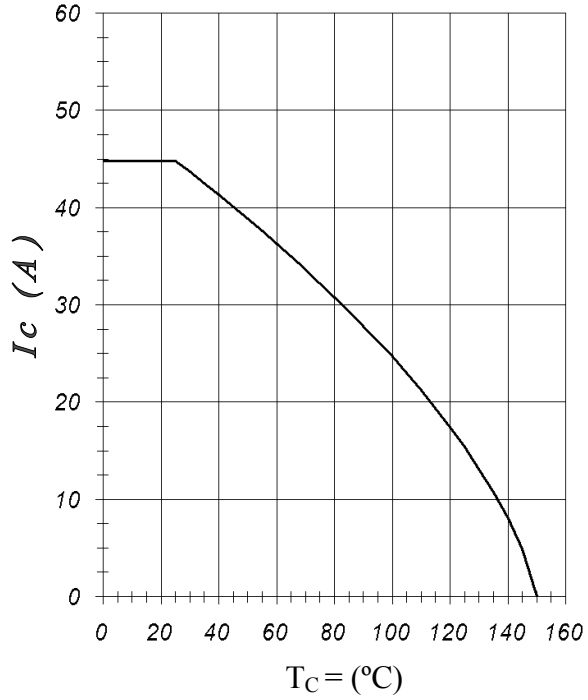


Fig. 2 – Power Dissipation vs. Case Temperature

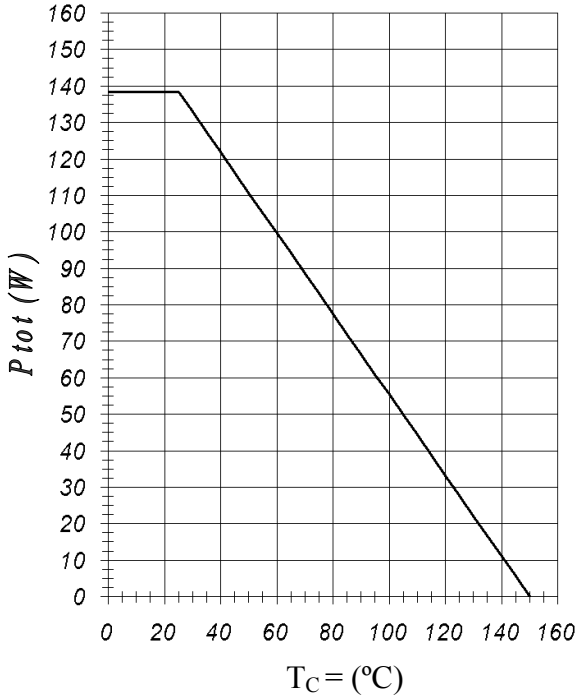


Fig. 3 – Forward SOA
T_C = 25ºC; Tj ≤ 150ºC

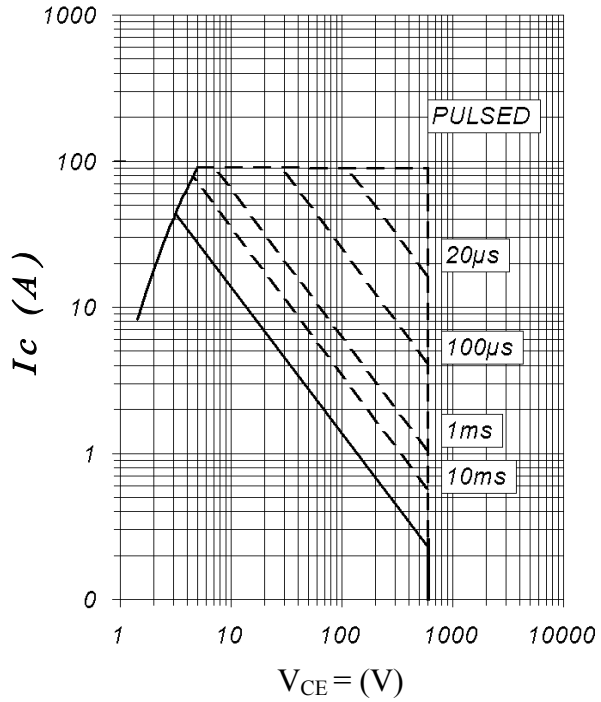


Fig. 4 – Reverse Bias SOA
Tj = 150ºC, V_{GE} = 15V

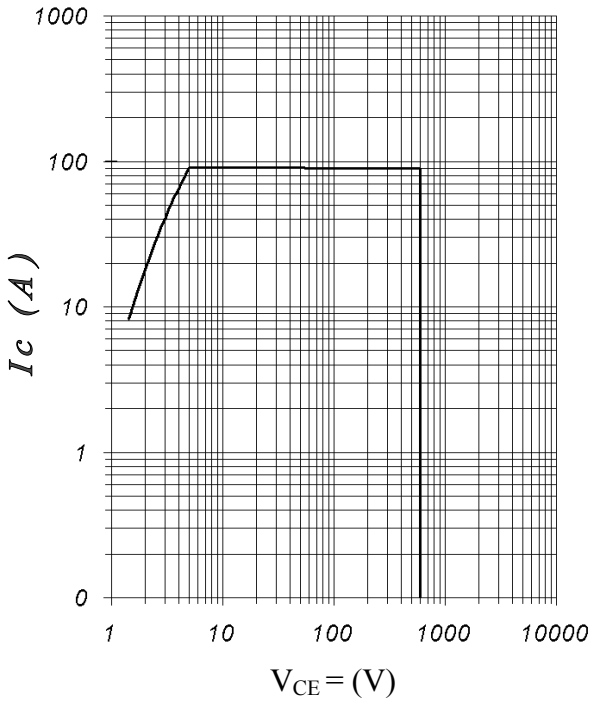


Fig. 5 – Typical IGBT Output Characteristics
Tj = - 40ºC; tp = 500µs

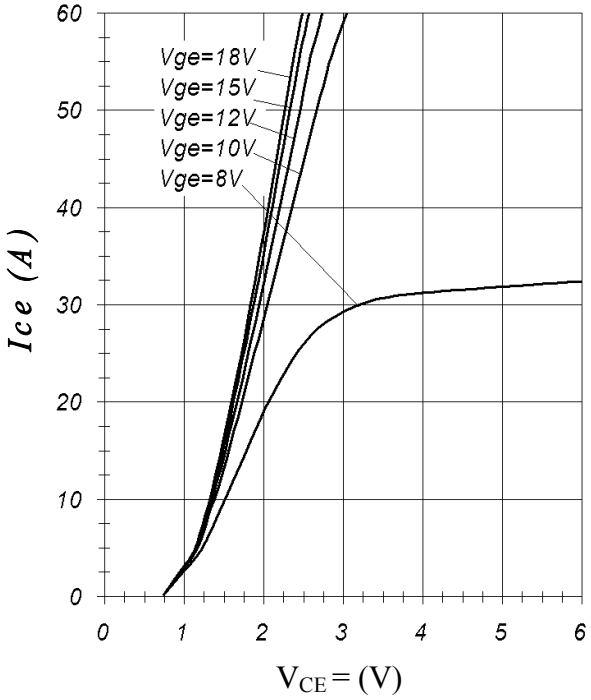


Fig. 6 – Typical IGBT Output haracteristics
Tj = 25ºC; tp = 500µs

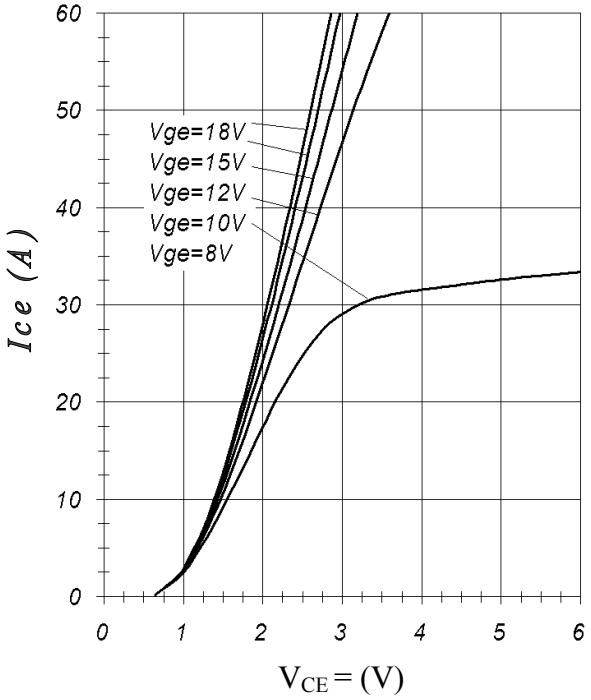


Fig. 7 – Typical IGBT Output Characteristics
Tj = 125ºC; tp = 500µs

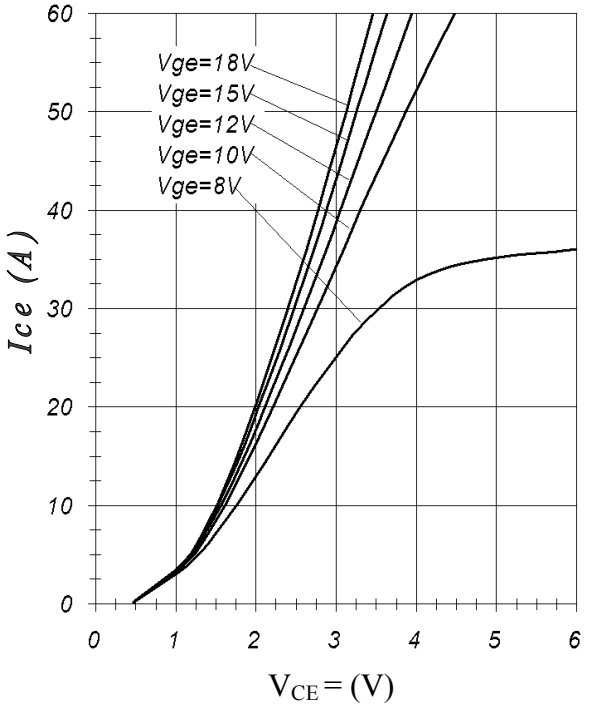


Fig. 8 – Typical Diode Forward Characteristics tp = 500µs

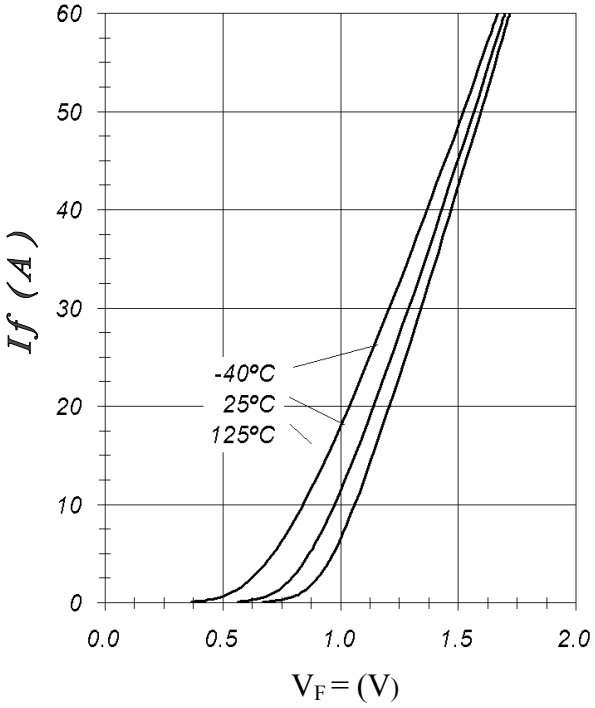


Fig. 9 – Typical V_{CE} vs. V_{GE}
Tj = - 40ºC

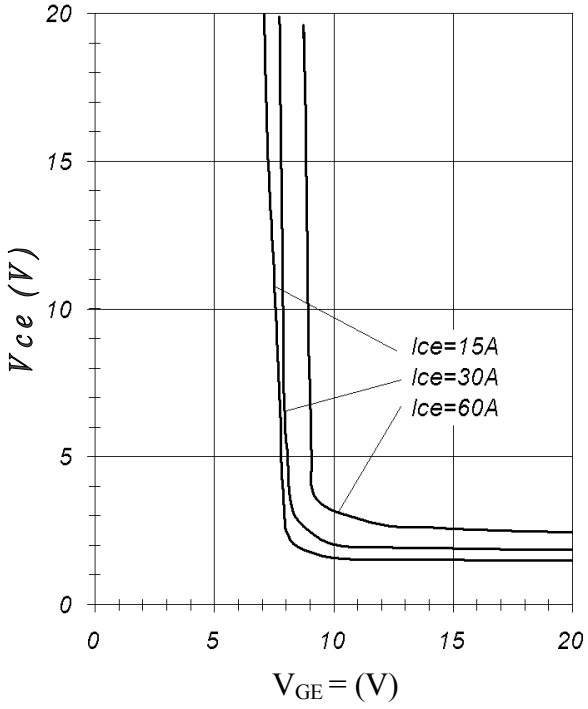


Fig. 10 – Typical V_{CE} vs. V_{GE}
Tj = 25ºC

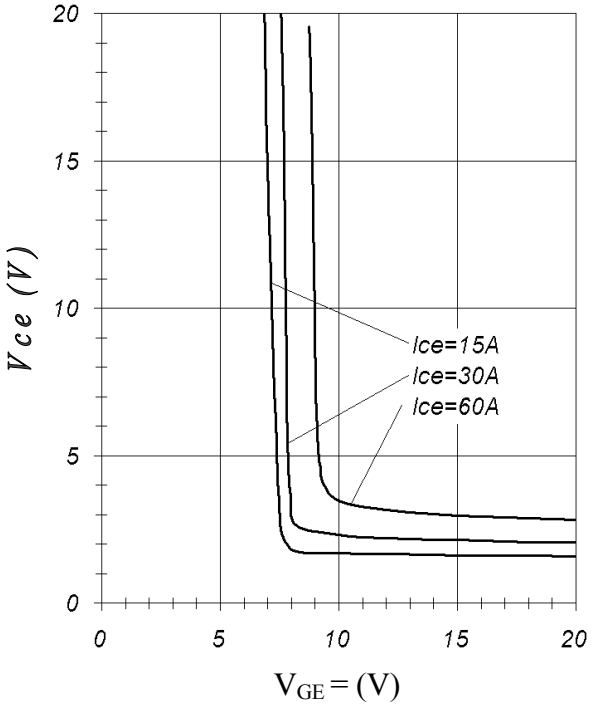


Fig. 11 – Typical V_{CE} vs. V_{GE}
Tj = 125ºC

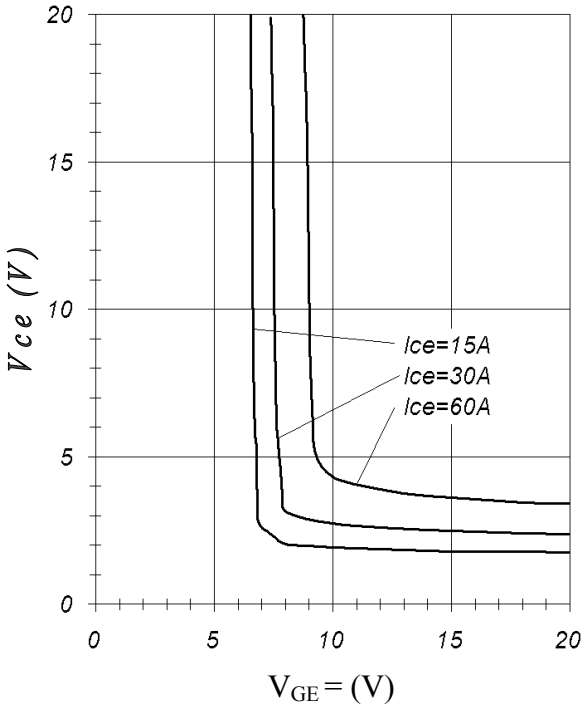


Fig. 12 – Typical Transfer Characteristics
V_{CE} = 20V; tp = 20µs

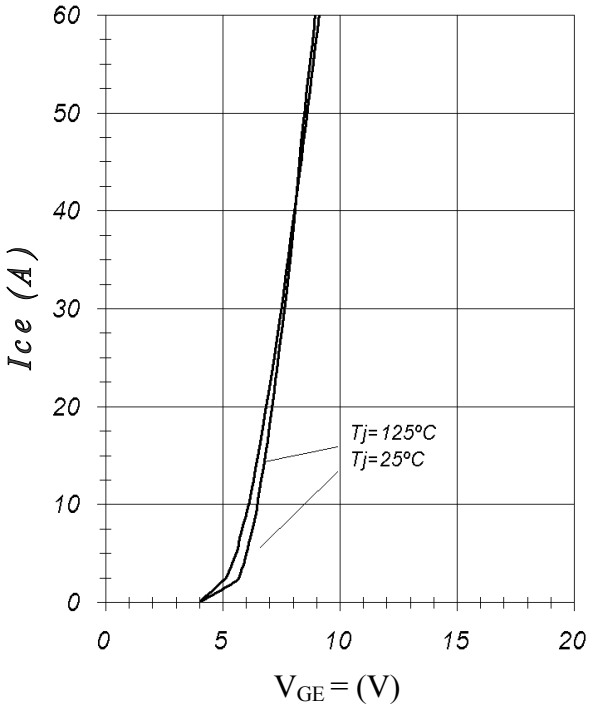


Fig. 13 – Typical Energy Loss vs. I_C
Tj = 125ºC; L = 800µH; V_{CE} = 400V;
Rg = 10Ω; V_{GE} = 15V

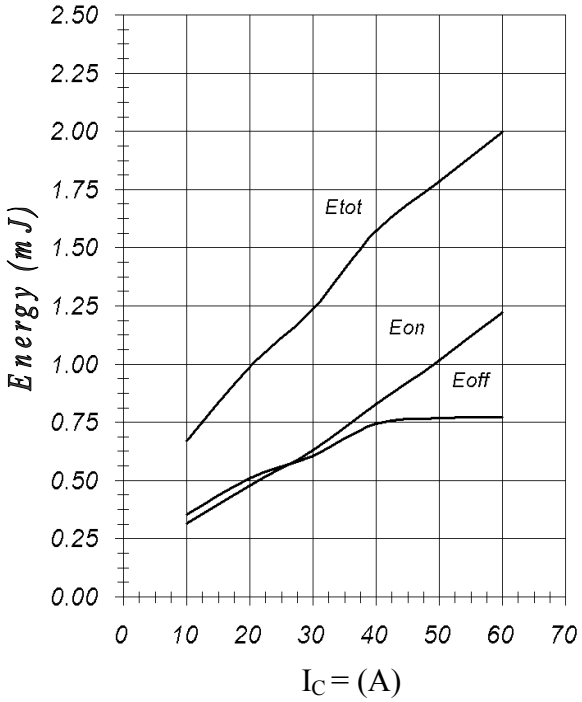


Fig. 14 – Typical Switching Time vs. I_C
Tj = 125ºC; L = 800µH; V_{CE} = 400V;
Rg = 10Ω; V_{GE} =15V

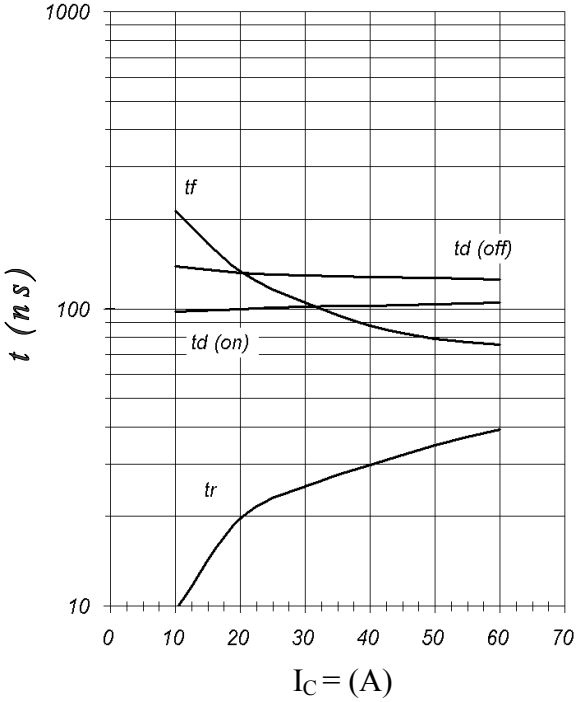


Fig. 15 – Typical Energy Loss vs. Rg
Tj = 125ºC; L = 800µH; V_{CE} = 400V;
I_{CE} = 30A; V_{GE} = 15V

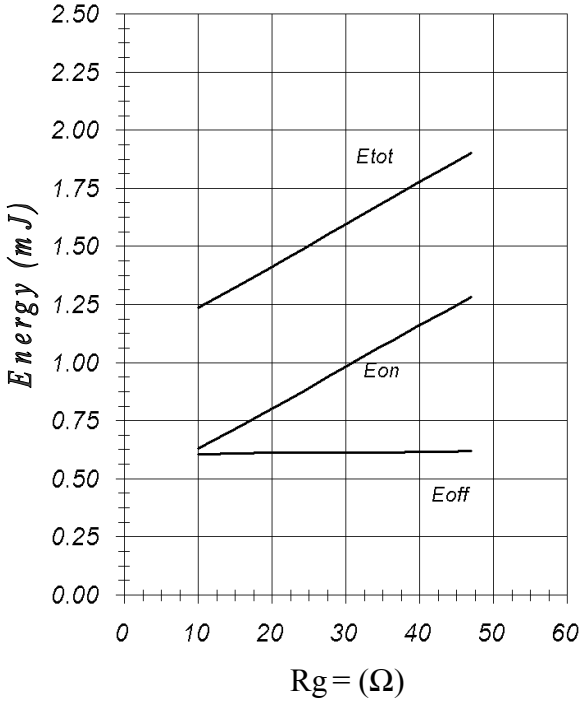


Fig. 16 – Typical Switching Time vs. Rg
Tj = 125ºC; L = 800µH; V_{CE} = 400V;
I_{CE} = 30A; V_{GE} = 15V

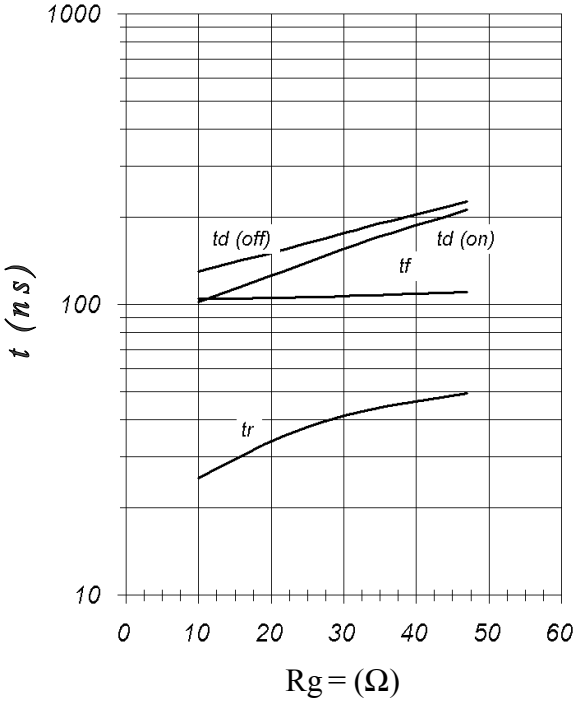


Fig. 17 – Typical Diode I_{RR} vs. I_F
Tj = 125ºC

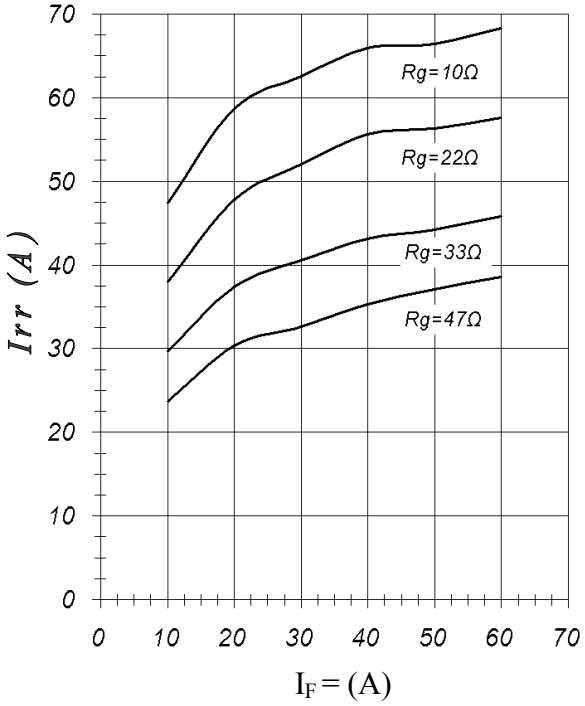


Fig. 18 – Typical Diode I_{RR} vs. Rg
I_F = 30A; Tj = 125ºC

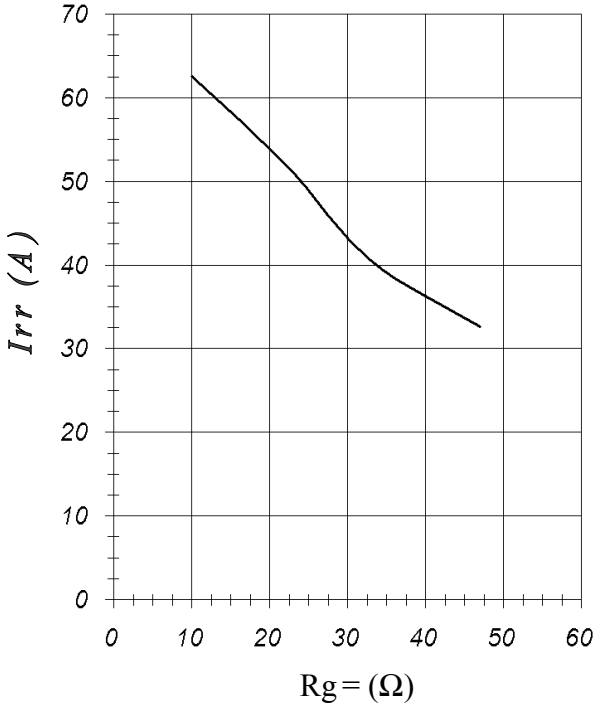


Fig. 19 – Typical Diode I_{RR} vs. dI_F/dt
V_{DC} = 400V; V_{GE} = 15V; I_F = 30A;
Tj = 125ºC

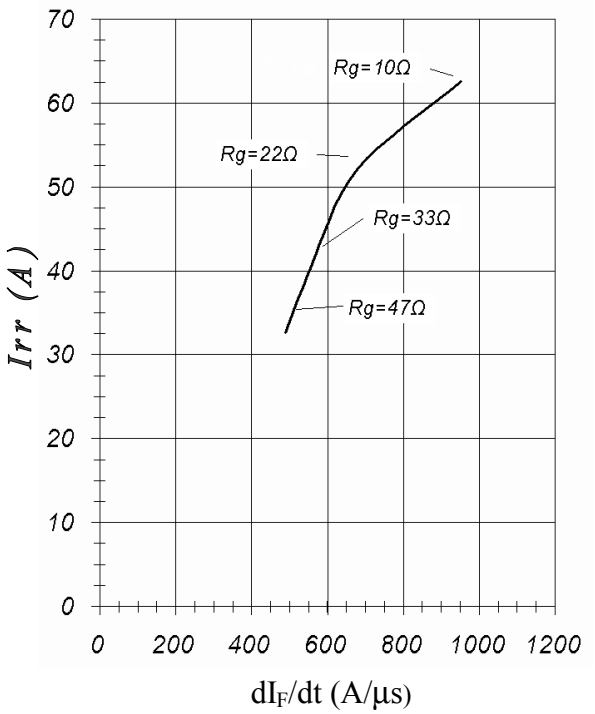


Fig. 20 – Typical Diode Q_{RR}
V_{DC} = 400V; V_{GE} = 15V; Tj = 125ºC

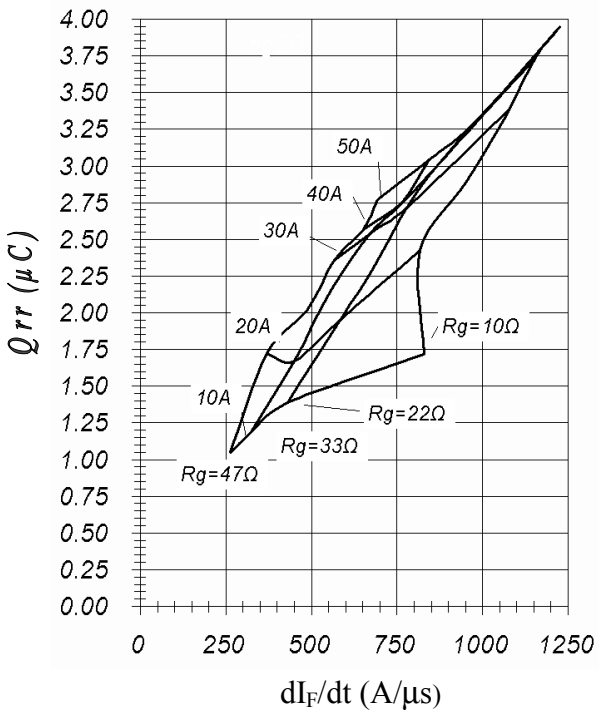


Fig. 21 – Typical Diode E_{REC} vs. I_F
Tj = 125ºC

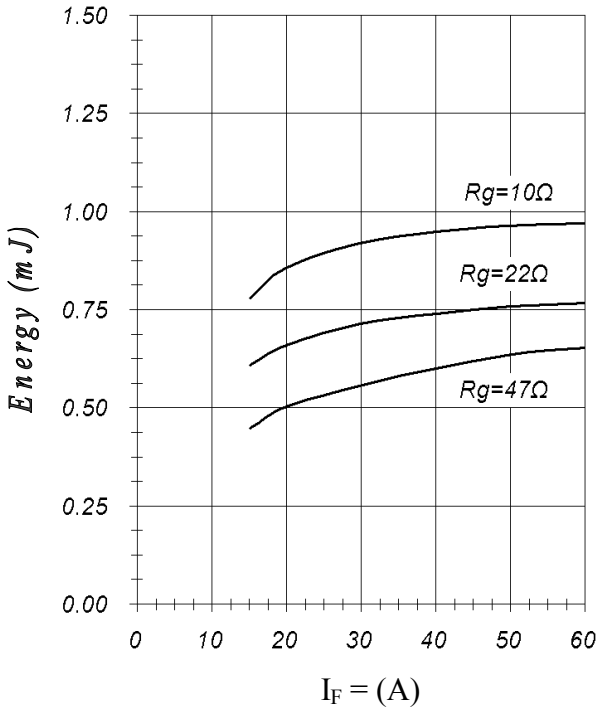


Fig. 22 – Typical Capacitance vs. V_{CE}
V_{GE} = 0V; f = 1MHz

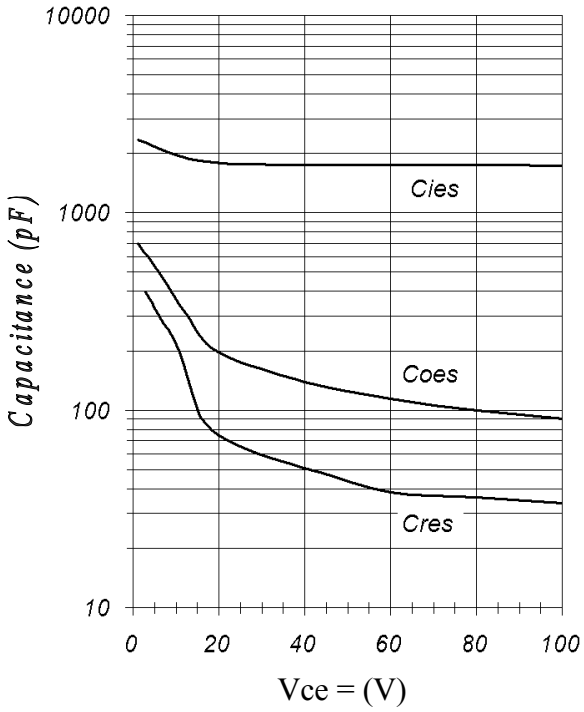


Fig. 23 – Typical Gate Charge vs. V_{GE}
I_C = 30A; L = 600µH; V_{CC} = 400V

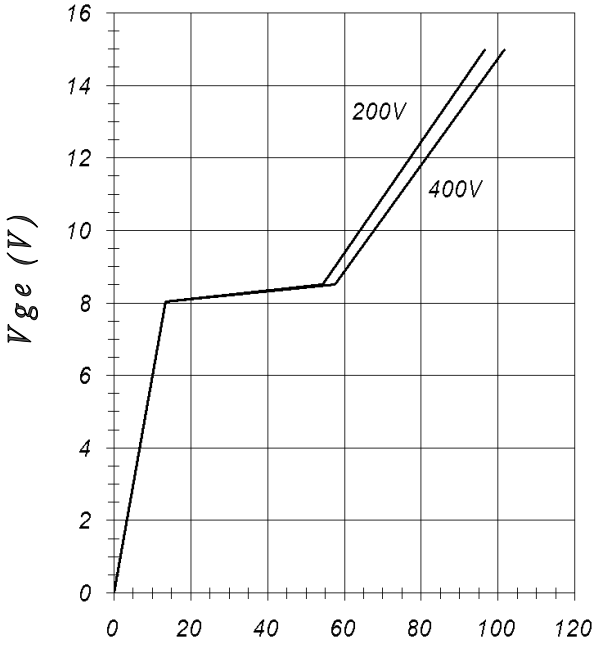


Fig. 24 – On state Voltage Drop
characteristic V_{FM} vs I_F t_p = 400µs

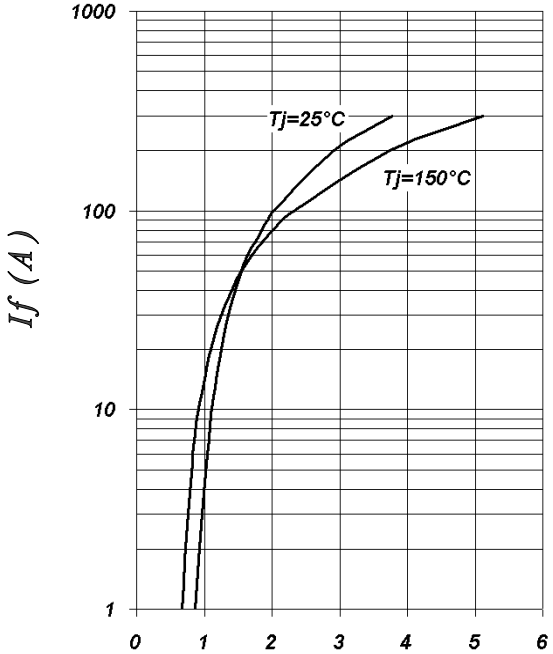
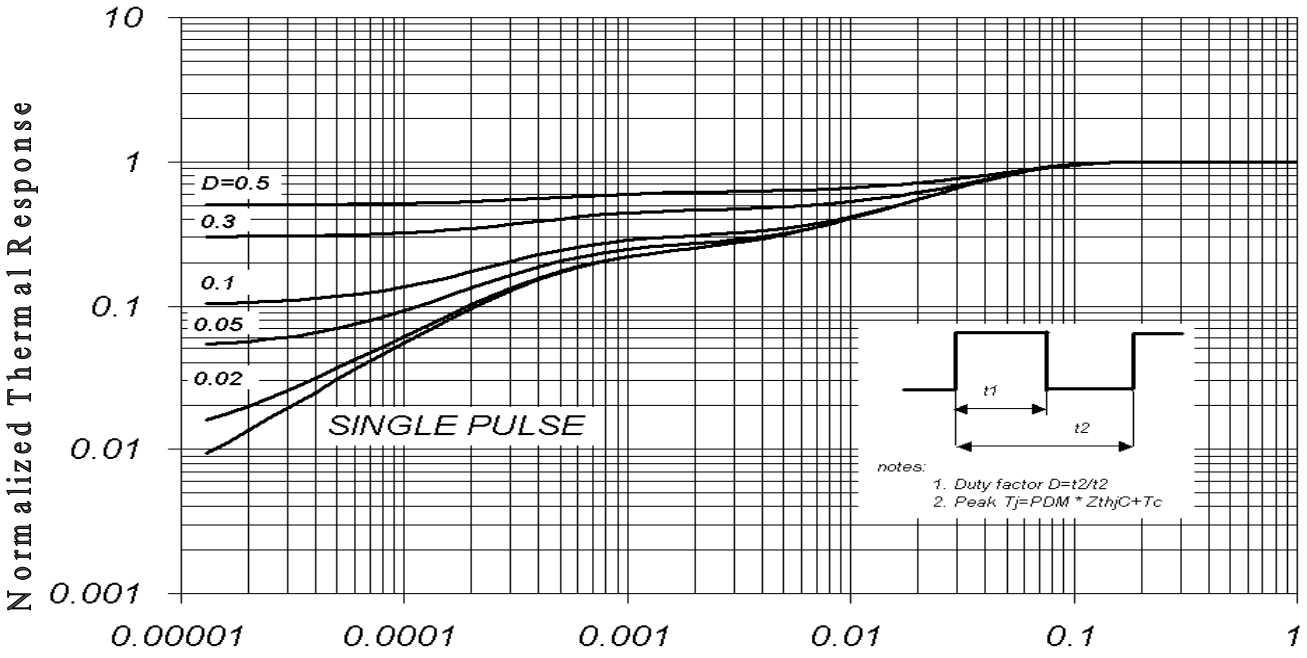
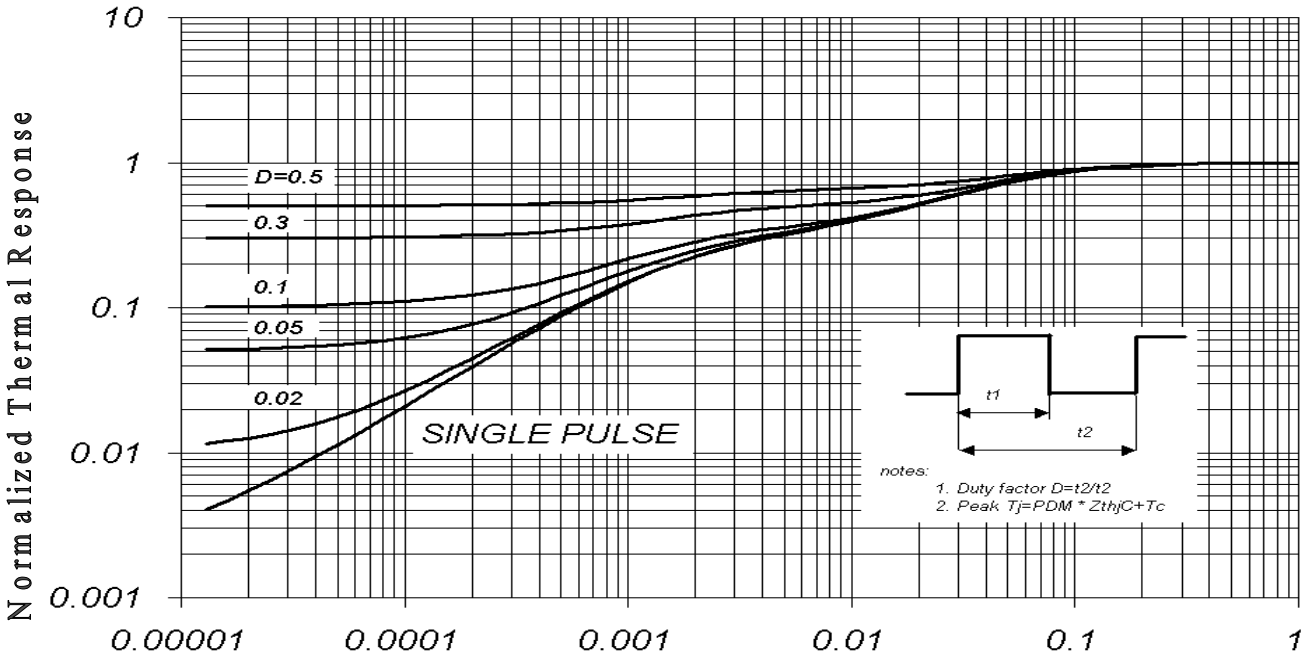


Fig. 25 – Normalized Transient Thermal Impedance, Junction-to-copper plate (IGBTs)



t1, Rectangular Pulse Duration (sec)

Fig. 26 – Normalized Transient Impedance, Junction-to-copper plate (FRED diodes)



t1, Rectangular Pulse Duration (sec)

Fig. CT.1 - Gate Charge Circuit (turn-off)

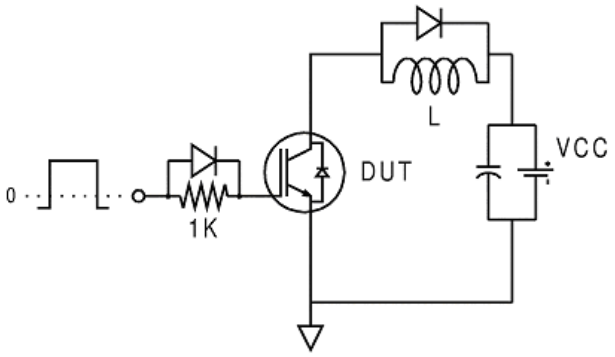


Fig. CT.2 - RBSOA Circuit

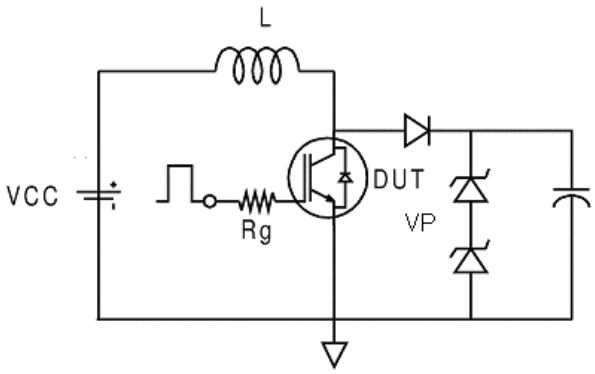


Fig. CT.3 - S.C. SOA Circuit

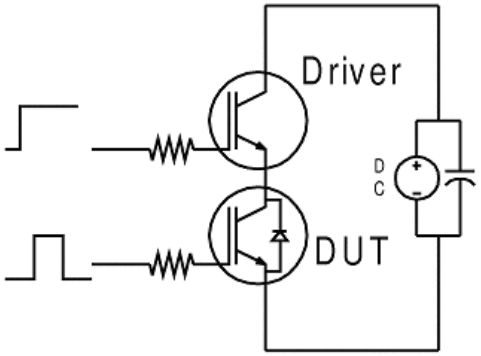


Fig. CT.4 - Switching Loss Circuit

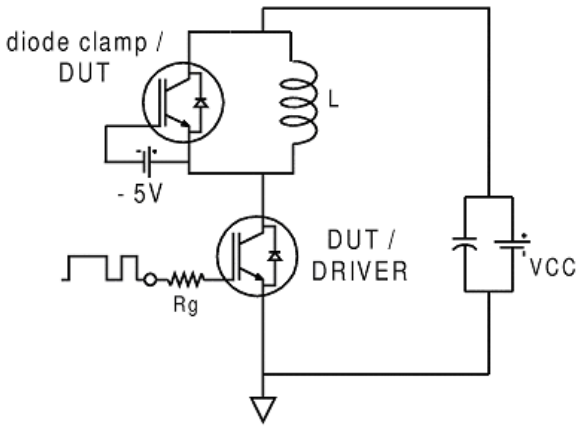


Fig. CT.5 - Resistive Load Circuit

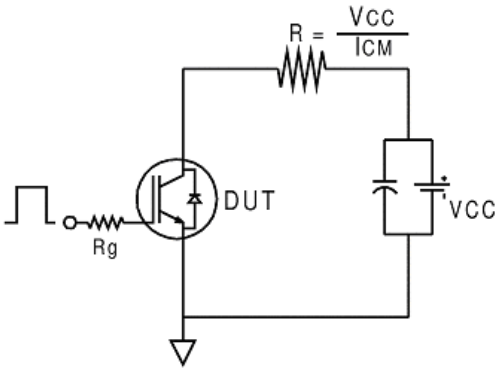


Fig. WF1- Typ. Turn-off Loss Waveform
@ T_J = 150°C using Fig. CT.4

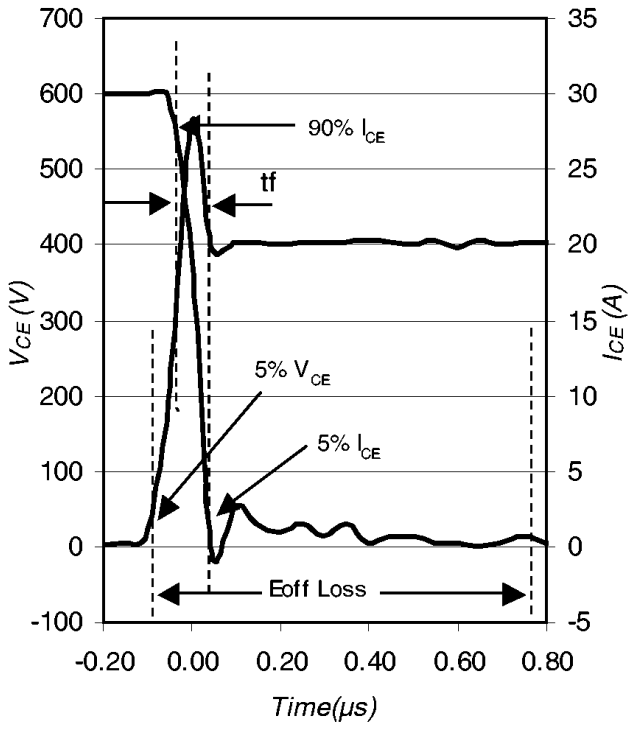


Fig. WF2- Typ. Turn-on Loss Waveform
@ T_J = 150°C using Fig. CT.4

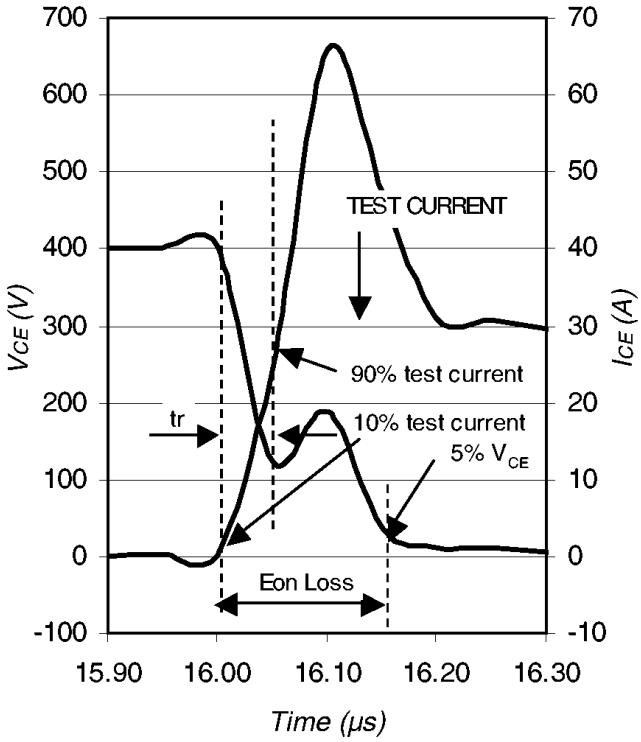


Fig. WF3- Typ. Diode Recovery Waveform
@ T_J = 150°C using Fig. CT.4

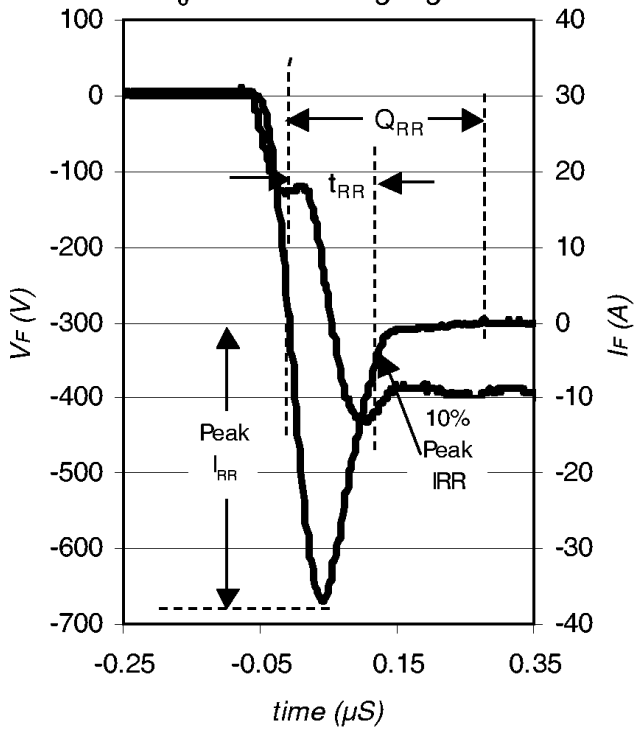


Fig. WF4- Typ. S.C Waveform
@ T_C = 150°C using Fig. CT.3

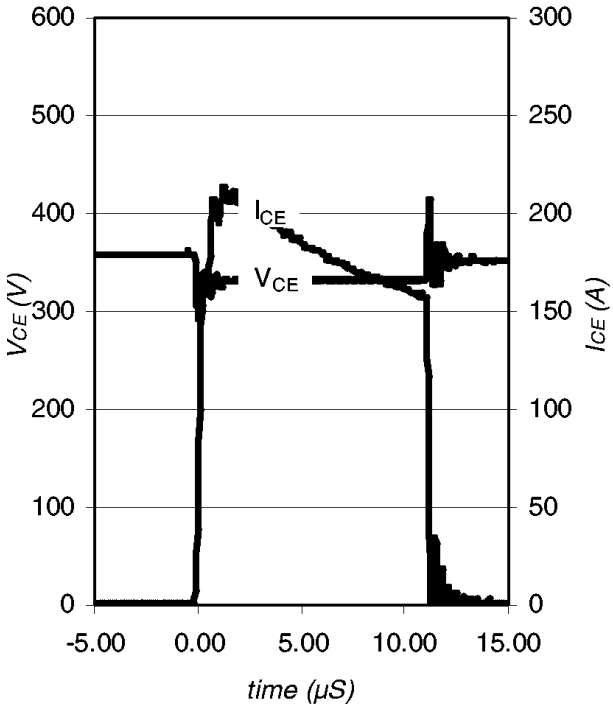


Fig. PD1 – Total Dissipated Power vs. f_{SW}
$Iout_{RMS}$ = 3.3A, V_{DC} = 300V, T_C = 55ºC

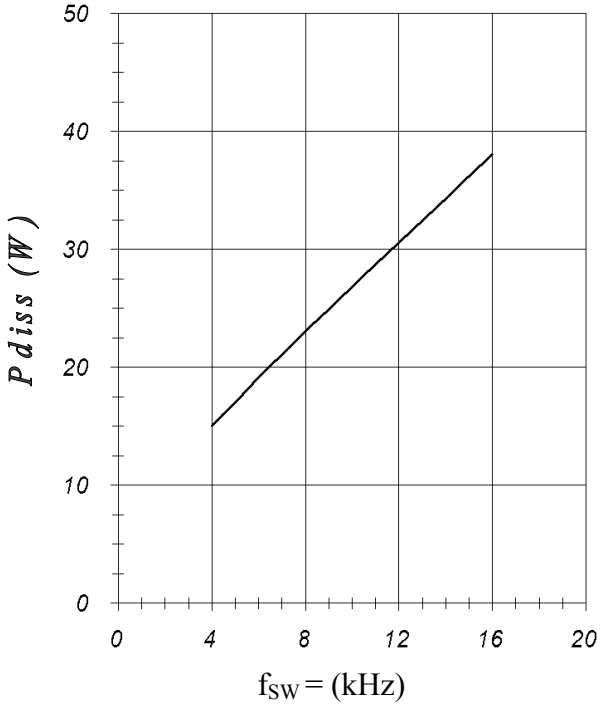


Fig. PD2 – Total Dissipated Power vs. f_{SW}
$Iout_{RMS}$ = 6A, V_{DC} = 300V, T_C = 55ºC

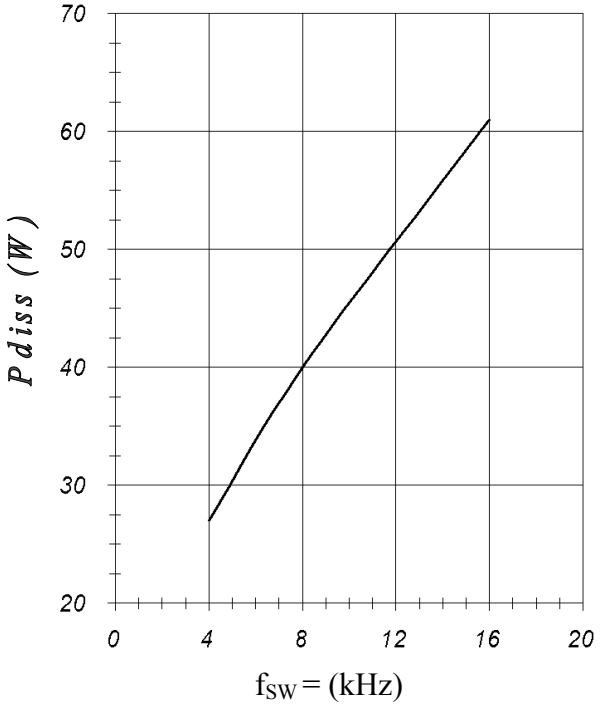


Fig. PD3 – Total Dissipated Power vs. f_{SW}
$Iout_{RMS}$ = 14A, V_{DC} = 300V, T_C = 40ºC

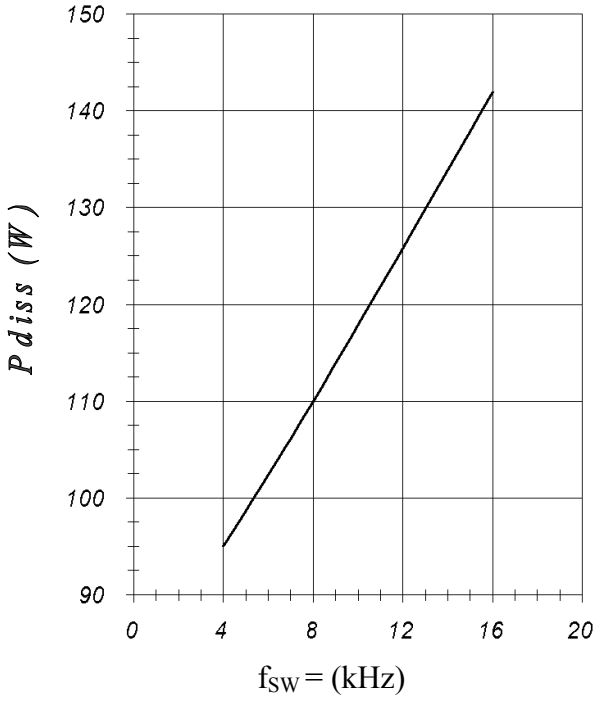
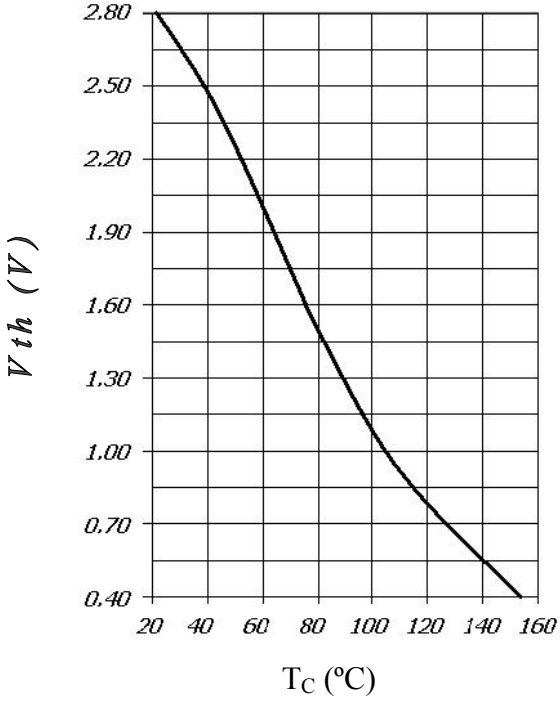
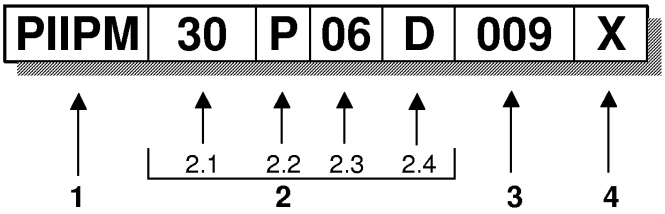


Fig. TF1 – Thermal Sensor Voltage Feedback vs. Base-plate Temperature



International
IOR Rectifier

PIIPM family part number identification



1- Device type (**P**rogrammable **I**solated **I**ntelligent **P**ower **M**odule)

2- Power package code

2.1- Current rating Code [A]

2.2- Sensing Resistors configuration

- P = on 3 phases
- Q = on 2 phases (*)
- R = on 1 phase (only for Matrix config.) (*)
- E = on 3 emitters
- F = on 2 emitters (*)
- G = on 1 emitter (*)

2.3- Voltage rating Code [V/100]

- 06 = 600V
- 12 = 1200V

2.4- Power Module configuration code

- A = Bridge brake (*)
- B = Inverter
- C = Inverter + brake
- D = BBI (Bridge Brake Inverter)
- M = Matrix (*)

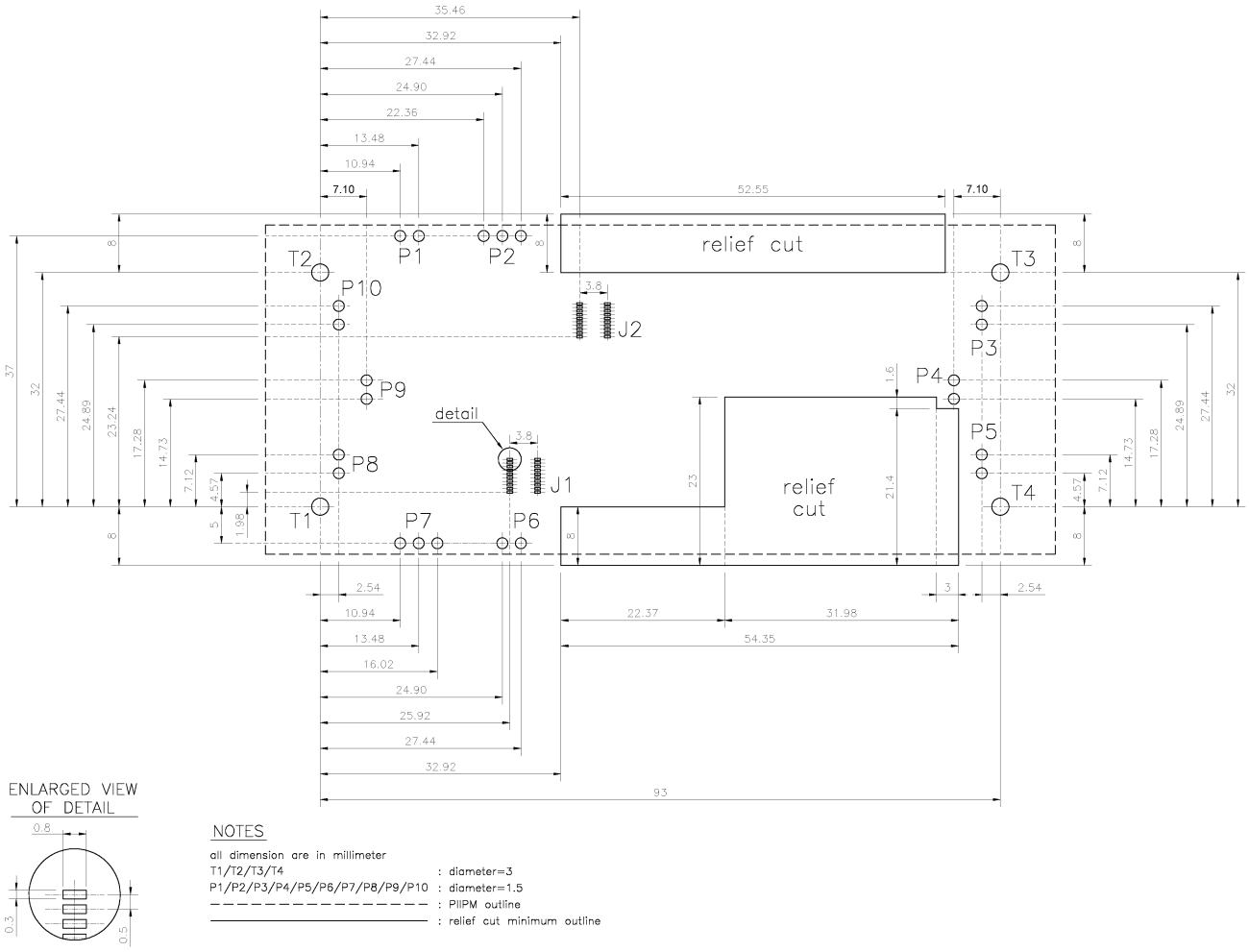
3- EDB configuration code — See detailed Block Diagram

4- Status code

- X = Sample (product with pre-qualification approval) Mating connectors included in the box
- blank = Fully qualified product

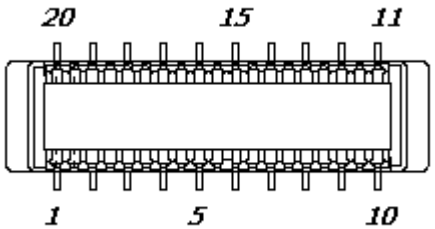
note: *= contact factory for availability

Top board suggested footprint
(top view)



RS485 and JTAG Connectors
Top view

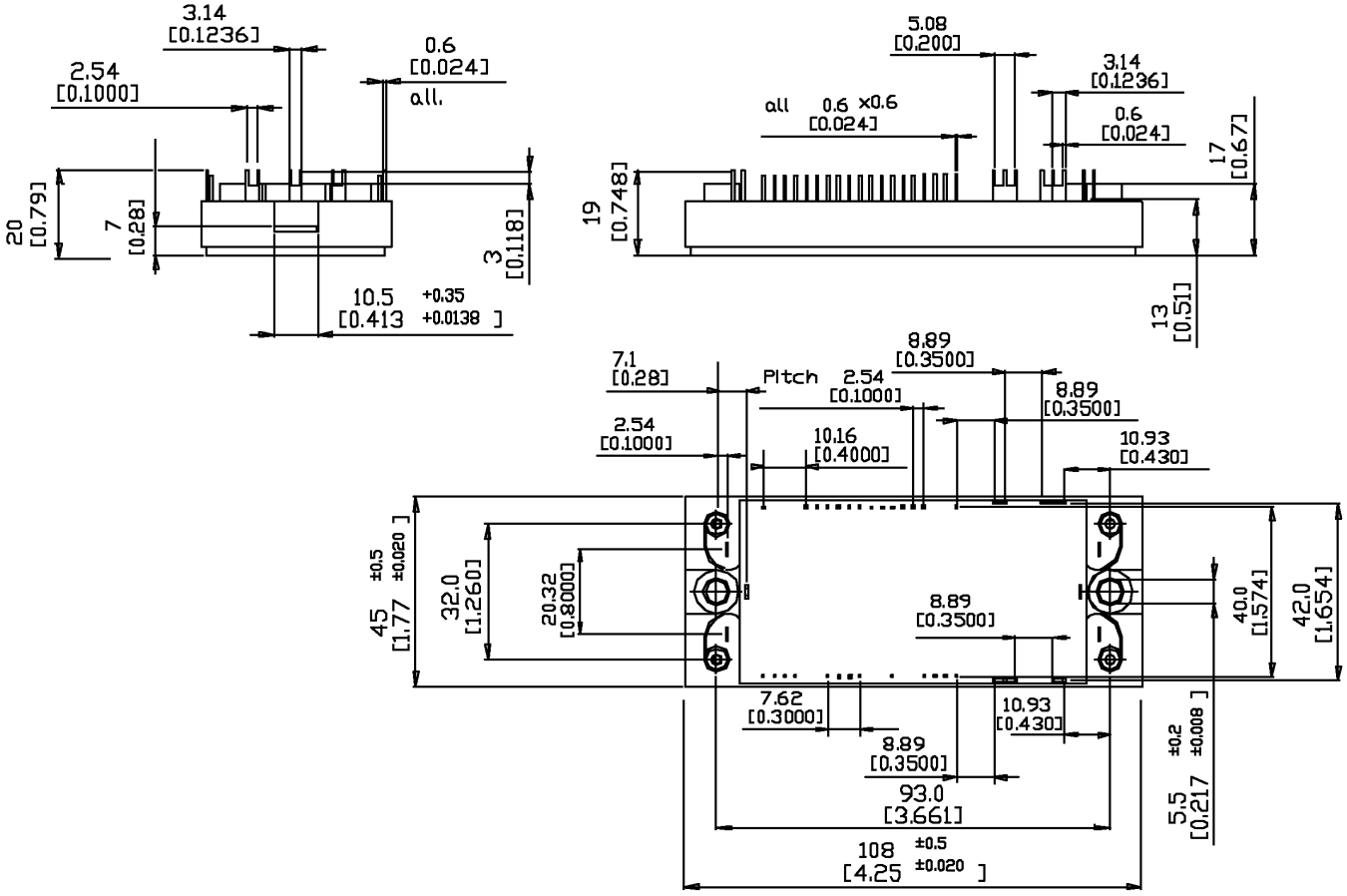
These connectors do not have any orientation tag; please check their Pin 1 position on Power Module Frame Pins Mapping before inserting mate part.



Molex 53916-0204
mates with 54167-0208 or 52991-0208

International
IOR Rectifier

PIIPM30P06D009 case outline and dimensions



Data and specifications subject to change without notice
This product has been designed and qualified for Industrial Level.
Qualification Standards can be found on IR's Web Site.

International
IOR Rectifier

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