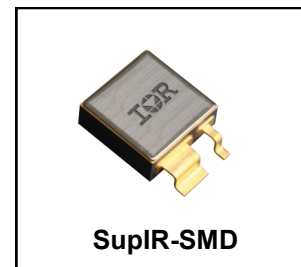


**RADIATION HARDENED
POWER MOSFET
SURFACE MOUNT (SupIR-SMD)**

**500V, N-CHANNEL
RAD-Hard HEXFET TECHNOLOGY**

Product Summary

Part Number	Radiation Level	RDS(on)	I _D
IRHNS7460SE	100 kRads (Si)	0.32Ω	20A



Description

IR HiRel RAD-Hard HEXFET technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low R_{ds(on)} and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Ultra Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Light Weight
- Surface Mount
- ESD Rating: Class 3B per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units
I _{D1} @ V _{GS} = 12V, T _C = 25°C	Continuous Drain Current	20	A
I _{D2} @ V _{GS} = 12V, T _C = 100°C	Continuous Drain Current	12	
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	80	
P _D @ T _C = 25°C	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.4	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy ②	500	mJ
I _{AR}	Avalanche Current ①	20	A
E _{AR}	Repetitive Avalanche Energy ①	30	mJ
dv/dt	Peak Diode Recovery dv/dt ③	3.8	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5s)	
	Weight	3.3 (Typical)	

For Footnotes, refer to the page 2.

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	500	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.66	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.32	Ω	V _{GS} = 12V, I _{D2} = 12A ④
		—	—	0.36		V _{GS} = 12V, I _{D1} = 20A ④
V _{GS(th)}	Gate Threshold Voltage	2.5	—	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
G _{fs}	Forward Transconductance	6.0	—	—	S	V _{DS} = 15V, I _{D2} = 12A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	50	μA	V _{DS} = 400V, V _{GS} = 0V
		—	—	250		V _{DS} = 400V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _G	Total Gate Charge	—	—	220	nC	I _{D1} = 20A
Q _{GS}	Gate-to-Source Charge	—	—	50		V _{DS} = 250V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	110		V _{GS} = 12V
t _{d(on)}	Turn-On Delay Time	—	—	35	ns	V _{DD} = 250V
t _r	Rise Time	—	—	100		I _{D1} = 20A
t _{d(off)}	Turn-Off Delay Time	—	—	100		R _G = 2.35Ω
t _f	Fall Time	—	—	100		V _{GS} = 12V
L _S + L _D	Total Inductance	—	4.0	—	nH	Measured from center of Drain pad to center of Source pad
C _{iss}	Input Capacitance	—	3500	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	730	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	260	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	20	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	80		
V _{SD}	Diode Forward Voltage	—	—	1.8	V	T _J = 25°C, I _S = 20A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	800	ns	T _J = 25°C, I _F = 20A, V _{DD} ≤ 50V
Q _{rr}	Reverse Recovery Charge	—	—	16	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	0.42	°C/W
R _{θJ-PCB}	Junction-to-PC Board (Soldered to 2" sq.inch copper clad board)	—	1.6	—	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = 50V, starting T_J = 25°C, L = 2.5mH, Peak I_L = 20A, V_{GS} = 12V
- ③ I_{SD} ≤ 20A, di/dt ≤ 120A/μs, V_{DD} ≤ 500V, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V_{GS} Bias. 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V_{DS} Bias. 400 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	100 kRads (Si)		Units	Test Conditions
		Min.	Max.		
BV _{DSS}	Drain-to-Source Breakdown Voltage	500	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.5	V	V _{DS} = V _{GS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	nA	V _{GS} = -20V
I _{DSS}	Zero Gate Voltage Drain Current	—	50	μA	V _{DS} = 400V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.32	Ω	V _{GS} = 12V, I _{D2} = 12A
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (SupIR-SMD)	—	0.32	Ω	V _{GS} = 12V, I _{D2} = 12A
V _{SD}	Diode Forward Voltage	—	1.8	V	V _{GS} = 0V, I _S = 20A

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)				
				@ VGS = 0V	@ VGS = -5V	@ VGS = -10V	@ VGS = -15V	@ VGS = -20V
Cu	28	285	43	375	375	375	375	375
Br	36.8	305	39	350	350	350	325	300
Ni	26.6	265	42	—	375	—	—	—

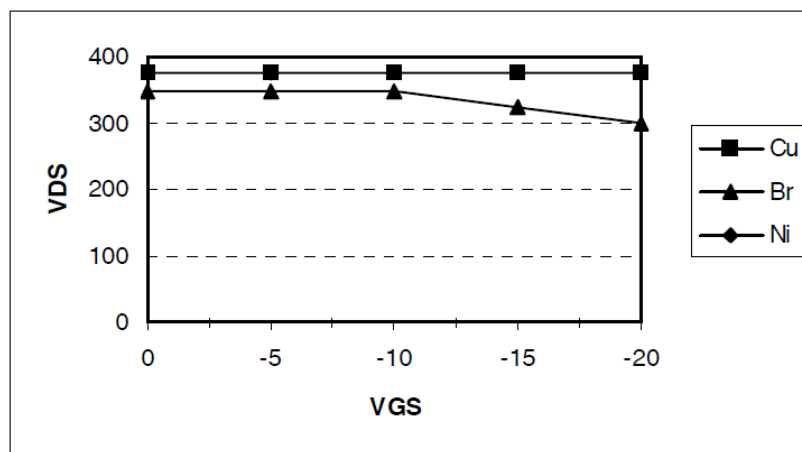


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

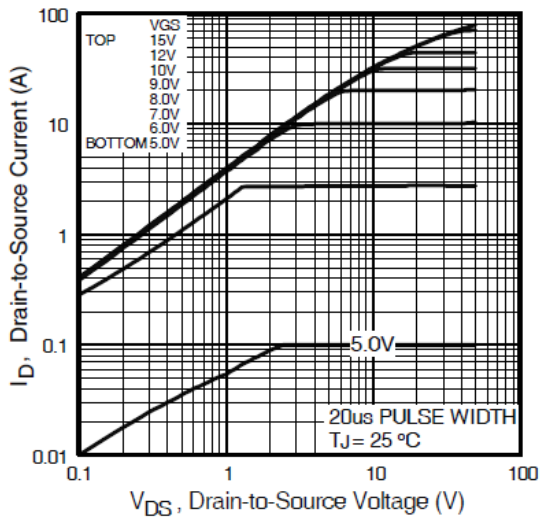


Fig 1. Typical Output Characteristics

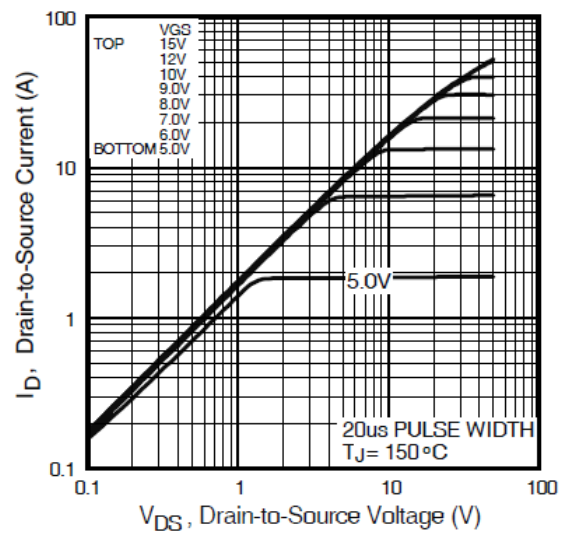


Fig 2. Typical Output Characteristics

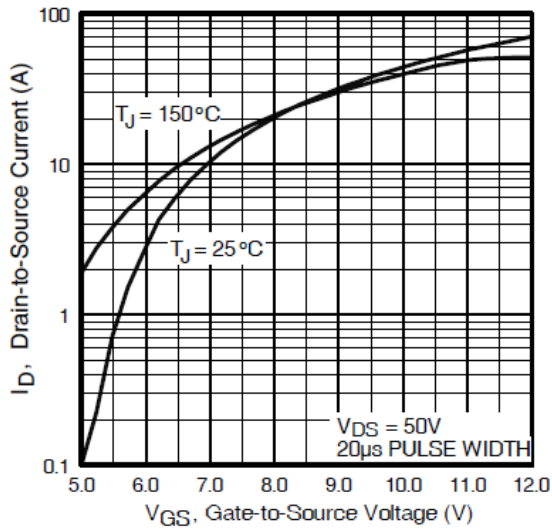


Fig 3. Typical Transfer Characteristics

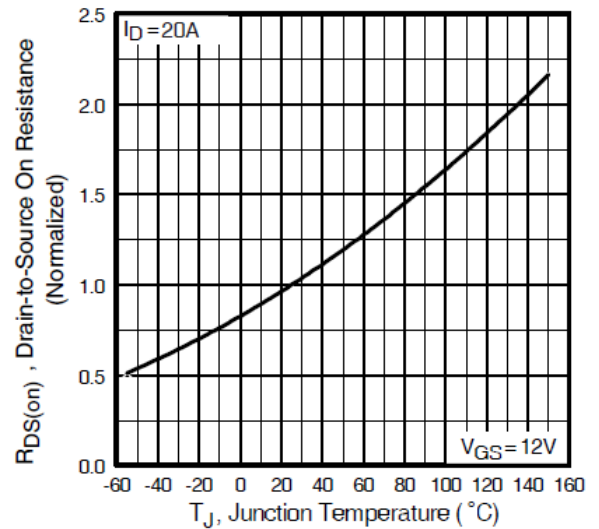


Fig 4. Normalized On-Resistance Vs. Temperature

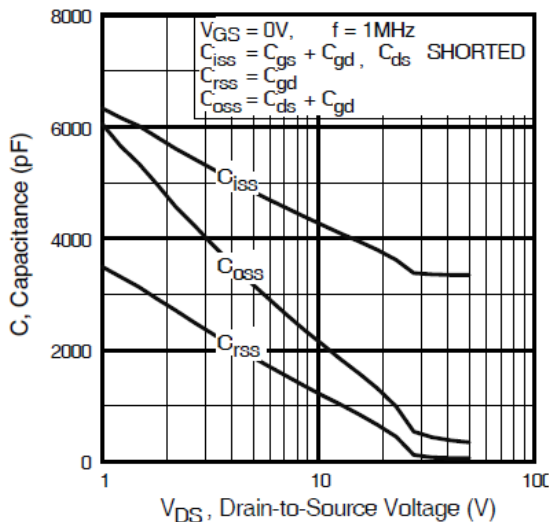


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

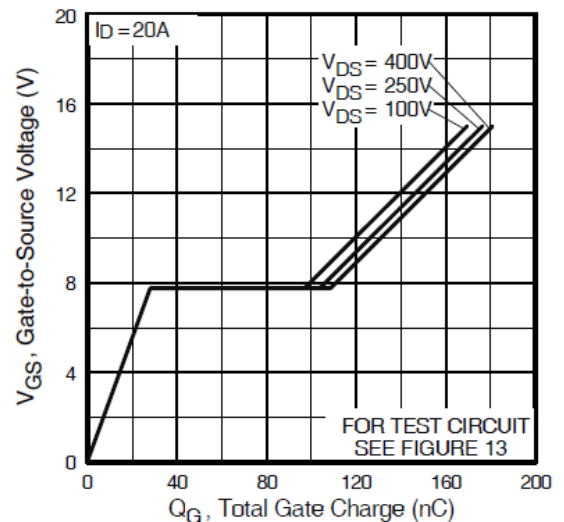


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

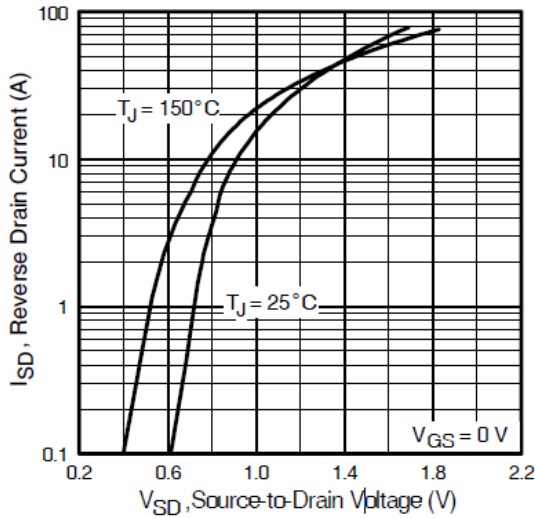


Fig 7. Typical Source-Drain Diode Forward Voltage

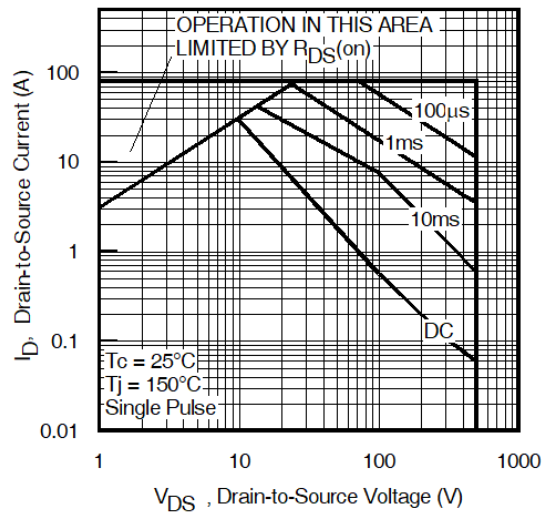


Fig 8. Maximum Safe Operating Area

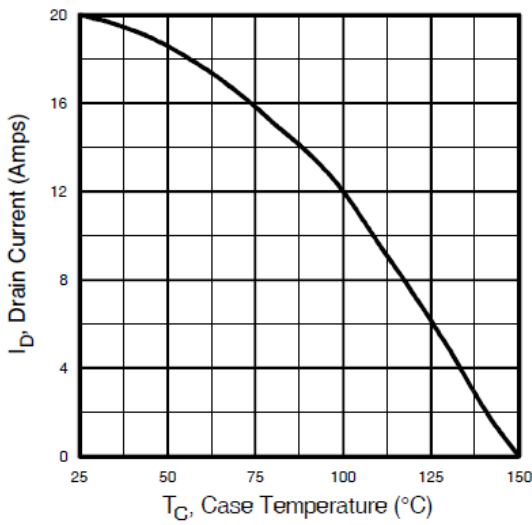


Fig 9. Maximum Drain Current Vs. Case Temperature

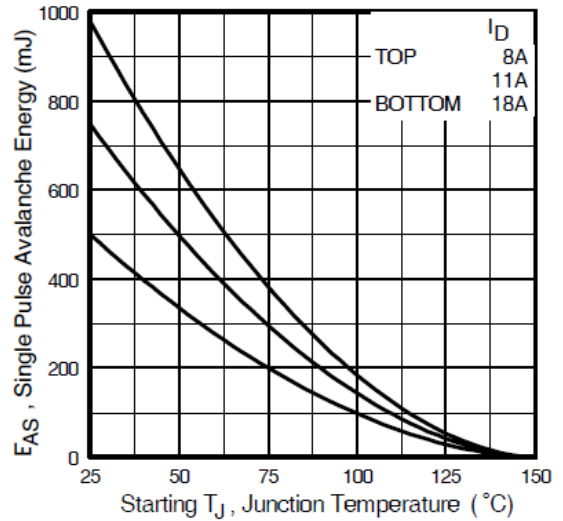


Fig 10. Maximum Avalanche Energy Vs. Drain Current

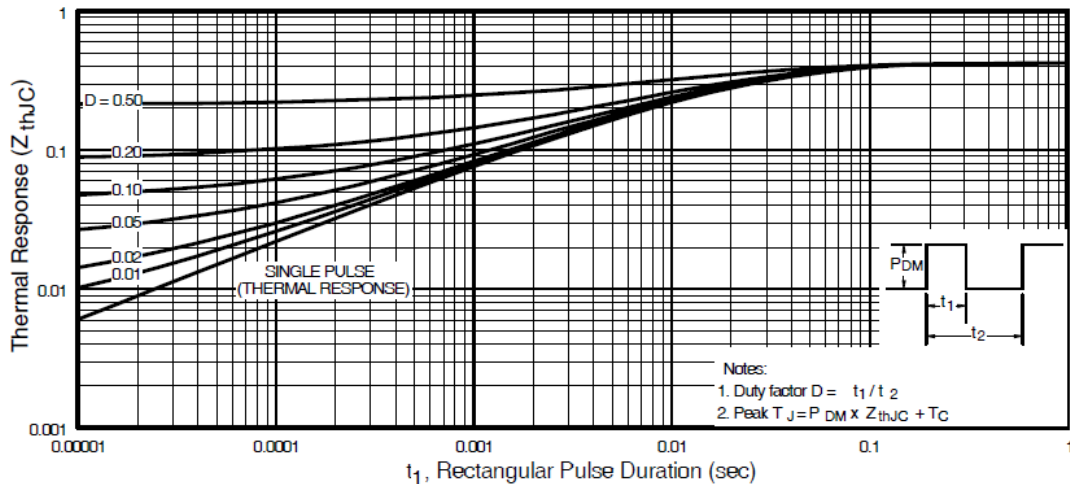


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

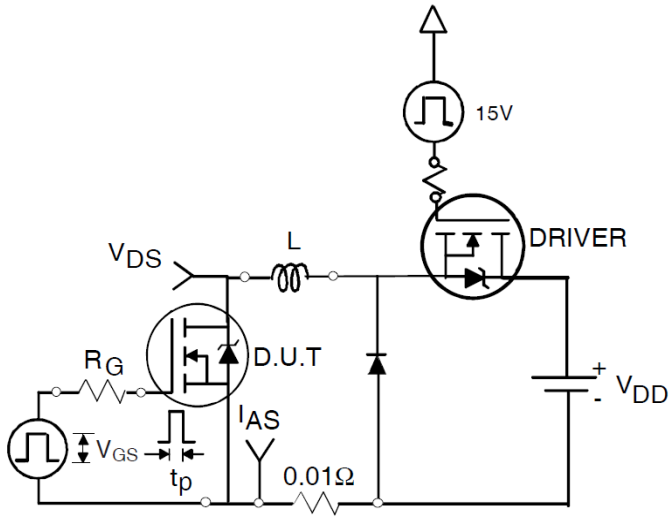


Fig 12a. Unclamped Inductive Test Circuit

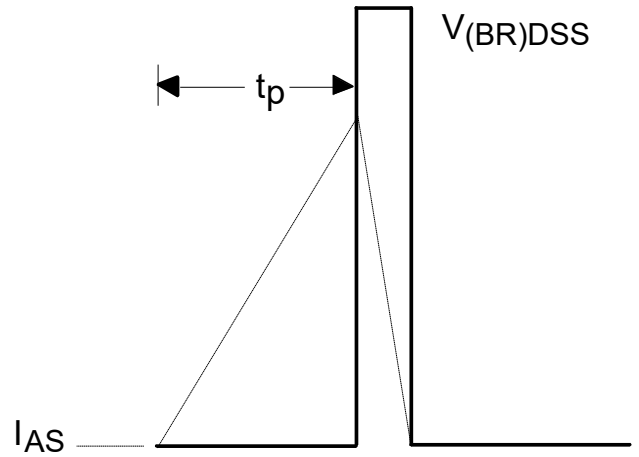


Fig 12b. Unclamped Inductive Waveforms

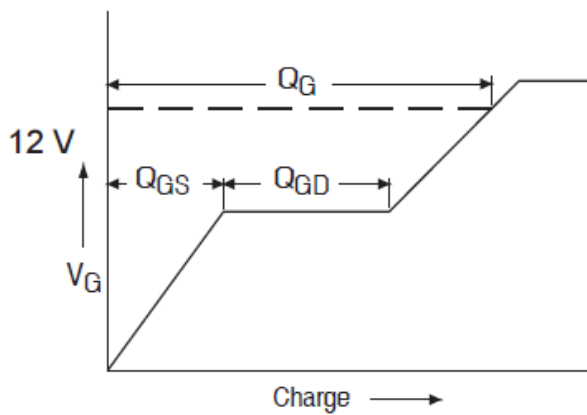


Fig 13a. Gate Charge Waveform

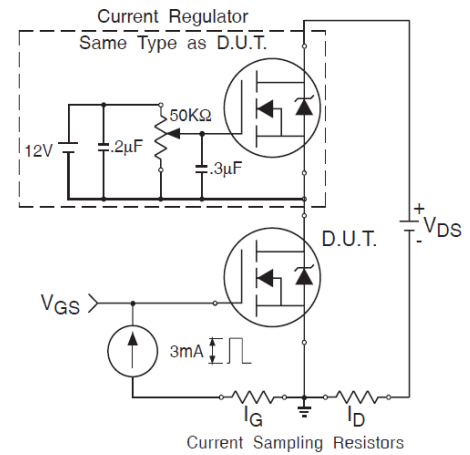


Fig 13b. Gate Charge Test Circuit

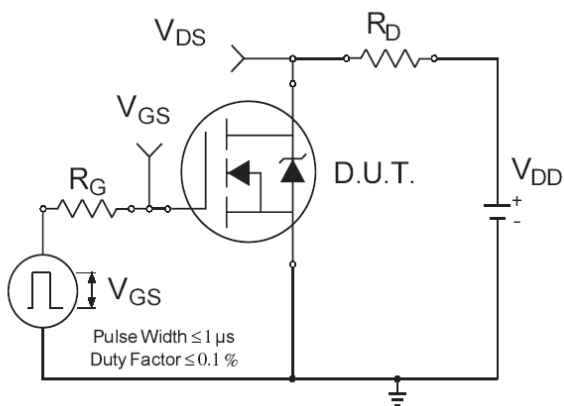


Fig 14a. Switching Time Test Circuit

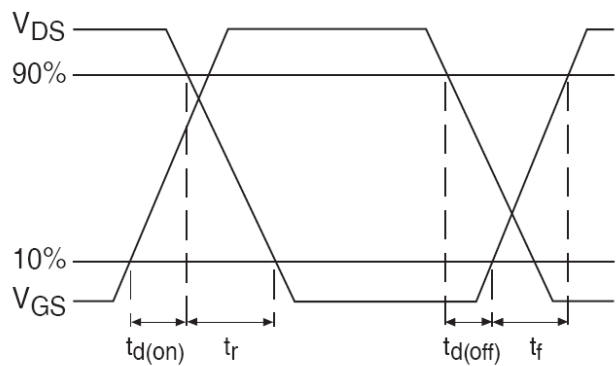
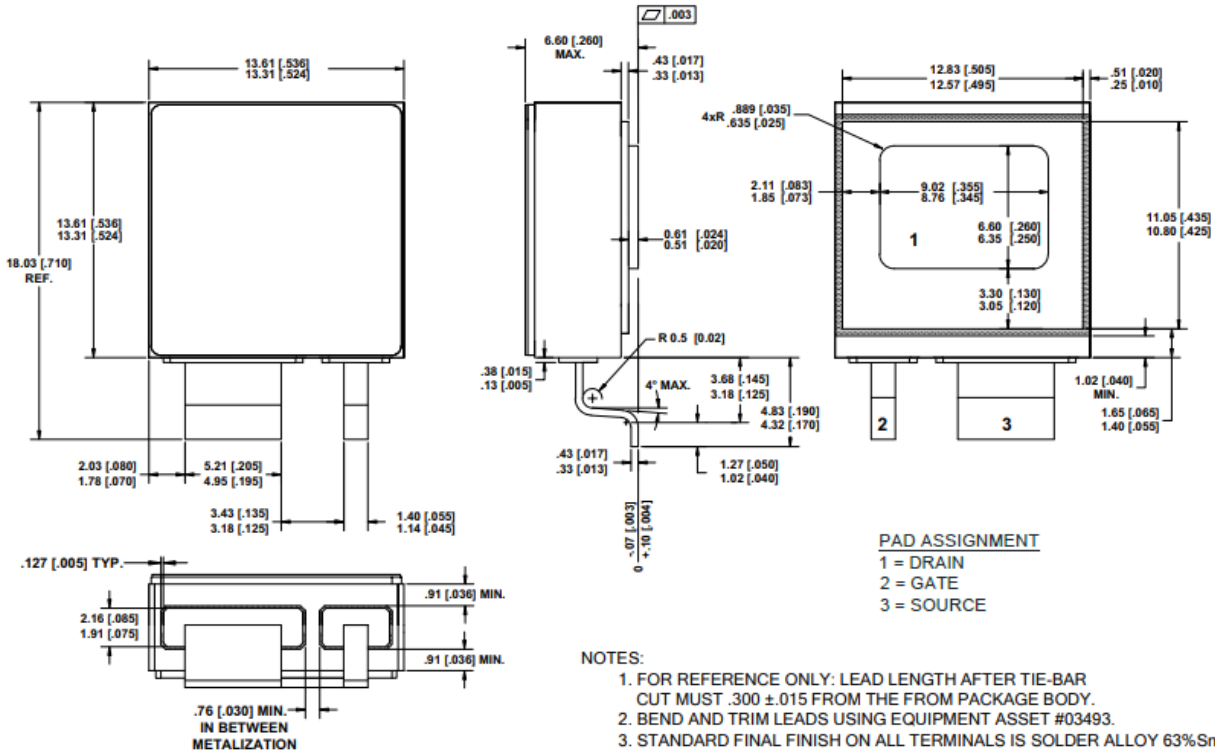


Fig 14b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: SupIR-SMD

Case Outline and Dimensions - SupIR-SMD

REV.	DESCRIPTION	ECN	DATE
E	INITIAL RELEASE	1120_08064	6-23-20



IOR HiRel
An Infineon Technologies Company

TITLE: SUPIR-SMD, OUTLINE	
DRAWING NO. D101003G-WEB	REV E

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