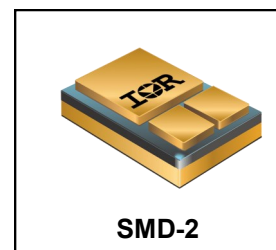


**RADIATION HARDENED**  
**POWER MOSFET**  
**SURFACE MOUNT (SMD-2)**
**200V, N-CHANNEL**  
**REF: MIL-PRF-19500/684**

**Product Summary**

Part Number	Radiation Level	RDS(on)	I <sub>D</sub>	QPL Part Number
IRHNA57260SE	100 kRads(Si)	0.038Ω	53.5A	JANSR2N7473U2


**Description**

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm<sup>2</sup>)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

**Features**

- Single Event Effect (SEE) Hardened
- Ultra Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight
- ESD Rating: Class 3B per MIL-STD-750, Method 1020

**Absolute Maximum Ratings**
**Pre-Irradiation**

Symbol	Parameter	Value	Units
I <sub>D1</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 25°C	Continuous Drain Current	53.5	A
I <sub>D2</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 100°C	Continuous Drain Current	34	
I <sub>DM</sub> @ T <sub>C</sub> = 25°C	Pulsed Drain Current ①	214	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	380	mJ
I <sub>AR</sub>	Avalanche Current ①	53.5	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	9.2	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 ( for 5s)	
	Weight	3.3 (Typical)	g

For Footnotes, refer to the page 2.

### Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.26	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.038	Ω	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 34A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.5	—	4.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0mA
G <sub>fs</sub>	Forward Transconductance	35	—	—	S	V <sub>DS</sub> = 15V, I <sub>D2</sub> = 34A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	10	μA	V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V
		—	—	25		V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>G</sub>	Total Gate Charge	—	—	155	nC	I <sub>D1</sub> = 53.5A
Q <sub>GS</sub>	Gate-to-Source Charge	—	—	45		V <sub>DS</sub> = 100V
Q <sub>GD</sub>	Gate-to-Drain ('Miller') Charge	—	—	75		V <sub>GS</sub> = 12V
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	35	ns	V <sub>DD</sub> = 100V
t <sub>r</sub>	Rise Time	—	—	125		I <sub>D1</sub> = 53.5A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	80		R <sub>G</sub> = 2.35Ω
t <sub>f</sub>	Fall Time	—	—	50		V <sub>GS</sub> = 12V
L <sub>s</sub> + L <sub>D</sub>	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad
C <sub>iss</sub>	Input Capacitance	—	6044	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	913	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	65	—		f = 1.0MHz

### Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	53.5	A	
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	214		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 53.5A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	450	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 53.5A, V <sub>DD</sub> ≤ 50V
Q <sub>rr</sub>	Reverse Recovery Charge	—	—	7.0	μC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	—	0.50	°C/W
R <sub>θPCB</sub>	Junction-to-PC Board (soldered to 1 inch square cu clad board)	—	1.6	—	

### Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V<sub>DD</sub> = 50V, starting T<sub>J</sub> = 25°C, L = 0.27mH, Peak I<sub>L</sub> = 53.5A, V<sub>GS</sub> = 12V
- ③ I<sub>SD</sub> ≤ 53.5A, di/dt ≤ 190A/μs, V<sub>DD</sub> ≤ 200V, T<sub>J</sub> ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V<sub>GS</sub> Bias. 12 volt V<sub>GS</sub> applied and V<sub>DS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V<sub>DS</sub> Bias. 160volt V<sub>DS</sub> applied and V<sub>GS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

## Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

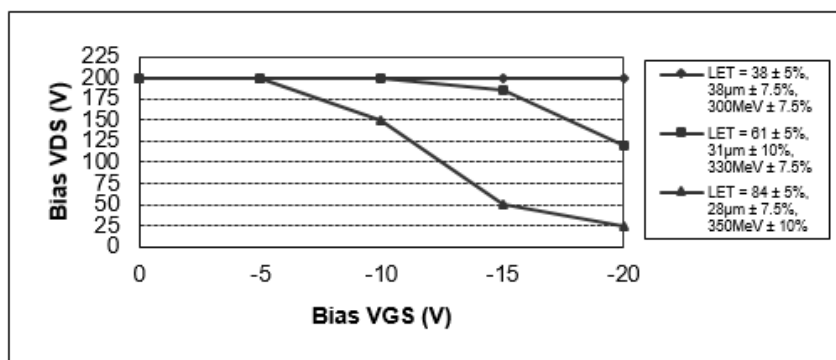
**Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

Symbol	Parameter	100 kRads (Si)		Units	Test Conditions
		Min.	Max.		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	200	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	4.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0mA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	-100	nA	V <sub>GS</sub> = -20V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	10	μA	V <sub>DS</sub> = 160V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.039	Ω	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 34A
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (SMD-2)	—	0.038	Ω	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 34A
V <sub>SD</sub>	Diode Forward Voltage ④	—	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 53.5A

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

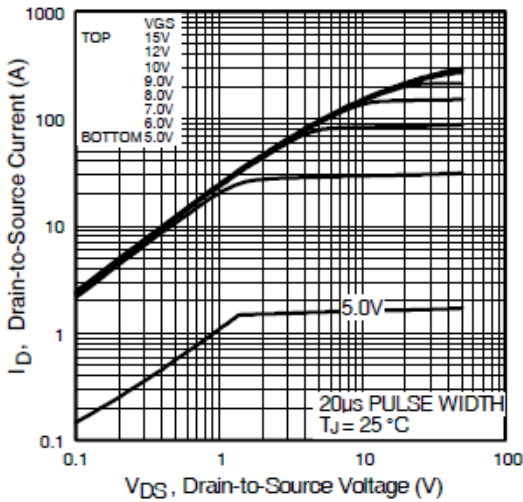
**Table 2. Typical Single Event Effect Safe Operating Area**

LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)				
			@ VGS = 0V	@ VGS = -5V	@ VGS = -10V	@ VGS = -15V	@ VGS = -20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	200	200	200	200	200
61 ± 5%	330 ± 7.5%	31 ± 10%	200	200	200	185	120
84 ± 5%	350 ± 10%	28 ± 7.5%	200	200	150	50	25

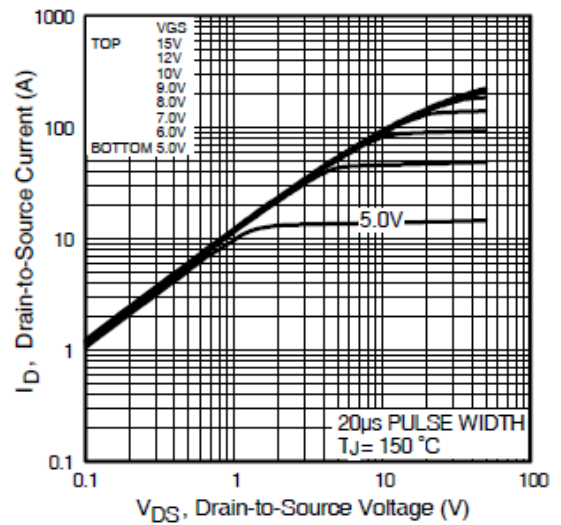


**Fig a.** Typical Single Event Effect, Safe Operating Area

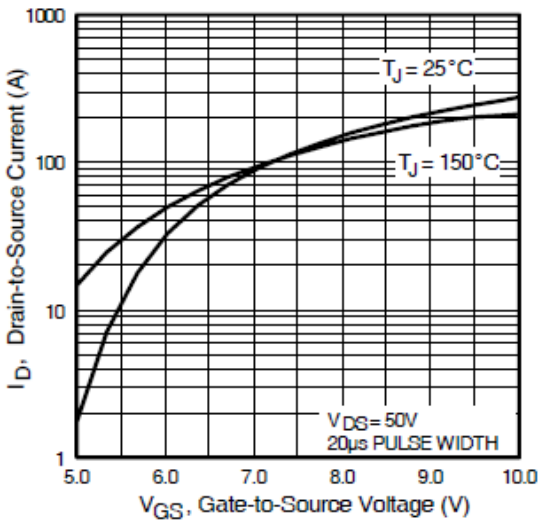
For Footnotes, refer to the page 2.



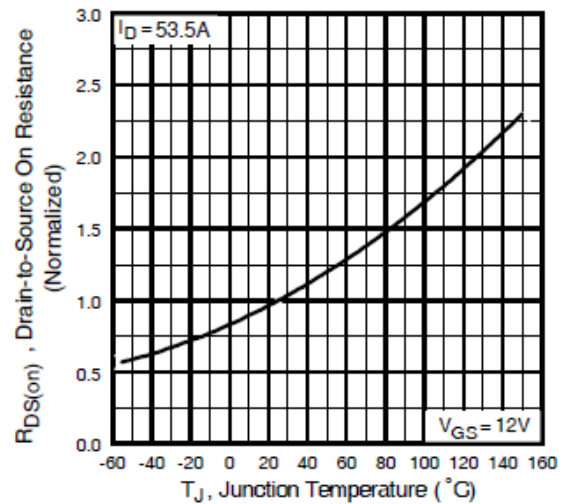
**Fig 1.** Typical Output Characteristics



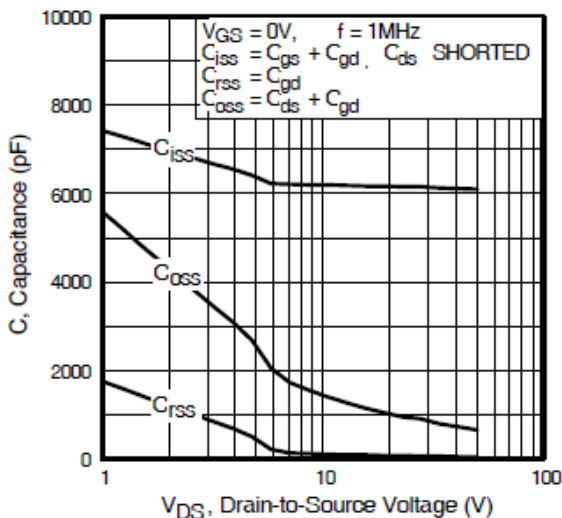
**Fig 2.** Typical Output Characteristics



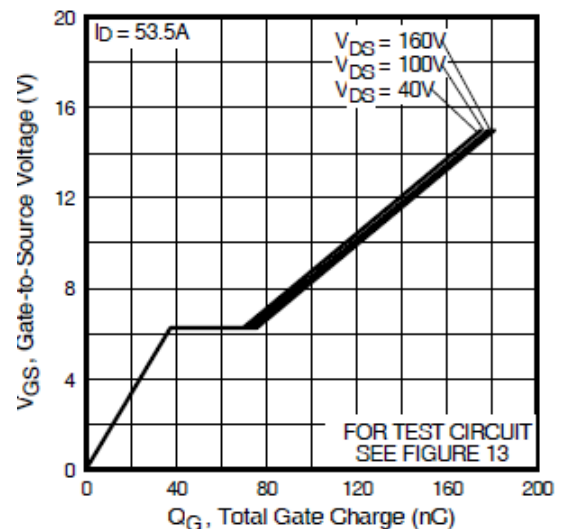
**Fig 3.** Typical Transfer Characteristics



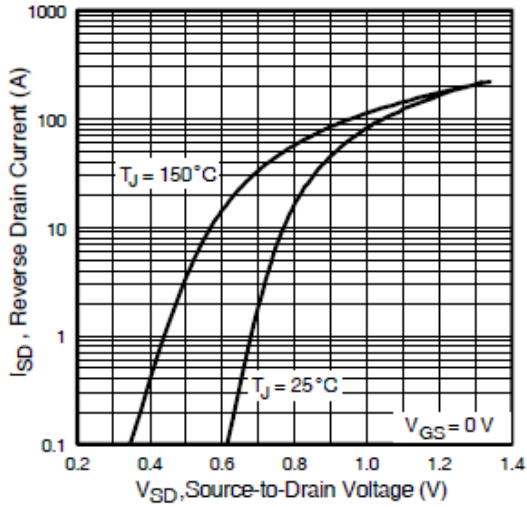
**Fig 4.** Normalized On-Resistance Vs. Temperature



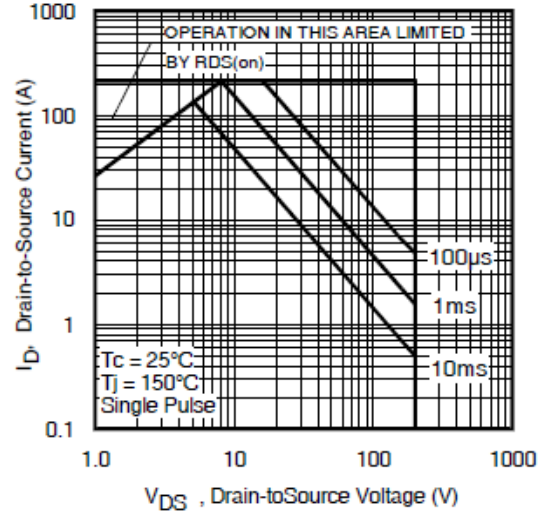
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



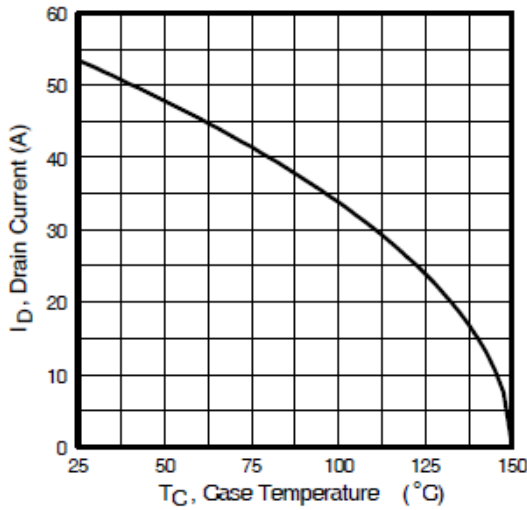
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



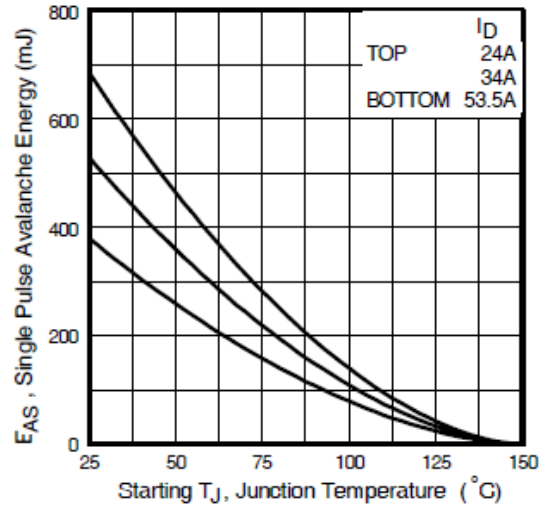
**Fig 7.** Typical Source-Drain Diode Forward Voltage



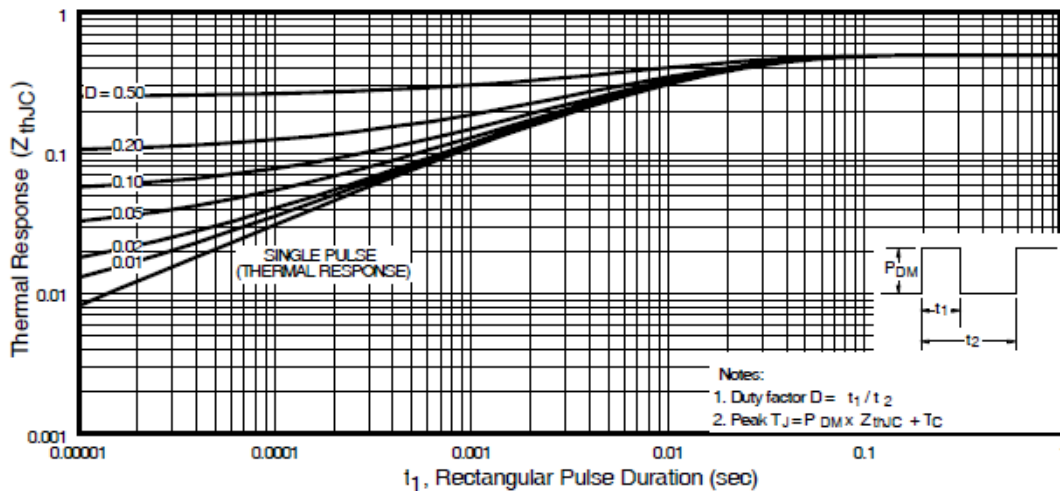
**Fig 8.** Maximum Safe Operating Area



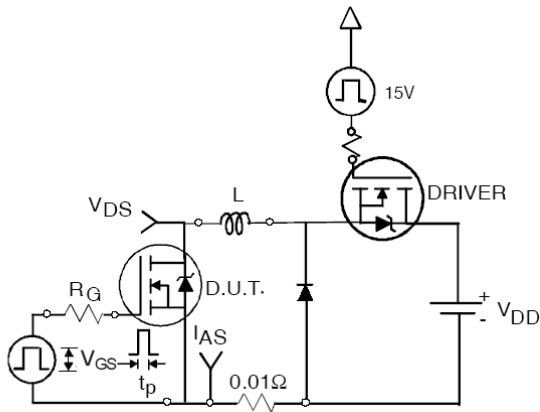
**Fig 9.** Maximum Drain Current Vs. Case Temperature



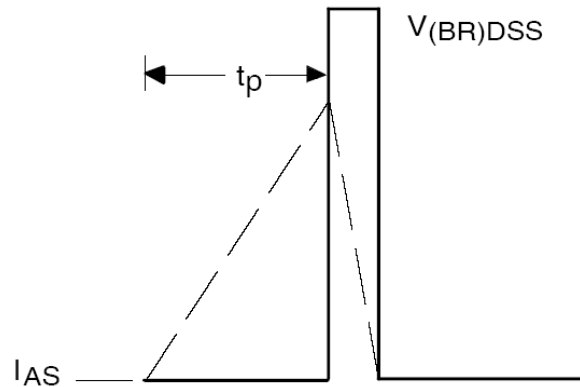
**Fig 10.** Maximum Avalanche Energy Vs. Drain Current



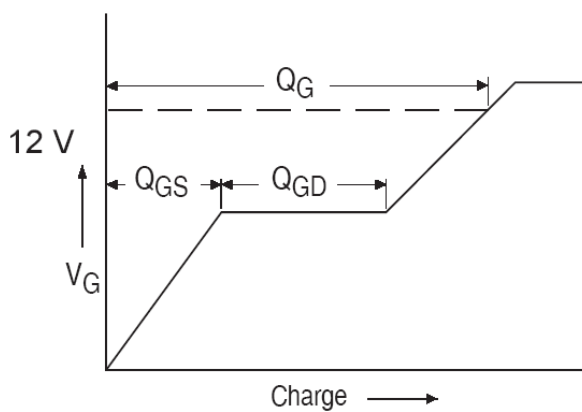
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



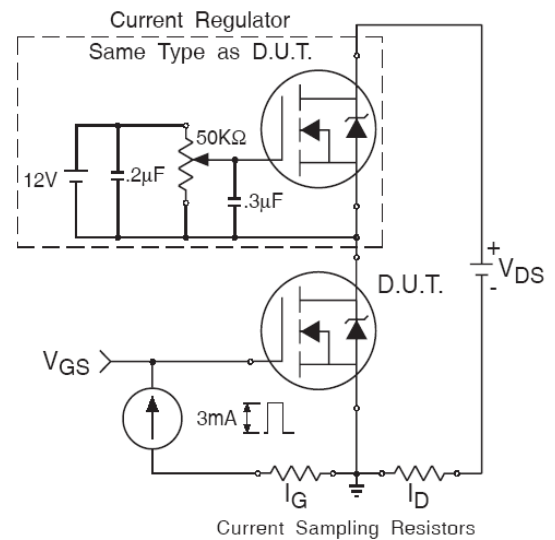
**Fig 12a.** Unclamped Inductive Test Circuit



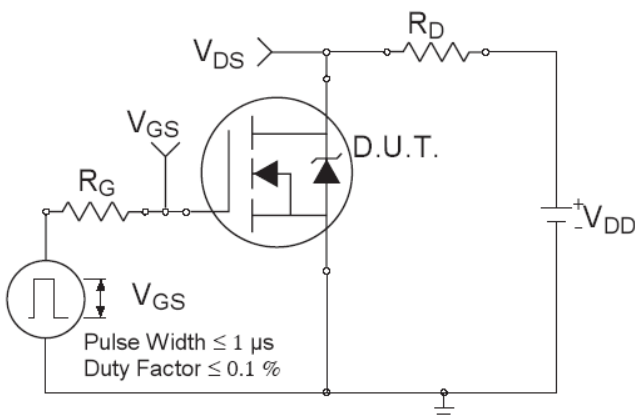
**Fig 12b.** Unclamped Inductive Wave-



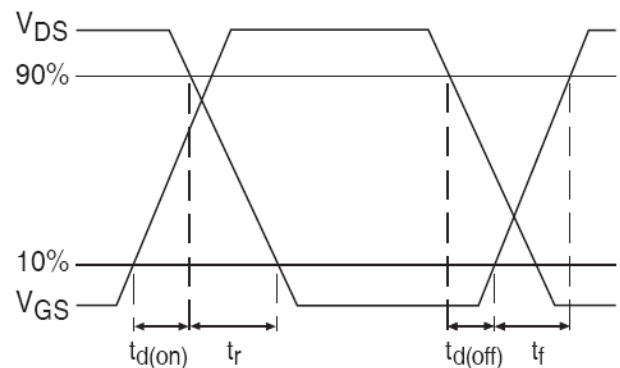
**Fig 13a.** Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



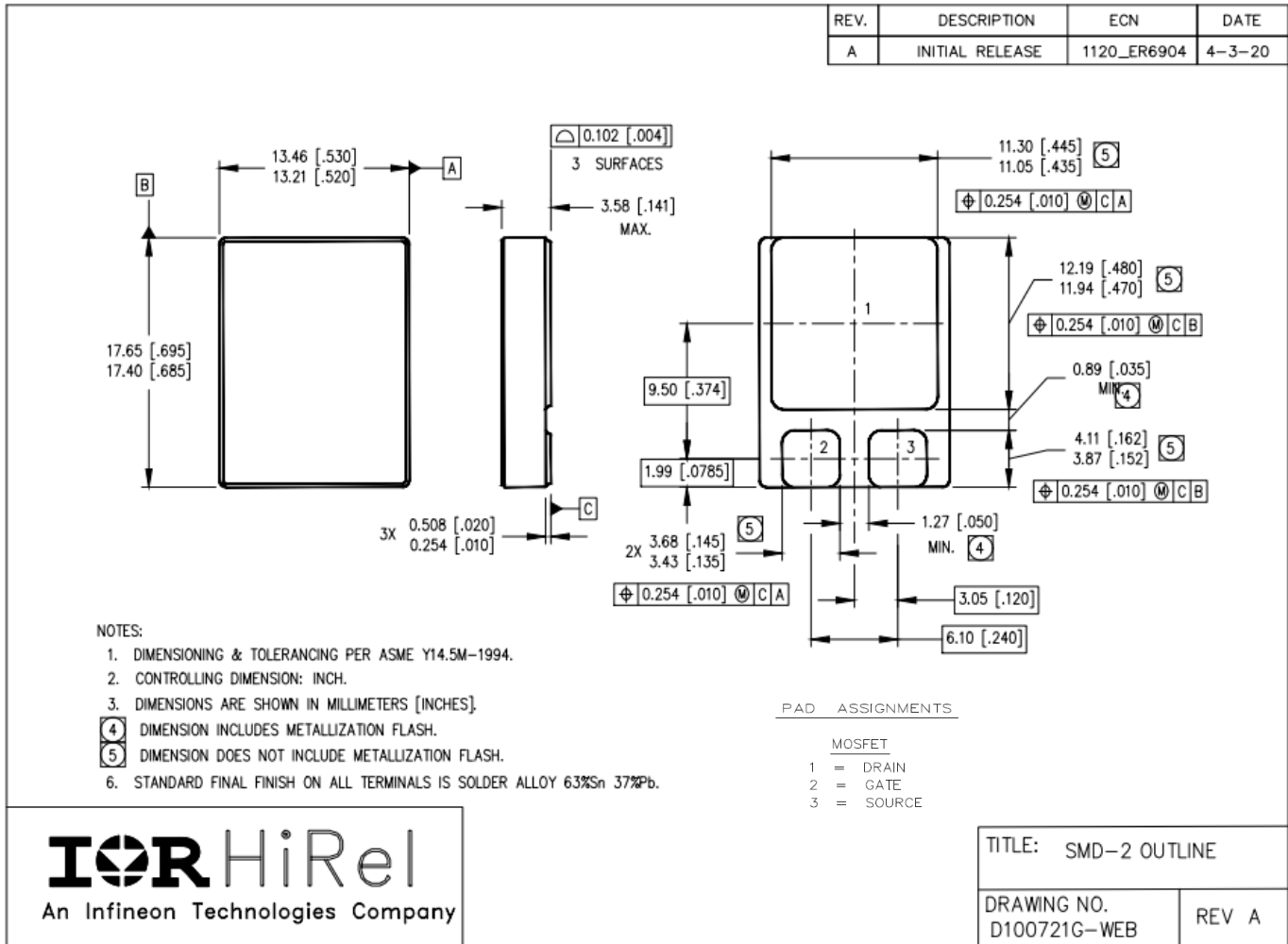
**Fig 14a.** Switching Time Test Circuit



**Fig 14b.** Switching Time Waveforms

Note: For the most updated package outline, please see the website: [SMD-2](#)

**Case Outline and Dimensions — SMD-2**



### **IMPORTANT NOTICE**

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