IRHLUC7670Z4

PD-97268E

Radiation Hardened Logic Level Power MOSFETs
Surface Mount (LCC-6)
60V Dual 1N & 1P, R7 Technology

Features

- 5V CMOS and TTL compatible
- Low $R_{DS(on)}$
- Single event effect (SEE) hardened
- Fast switching
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Light weight
- Surface mount
- ESD rating: Class 0B per MIL-STD-750, Method 1020

Potential Applications

- DC-DC converter
- Motor drives

Product Summary

- **BV_{DSS}:** ± 60V
- **I_D:** 0.89A (N-Ch), -0.65A (P-Ch)
- **$R_{DS(on),\,max}$:** 0.75Ω (N-Ch), 1.6Ω (P-Ch)
- **$Q_{G,\,max}$:** 3.6nC (N-Ch), 3.6nC (P-Ch)

LCC-6

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel R7 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity. The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHLUC7670Z4	LCC-6	COTS	100 krad(Si)
IRHLUC7670Z4SCS	LCC-6	S-Level	100 krad(Si)
IRHLUC7630Z4	LCC-6	COTS	300 krad(Si)

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	N-Channel	P-Channel	Unit
I_{D1} @ V_{GS} = ±4.5V, T_C = 25°C	Continuous Drain Current	0.89	-0.65	A
I_{D2} @ V_{GS} = ±4.5V, T_C = 100°C	Continuous Drain Current	0.56	-0.41	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	3.56	-2.6	A
P_D @ T_C = 25°C	Maximum Power Dissipation	1.0	1.0	W
	Linear Derating Factor	0.01	0.01	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	± 10	V
E_{AS}	Single Pulse Avalanche Energy [2],[3]	20	34	mJ
I_{AR}	Avalanche Current [1]	0.89	-0.65	A
E_{AR}	Repetitive Avalanche Energy [1]	0.1	0.1	mJ
dv/dt	Peak Diode Reverse Recovery [4],[5]	4.7	-5.6	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150		°C
	Lead Temperature	300 (for 5s)		
	Weight	0.2 (Typical)		g

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] V_{DD} = 25V, starting T_J = 25°C, L = 50.4mH, Peak I_L = 0.89A, V_{GS} = 10V

[3] V_{DD} = -25V, starting T_J = 25°C, L = 161mH, Peak I_L = -0.65A, V_{GS} = -10V

[4] $I_{SD} \leq$ 0.89A, di/dt ≤ 200A/µs, $V_{DD} \leq$ 60V, $T_J \leq$ 150°C

[5] $I_{SD} \leq$ -0.65A, di/dt ≤ -150A/µs, $V_{DD} \leq$ -60V, $T_J \leq$ 150°C

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation-N channel)

Table 3 Static and Dynamic Electrical Characteristic @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.07	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.75	Ω	V_{GS} = 4.5V, I_{D2} = 0.56A [1]
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-4.5	—	mV/°C	
Gfs	Forward Transconductance	1.1	—	—	S	V_{DS} = 15V, I_{D2} = -0.56A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	µA	V_{DS} = 48V, V_{GS} = 0V
		—	—	10		V_{DS} = 48V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 10V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -10V
Q_G	Total Gate Charge	—	—	3.6	nC	I_{D1} = 0.89A V_{DS} = 30V V_{GS} = 4.5V
Q_{GS}	Gate-to-Source Charge	—	—	1.5		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	1.8		
$t_{d(on)}$	Turn-On Delay Time	—	—	8.0	ns	I_{D1} = 0.89A ** V_{DD} = 30V R_G = 24Ω V_{GS} = 5.0V
t_r	Rise Time	—	—	15		
$t_{d(off)}$	Turn-Off Delay Time	—	—	30		
t_f	Fall Time	—	—	12		
L_s +L_D	Total Inductance	—	33	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	145	—	pF	V_{GS} = 0V V_{DS} = -25V f = 1.0MHz
C_{oss}	Output Capacitance	—	43	—		
C_{rss}	Reverse Transfer Capacitance	—	2.5	—		
R_G	Gate Resistance	—	9.5	—	Ω	f = 1.0MHz, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Electrical Characteristics (Pre-Irradiation P-channel)

Table 4 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	—	V	V_{GS} = 0V, I_D = -250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.06	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	1.6	Ω	V_{GS} = -4.5V, I_{D2} = -0.41A [1]
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-2.0	V	V_{DS} = V_{GS}, I_D = -250µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	3.6	—	mV/°C	
Gfs	Forward Transconductance	0.6	—	—	S	V_{DS} = -15V, I_{D2} = -0.41A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-1.0	µA	V_{DS} = -48V, V_{GS} = 0V
		—	—	-20		V_{DS} = -48V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = -10V
	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 10V
Q_G	Total Gate Charge	—	—	3.6	nC	I_{D1} = -0.65A V_{DS} = -30V V_{GS} = -4.5V
Q_{GS}	Gate-to-Source Charge	—	—	1.5		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	1.8		
$t_{d(on)}$	Turn-On Delay Time	—	—	23	ns	I_{D1} = -0.65A ** V_{DD} = -30V R_G = 24Ω V_{GS} = -5.0V
t_r	Rise Time	—	—	22		
$t_{d(off)}$	Turn-Off Delay Time	—	—	32		
t_f	Fall Time	—	—	26		
L_s +L_D	Total Inductance	—	33	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	147	—	pF	V_{GS} = 0V V_{DS} = -25V f = 1.0MHz
C_{oss}	Output Capacitance	—	46	—		
C_{rss}	Reverse Transfer Capacitance	—	8.1	—		
R_G	Gate Resistance	—	52	—	Ω	f = 1.0MHz, open drain

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.3 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation N-channel)

Table 5 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	0.89	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	3.56	A	
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 0.89A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	—	65	ns	T_J = 25°C, I_F = 0.89A, V_{DD} ≤ 25V
Q_{rr}	Reverse Recovery Charge	—	—	67	nC	di/dt = 100A/µs [2]
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.4 Thermal Characteristics (N channel)

Table 6 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JA}$	Junction-to-Ambient	—	—	125	°C/W
$R_{\theta JL}$	Junction-to-Lead	—	—	40	

2.5 Radiation Characteristics (N channel)

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.5.1 Electrical Characteristics — Post Total Dose Irradiation (N channel)

Table 7 Electrical Characteristics @ T_J = 25°C, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 300 krad (Si) [5]		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	V	V_{GS} = 0V, I_D = 250µA
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V_{GS} = 10V
	Gate-to-Source Leakage Reverse	—	-100		V_{GS} = -10V
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	µA	V_{DS} = 48V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-39) [2]	—	0.65	Ω	V_{GS} = 4.5V, I_{D2} = 0.56A
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (LCC-6) [2]	—	0.75	Ω	V_{GS} = 4.5V, I_{D2} = 0.56A
V_{SD}	Diode Forward Voltage	—	1.2	V	V_{GS} = 0V, I_F = 0.89A

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

[3] Total Dose Irradiation with V_{GS} Bias. V_{GS} = 10V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[4] Total Dose Irradiation with V_{DS} Bias. V_{DS} = 48V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[5] Part numbers: IRHLUC7670Z4 and IRHLUC7630Z4

2.6 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation P-channel)

Table 8 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-0.65	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	-2.6	A	
V_{SD}	Diode Forward Voltage	—	—	-5.0	V	T_J = 25°C, I_S=-0.65A, V_{GS} = 0V [2]
t_{rr}	Reverse Recovery Time	—	—	35	ns	T_J = 25°C, I_F = -0.65A, V_{DD} ≤ -25V
Q_{rr}	Reverse Recovery Charge	—	—	9.8	nC	di/dt = -100A/µs [2]
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.7 Thermal Characteristics (P channel)

Table 9 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JA}$	Junction-to-Ambient	—	—	125	°C/W
$R_{\theta JL}$	Junction-to-Lead	—	—	40	

2.8 Radiation Characteristics (P channel)

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.8.1 Electrical Characteristics — Post Total Dose Irradiation (P channel)

Table 10 Electrical Characteristics @ T_J = 25°C, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	Up to 300 krad (Si) [5]		Unit	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	—	V	V_{GS} = 0V, I_D = -250µA
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-2.0	V	V_{DS} = V_{GS}, I_D = -250µA
I_{GSS}	Gate-to-Source Leakage Forward	—	-100	nA	V_{GS} = -10V
	Gate-to-Source Leakage Reverse	—	100		V_{GS} = 10V
I_{DSS}	Zero Gate Voltage Drain Current	—	-1.0	µA	V_{DS} = -48V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-39) [2]	—	1.4	Ω	V_{GS} = -4.5V, I_{D2} = -0.41A
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (LCC-6) [2]	—	1.6	Ω	V_{GS} = -4.5V, I_{D2} = -0.41A
V_{SD}	Diode Forward Voltage	—	-5.0	V	V_{GS} = 0V, I_F = -0.65A

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.

[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

[3] Total Dose Irradiation with V_{GS} Bias. V_{GS} = -10V applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[4] Total Dose Irradiation with V_{DS} Bias. V_{DS} = -48V applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

[5] Part numbers: IRHLUC7670Z4 and IRHLUC7630Z4

2.8.2 Single Event Effects — Safe Operating Area (N channel)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 11 Typical Single Event Effects Safe Operating Area

LET (MeV·cm²/mg)	Energy (MeV)	Range (µm)	V_{DS} (V)					
			V_{GS} = 0V	V_{GS} = -2V	V_{GS} = -3V	V_{GS} = -4V	V_{GS} = -5V	V_{GS} = -6V
38.1	358	43.9	60	60	60	60	60	60
60.9	659	54	60	60	60	60	60	—
90.7	1375	75.4	60	60	—	—	—	—

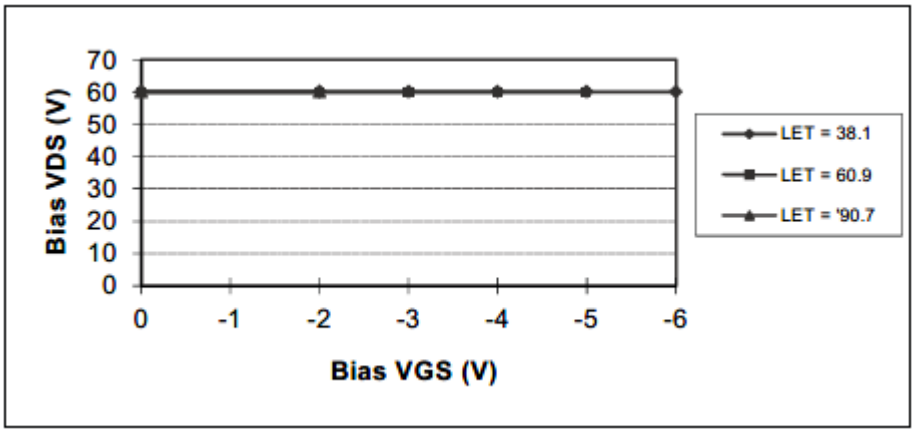


Figure 1 Typical Single Event Effect, Safe Operating Area

2.8.3 Single Event Effects — Safe Operating Area (P channel)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 12 Typical Single Event Effects Safe Operating Area

LET (MeV·cm²/mg)	Energy (MeV)	Range (µm)	V_{DS} (V)					
			V_{GS} = 0V	V_{GS} = 2V	V_{GS} = 4V	V_{GS} = 5V	V_{GS} = 6V	V_{GS} = 7V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	-60	-60	-60	-60	-60	-50
62 ± 5%	355 ± 7.5%	33 ± 7.5%	-60	-60	-60	-60	-60	—
85 ± 5%	380 ± 7.5%	29 ± 7.5%	-60	-60	-60	-60	—	—

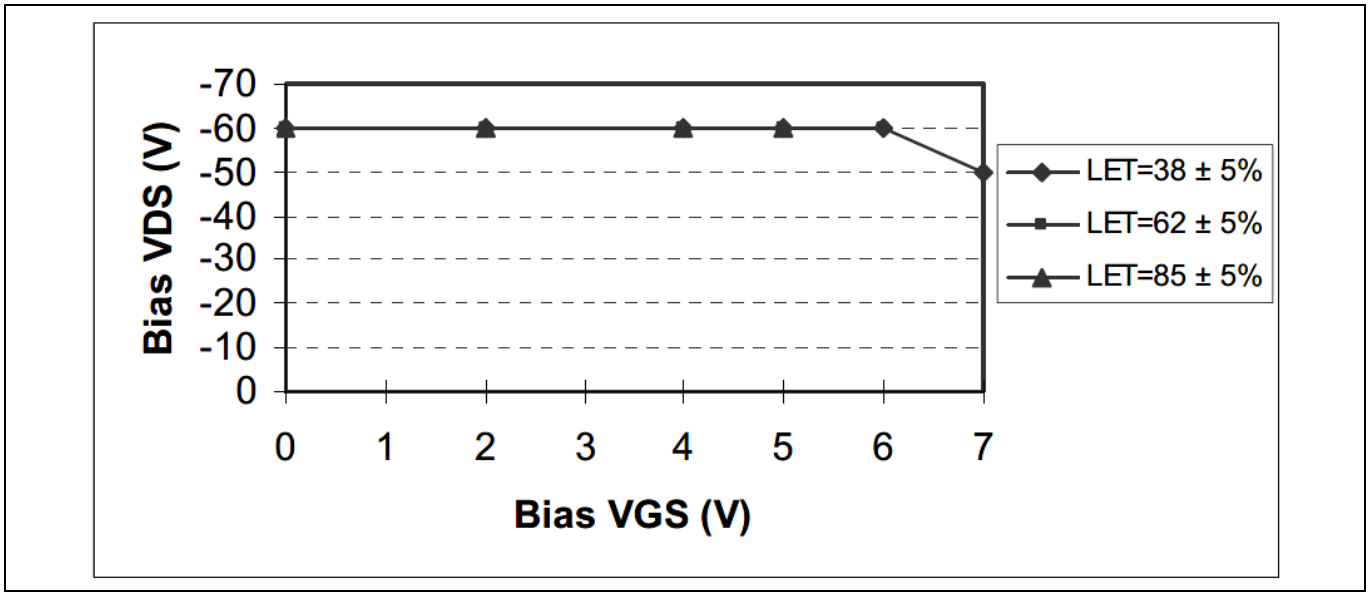


Figure 2 Worst Case Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-Irradiation N-channel)

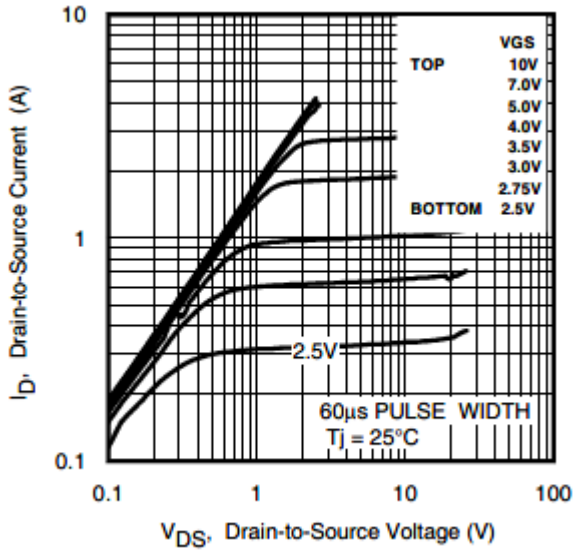


Figure 3 **Typical Output Characteristics**

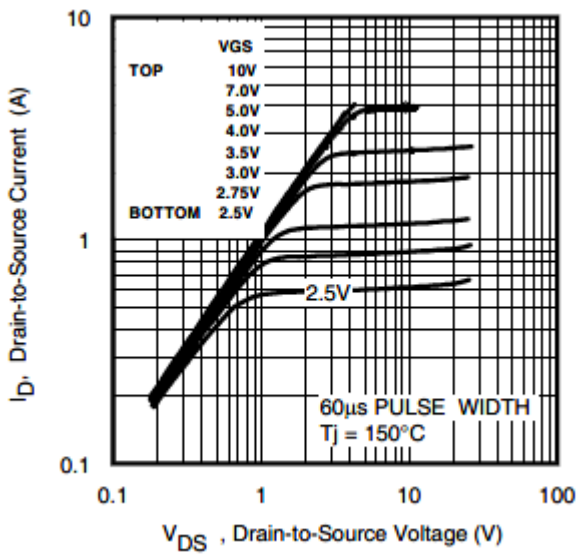


Figure 4 **Typical Output Characteristics**

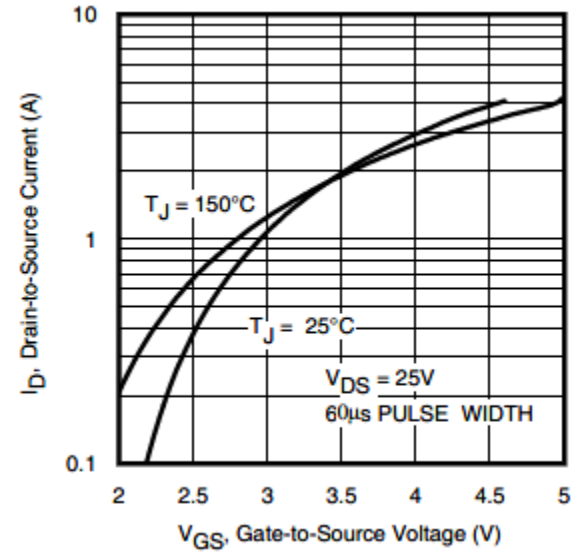


Figure 5 **Typical Transfer Characteristics**

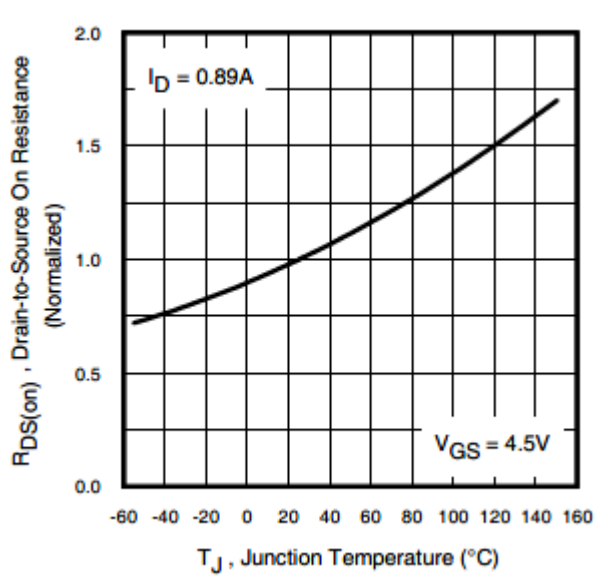


Figure 6 **Normalized On-Resistance Vs. Temperature**

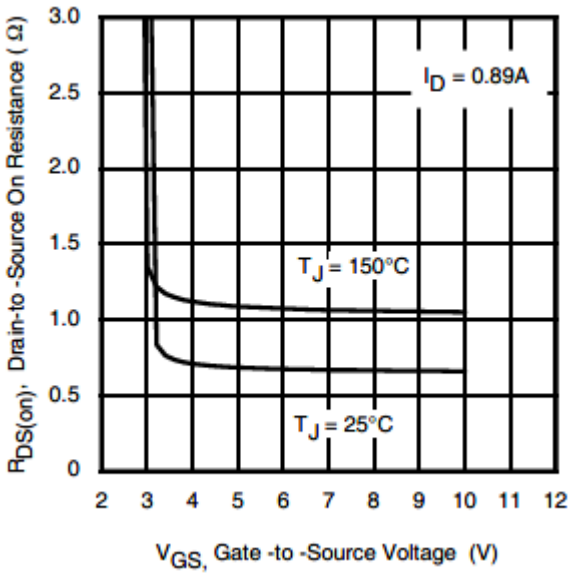


Figure 7 **Typical On-Resistance Vs. Gate Voltage**

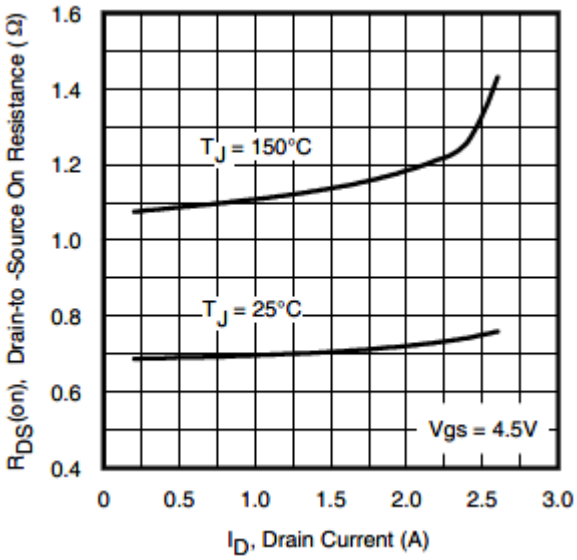


Figure 8 **Typical On-Resistance Vs. Drain Current**

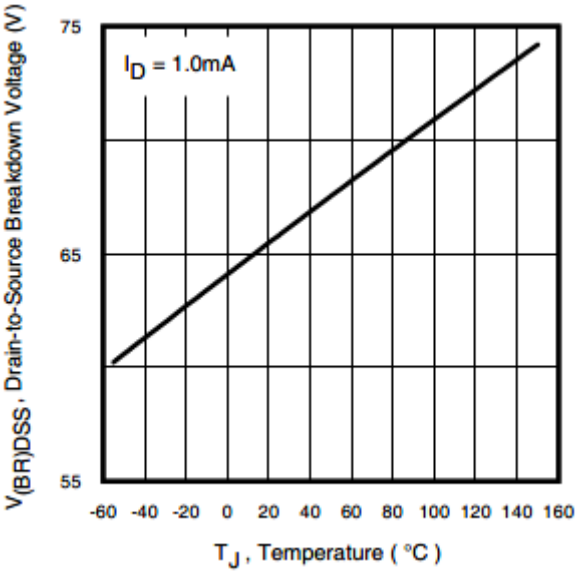


Figure 9 **Typical Drain-to-Source Breakdown Voltage Vs. Temperature**

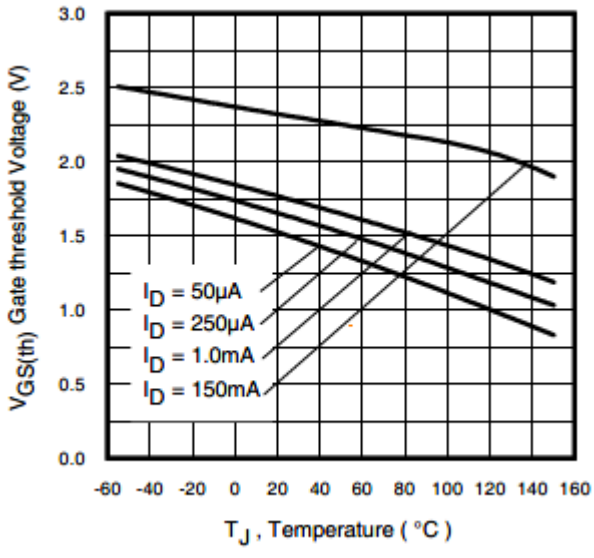


Figure 10 **Typical Threshold Voltage Vs. Temperature**

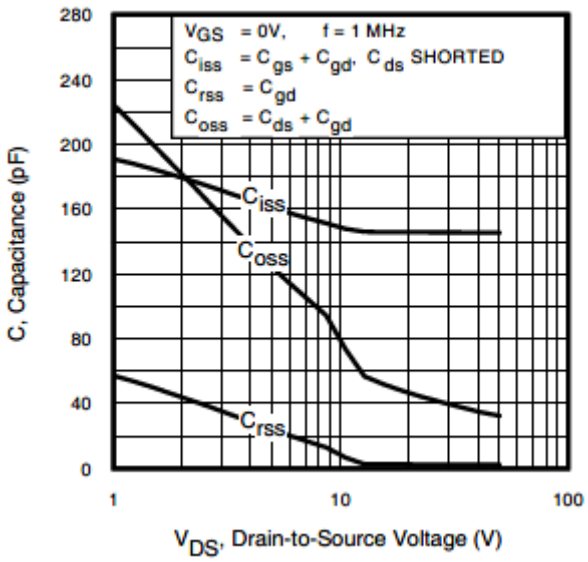


Figure 11 Typical Capacitance Vs. Drain-to-Source Voltage

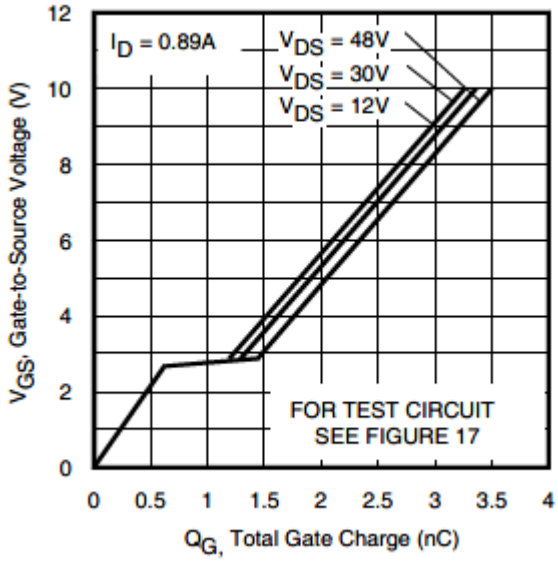


Figure 12 Gate-to-Source Voltage Vs. Typical Gate Charge

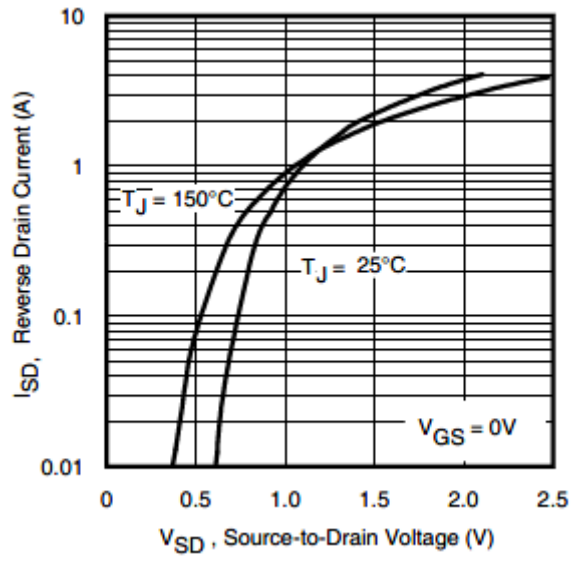


Figure 13 Typical Source-Drain Current Vs. Diode Forward Voltage

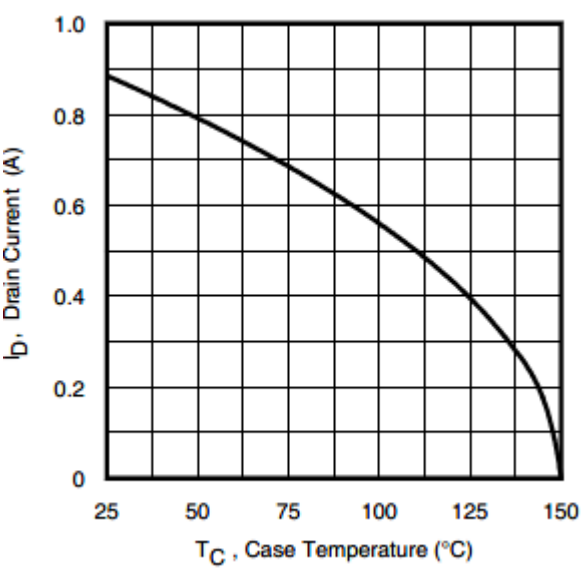


Figure 14 Maximum Drain Current Vs. Case Temperature

Electrical Characteristics Curves (Pre-Irradiation N-channel)

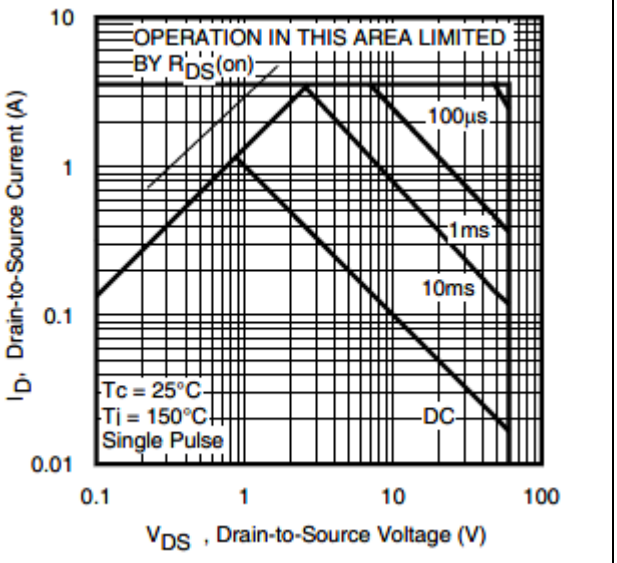


Figure 15 Maximum Safe Operating Area

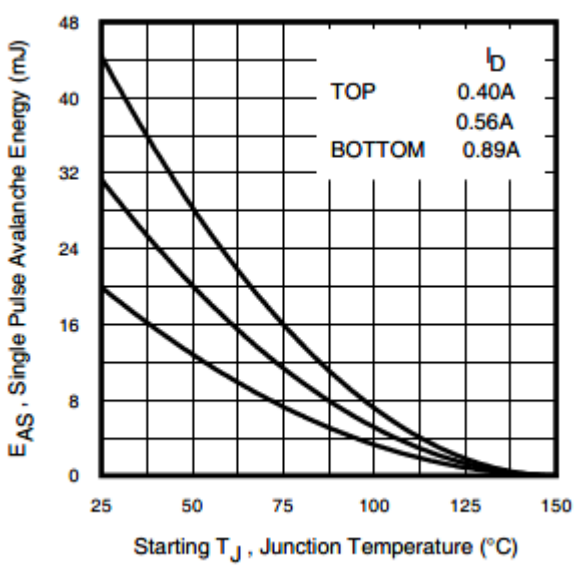


Figure 16 Maximum Avalanche Energy Vs. Junction Temperature

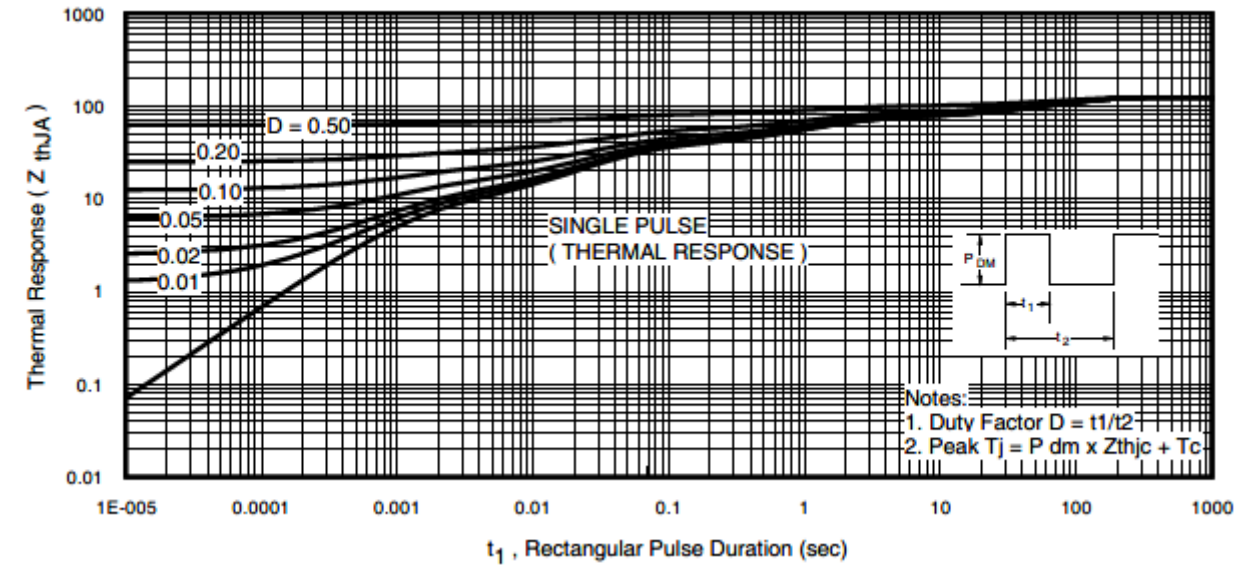


Figure 17 Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

4 Electrical Characteristics Curves (Pre-Irradiation P-channel)

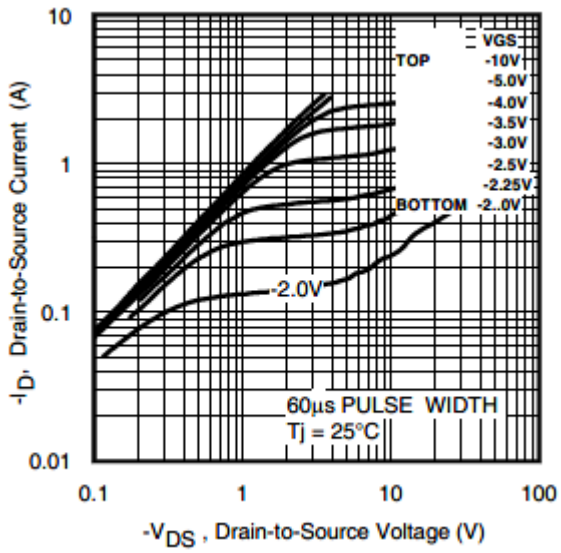


Figure 18 Typical Output Characteristics

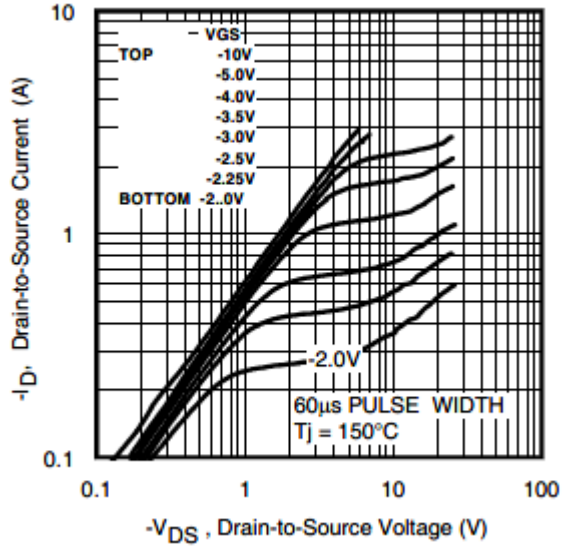


Figure 19 Typical Output Characteristics

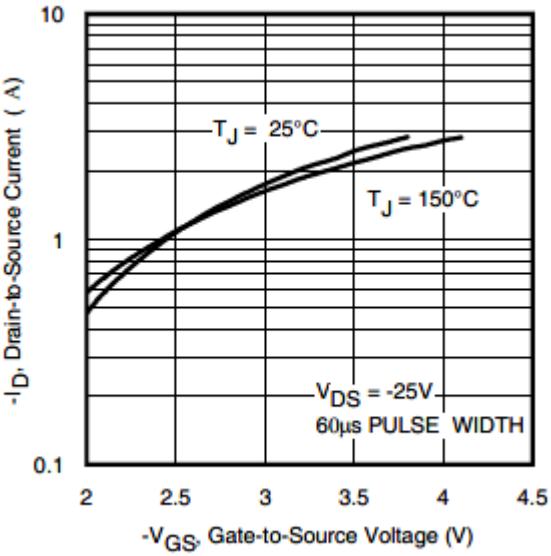


Figure 20 Typical Transfer Characteristics

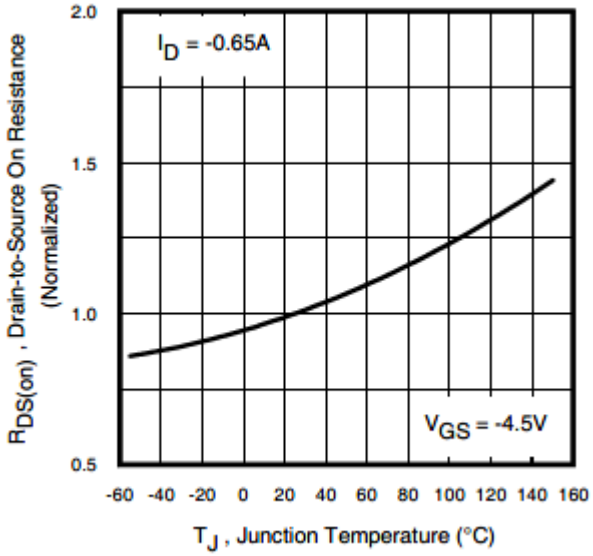


Figure 21 Normalized On-Resistance Vs. Temperature

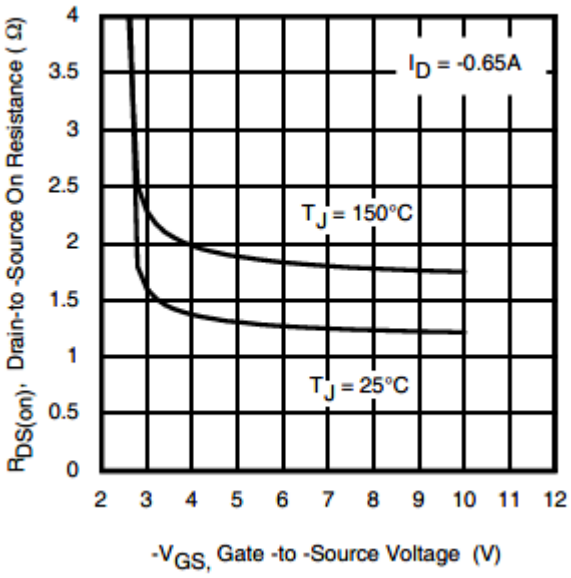


Figure 22 Typical On-Resistance Vs. Gate Voltage

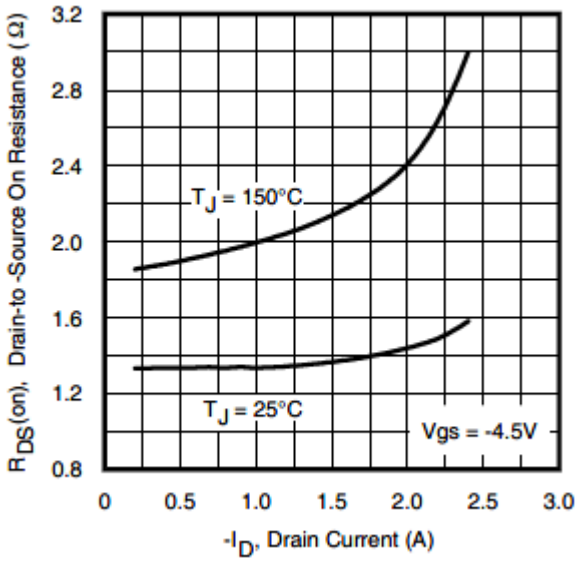


Figure 23 Typical On-Resistance Vs. Drain Current

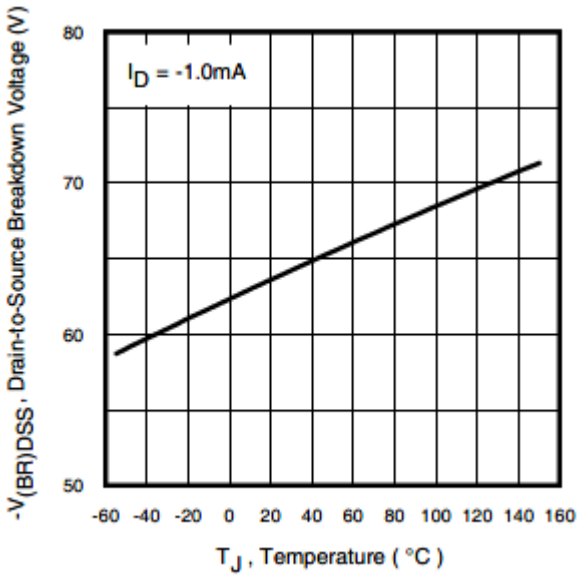


Figure 24 Typical Drain-to-Source Breakdown Voltage Vs. Temperature

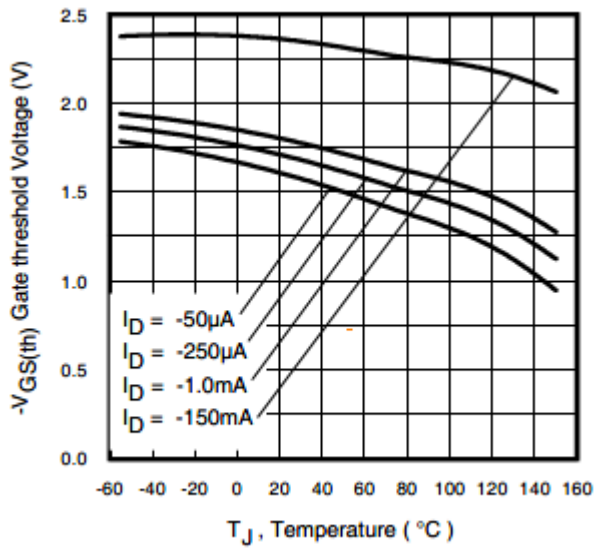


Figure 25 Typical Threshold Voltage Vs. Temperature

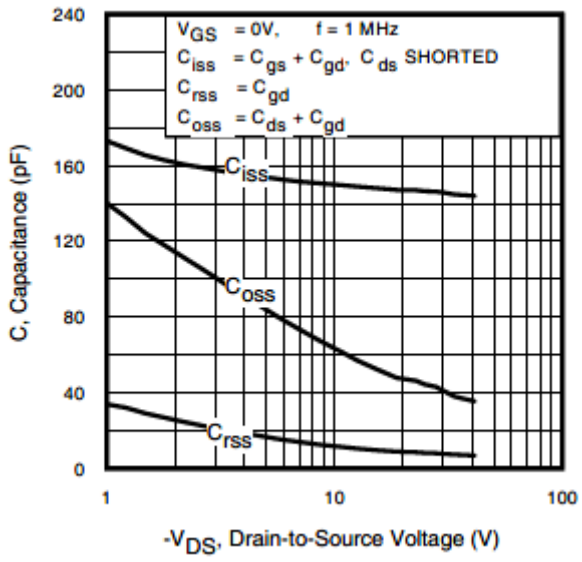


Figure 26 **Typical Capacitance Vs. Drain-to-Source Voltage**

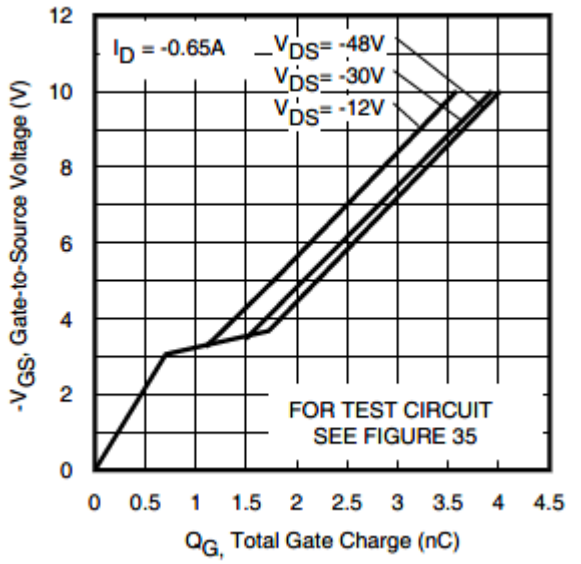


Figure 27 **Gate-to-Source Voltage Vs. Typical Gate Charge**

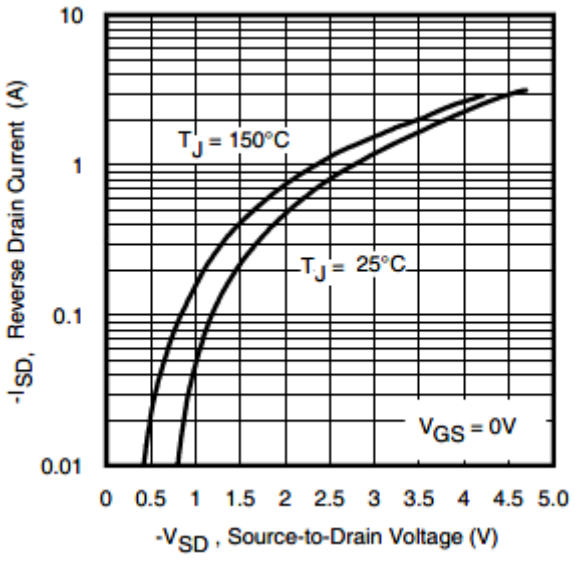


Figure 28 **Typical Source-Drain Current Vs. Diode Forward Voltage**

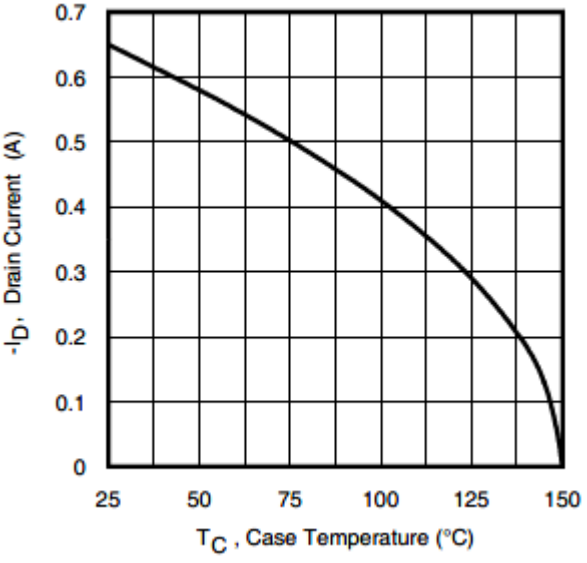


Figure 29 **Maximum Drain Current Vs. Case Temperature**

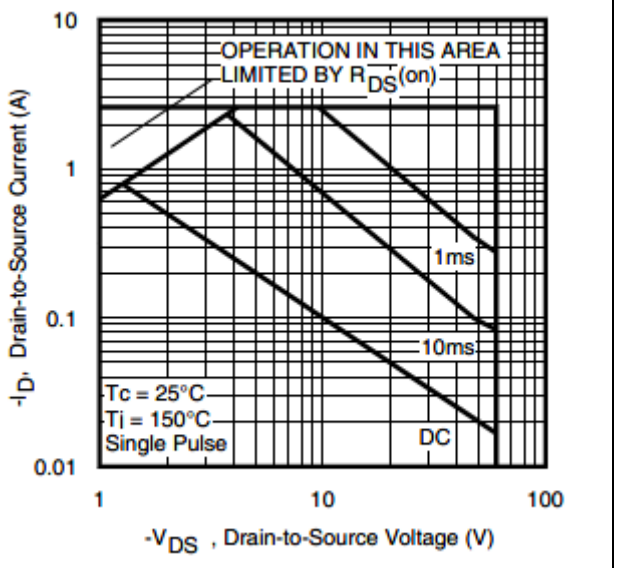


Figure 30 Maximum Safe Operating Area

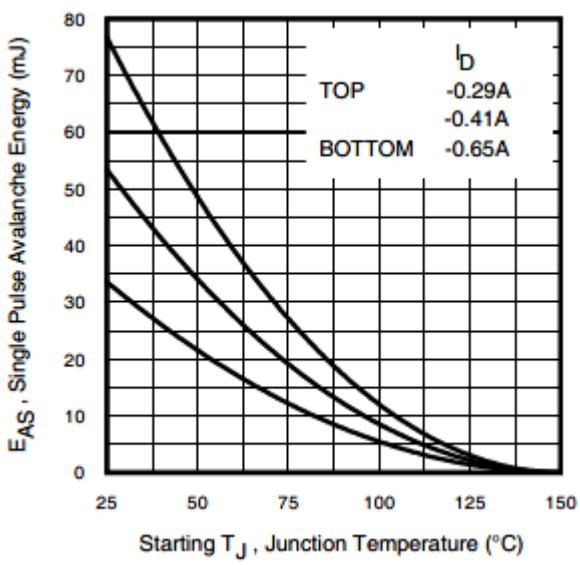


Figure 31 Maximum Avalanche Energy Vs. Junction Temperature

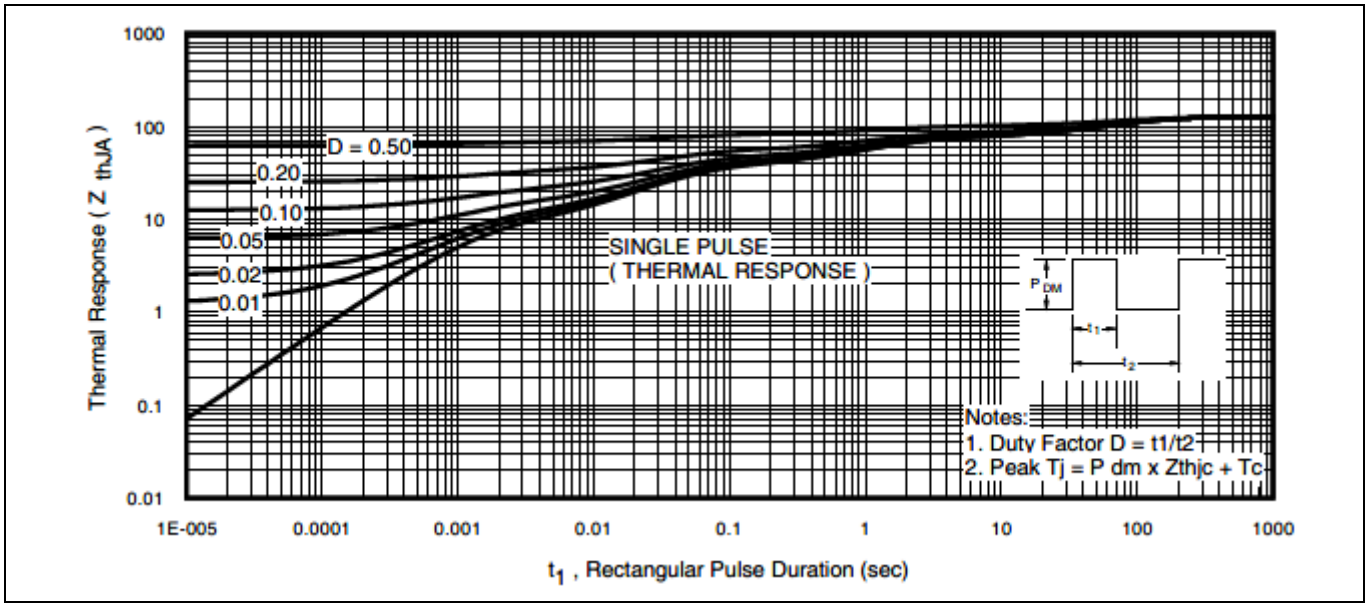


Figure 32 Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

5 Test Circuits (Pre-Irradiation N-channel)

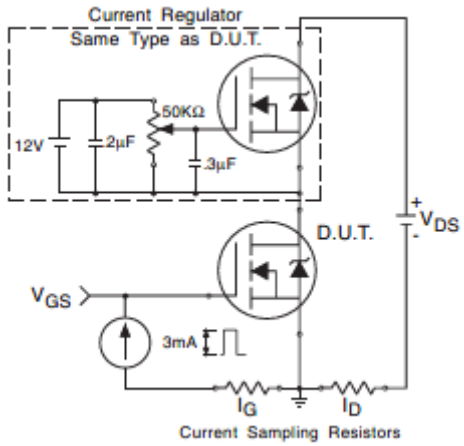


Figure 33 Gate Charge Test Circuit

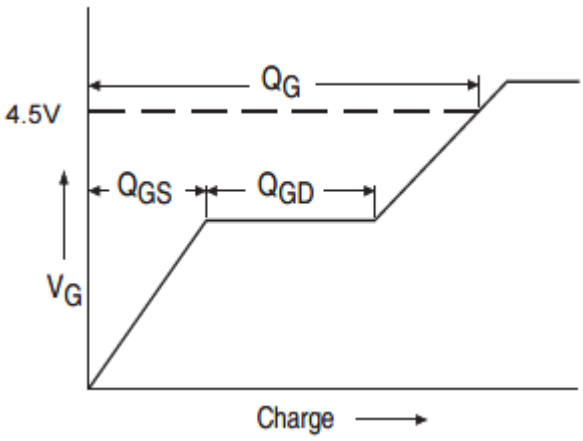


Figure 34 Gate Charge Waveform

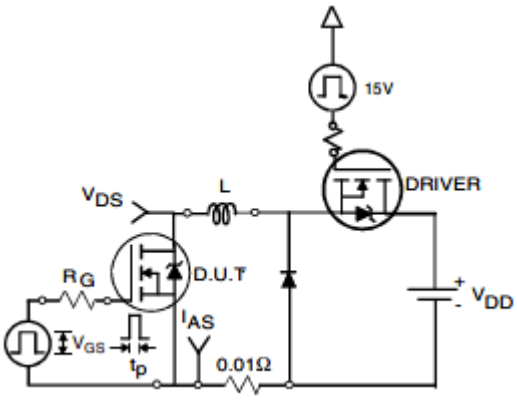


Figure 35 Unclamped Inductive Test Circuit

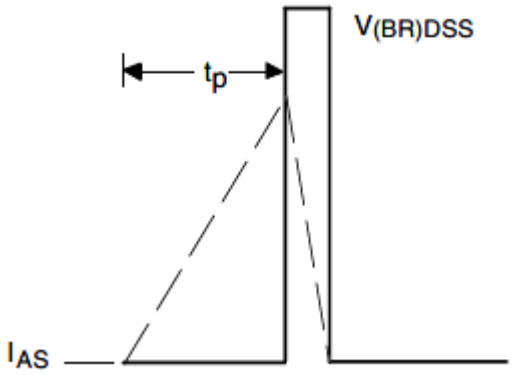


Figure 36 Unclamped Inductive Waveform

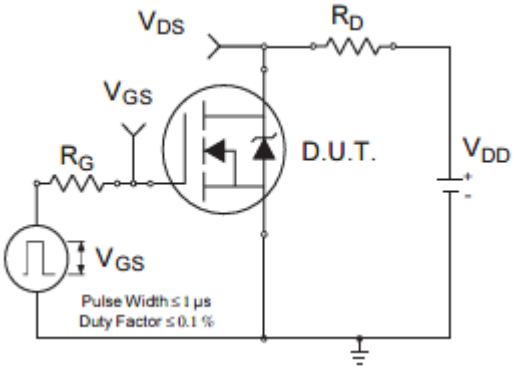


Figure 37 Switching Time Test Circuit

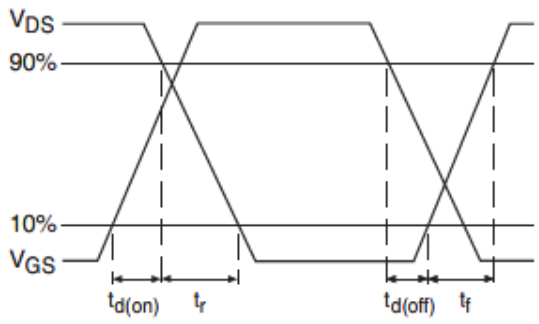


Figure 38 Switching Time Waveforms

6 Test Circuits (Pre-Irradiation P-channel)

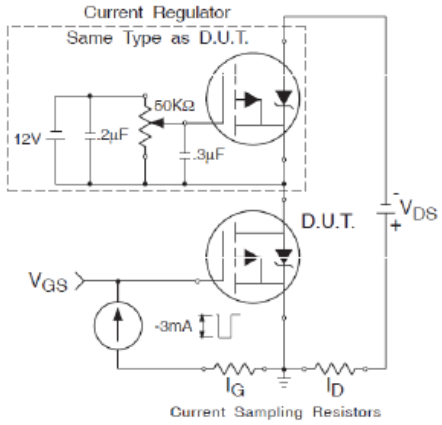


Figure 39 Gate Charge Test Circuit

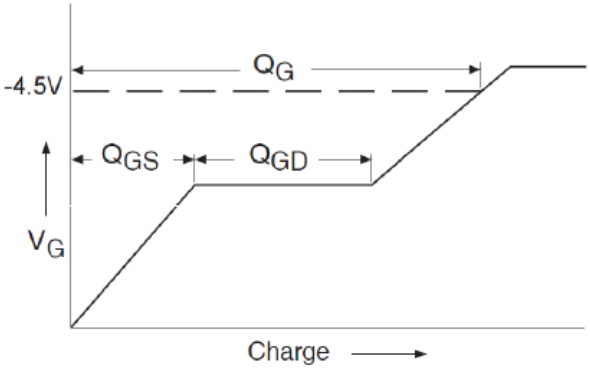


Figure 40 Gate Charge Waveform

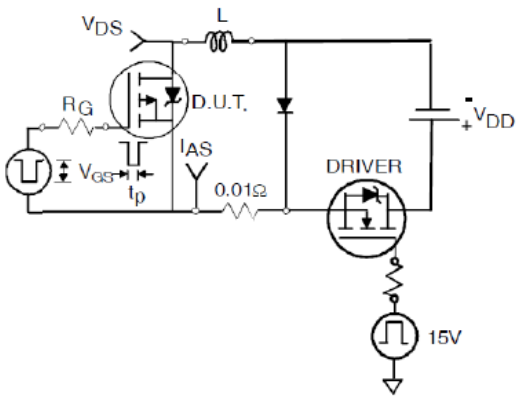


Figure 41 Unclamped Inductive Test Circuit

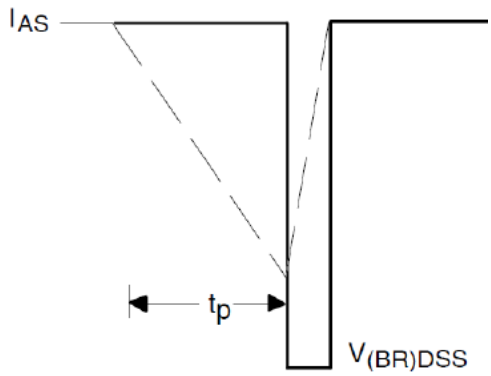


Figure 42 Unclamped Inductive Waveform

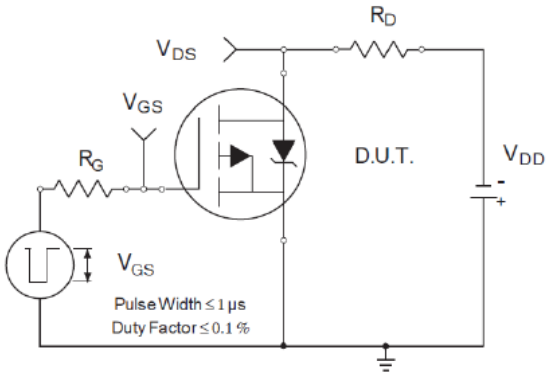


Figure 43 Switching Time Test Circuit

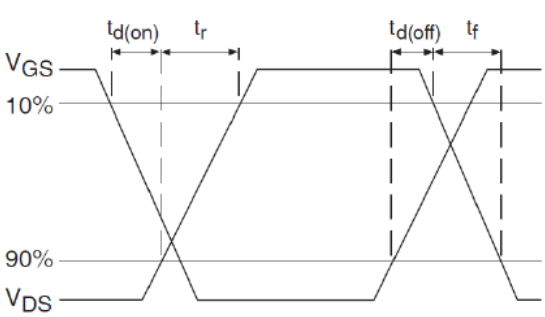
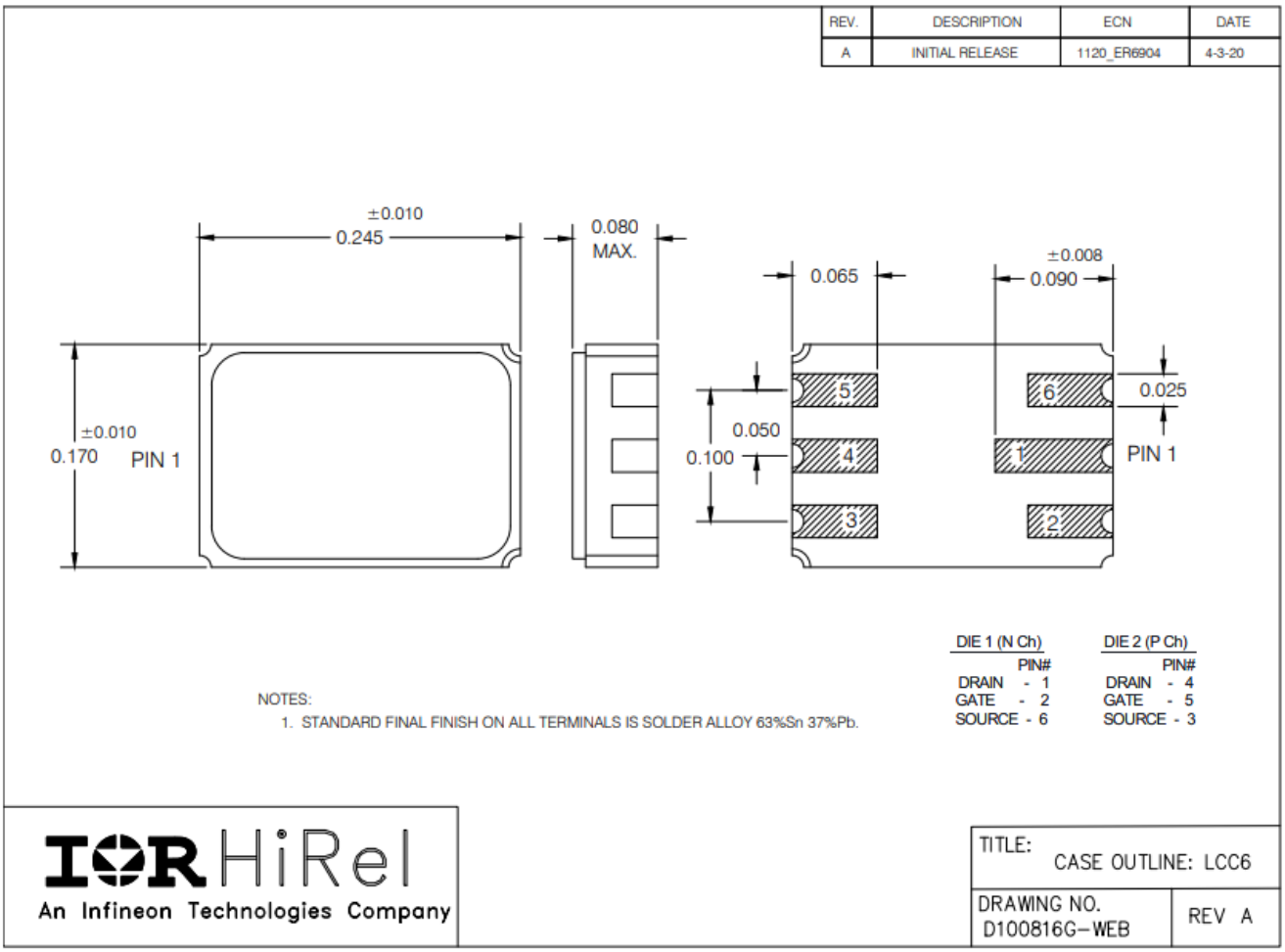


Figure 44 Switching Time Waveforms

7 Package Outline

Note: For the most updated package outline, please see the website: LCC-6



Revision history

Document version	Date of release	Description of changes
	03/26/2008	Datasheet (PD-94268)
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Rev B	02/13/2019	Updated based on ECN-1120_05818
Rev C	02/28/2019	Updated based on ECN-1120_06911
Rev D	08/13/2019	Updated based on ECN-1120_07306
Rev E	08/12/2022	Updated based on ECN-1120_09174

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