

# IRHE7110

PD-90732G

## Radiation Hardened Power MOSFET Surface Mount (LCC-18) 100V, 3.5A, N-channel, Rad Hard HEXFET™ Technology

### Features

- Single event effect (SEE) hardened
- Low  $R_{DS(on)}$
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Ceramic package
- Light weight
- Surface mount
- ESD rating: Class 1A per MIL-STD-750, Method 1020

### Potential Applications

- DC-DC converter
- Motor drives

### Product Validation

Qualified according to MIL-PRF-19500 for space applications

### Description

IR HiRel rad hard HEXFET technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low  $R_{DS(on)}$  and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

### Ordering Information

**Table 1** Ordering options

Part number	Package	Screening Level	TID Level
IRHE7110	LCC-18	COTS	100 krad(Si)
IRHE7110SCS	LCC-18	S-Level	100 krad(Si)
IRHE7110SCV	LCC-18	JANTXV-equivalent	100 krad(Si)
IRHE3110	LCC-18	COTS	300 krad(Si)
IRHE3110SCS	LCC-18	S-Level	300 krad(Si)
IRHE3110SCV	LCC-18	JANTXV-equivalent	300 krad(Si)
IRHE4110	LCC-18	COTS	500 krad(Si)
IRHE4110SCV	LCC-18	JANTXV-equivalent	500 krad(Si)

### Product Summary

- $BV_{DSS}$ : 100V
- $I_D$ : 3.5A
- $R_{DS(on),max}$ : 0.6 $\Omega$  (100 krad(Si))
- $Q_{G,max}$ : 11nC



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## Absolute Maximum Ratings

## 1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
$I_{D1} @ V_{GS} = 12V, T_C = 25^\circ C$	Continuous Drain Current	3.5	A
$I_{D2} @ V_{GS} = 12V, T_C = 100^\circ C$	Continuous Drain Current	2.2	A
$I_{DM} @ T_C = 25^\circ C$	Pulsed Drain Current <sup>1</sup>	14	A
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	15	W
	Linear Derating Factor	0.12	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy <sup>2</sup>	68	mJ
$I_{AR}$	Avalanche Current <sup>1</sup>	3.5	A
$E_{AR}$	Repetitive Avalanche Energy <sup>1</sup>	1.5	mJ
dv/dt	Peak Diode Reverse Recovery <sup>3</sup>	5.5	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5s)	
	Weight	0.42 (Typical)	

<sup>1</sup> Repetitive Rating; Pulse width limited by maximum junction temperature.

<sup>2</sup>  $V_{DD} = 25V$ , starting  $T_J = 25^\circ C$ ,  $L = 11.1mH$ , Peak  $I_L = 3.5A$ ,  $V_{GS} = 12V$ 
<sup>3</sup>  $I_{SD} \leq 3.5A$ ,  $di/dt \leq 140A/\mu s$ ,  $V_{DD} \leq 100V$ ,  $T_J \leq 150^\circ C$

## Device Characteristics

## 2 Device Characteristics

### 2.1 Electrical Characteristics (Pre-Irradiation)

**Table 3 Static and Dynamic Electrical Characteristics @  $T_j = 25^\circ\text{C}$  (Unless Otherwise Specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.60	$\Omega$	$V_{GS} = 12V, I_{D2} = 2.2A^1$
		—	—	0.69		$V_{GS} = 12V, I_{D1} = 3.5A^1$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 1mA$
$G_{fs}$	Forward Transconductance	0.8	—	—	S	$V_{DS} = 15V, I_{D2} = 2.2A^1$
$I_{DSS}$	Zero Gate Voltage Drain Current	—	—	25	$\mu\text{A}$	$V_{DS} = 80V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
$Q_G$	Total Gate Charge	—	—	11	nC	$I_{D1} = 3.5A$
$Q_{GS}$	Gate-to-Source Charge	—	—	3.0		$V_{DS} = 50V$
$Q_{GD}$	Gate-to-Drain ('Miller') Charge	—	—	3.3		$V_{GS} = 12V$
$t_{d(on)}$	Turn-On Delay Time	—	—	20	ns	$I_{D1} = 3.5A^{**}$ $V_{DD} = 50V$ $R_G = 7.5\Omega$ $V_{GS} = 12V$
$t_r$	Rise Time	—	—	25		
$t_{d(off)}$	Turn-Off Delay Time	—	—	40		
$t_f$	Fall Time	—	—	40		
$L_s + L_D$	Total Inductance	—	6.1	—	nH	Measured from center of Drain pad to center of Source pad
$C_{iss}$	Input Capacitance	—	290	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$
$C_{oss}$	Output Capacitance	—	100	—		
$C_{rss}$	Reverse Transfer Capacitance	—	15	—		

\*\* Switching speed maximum limits are based on manufacturing test equipment and capability.

<sup>1</sup> Pulse width  $\leq 300 \mu\text{s}$ ; Duty Cycle  $\leq 2\%$

## Device Characteristics

## 2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	3.5	A	
$I_{SM}$	Pulsed Source Current (Body Diode) <sup>1</sup>	—	—	14	A	
$V_{SD}$	Diode Forward Voltage	—	—	1.4	V	$T_J = 25^\circ\text{C}$ , $I_S = 3.5\text{A}$ , $V_{GS} = 0\text{V}$ <sup>2</sup>
$t_{rr}$	Reverse Recovery Time	—	—	180	ns	$T_J = 25^\circ\text{C}$ , $I_F = 3.5\text{A}$ , $V_{DD} \leq 50\text{V}$ $di/dt = 100\text{A}/\mu\text{s}$ <sup>2</sup>
$Q_{rr}$	Reverse Recovery Charge	—	—	2.0	$\mu\text{C}$	
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

## 2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	8.3	$^\circ\text{C}/\text{W}$
$R_{\theta J-PCB}$	Junction-to-PC Board (Soldered to 2" sq copper clad board)	—	27	—	

## 2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

## 2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @  $T_J = 25^\circ\text{C}$ , Post Total Dose Irradiation<sup>3, 4</sup>

Symbol	Parameter	100 krad (Si) <sup>5</sup>		Up to 500 krad (Si) <sup>6</sup>		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	100	—	100	—	V	$V_{GS} = 0\text{V}$ , $I_D = 1.0\text{mA}$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	2.0	4.0	V	$V_{DS} = V_{GS}$ , $I_D = 1.0\text{mA}$
$I_{GSS}$	Gate-to-Source Leakage Forward	—	100	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Leakage Reverse	—	-100	—	-100		$V_{GS} = -20\text{V}$
$I_{DSS}$	Zero Gate Voltage Drain Current	—	10	—	10	$\mu\text{A}$	$V_{DS} = 80\text{V}$ , $V_{GS} = 0\text{V}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) <sup>2</sup>	—	0.6	—	0.8	$\Omega$	$V_{GS} = 12\text{V}$ , $I_{D2} = 2.2\text{A}$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (LCC-18) <sup>2</sup>	—	0.6	—	0.8	$\Omega$	$V_{GS} = 12\text{V}$ , $I_{D2} = 2.2\text{A}$
$V_{SD}$	Diode Forward Voltage	—	1.4	—	1.4	V	$V_{GS} = 0\text{V}$ , $I_F = 3.5\text{A}$

<sup>1</sup> Repetitive Rating; Pulse width limited by maximum junction temperature.

<sup>2</sup> Pulse width  $\leq 300\ \mu\text{s}$ ; Duty Cycle  $\leq 2\%$

<sup>3</sup> Total Dose Irradiation with  $V_{GS}$  Bias.  $V_{GS} = 12\text{V}$  applied and  $V_{DS} = 0$  during irradiation per MIL-STD-750, Method 1019, condition A.

<sup>4</sup> Total Dose Irradiation with  $V_{DS}$  Bias.  $V_{DS} = 80\text{V}$  applied and  $V_{GS} = 0$  during irradiation per MIL-STD-750, Method 1019, condition A.

<sup>5</sup> Part numbers IRHE7110

<sup>6</sup> Part numbers IRHE3110 and IRHE4110

Device Characteristics

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

Ion	LET (MeV·cm <sup>2</sup> /mg)	Energy (MeV)	Range (μm)	V <sub>DS</sub> (V)				
				V <sub>GS</sub> = 0V	V <sub>GS</sub> = -5V	V <sub>GS</sub> = -10V	V <sub>GS</sub> = -15V	V <sub>GS</sub> = -20V
Cu	28	285	43	100	100	100	80	60
Br	36.8	305	39	100	90	70	50	—

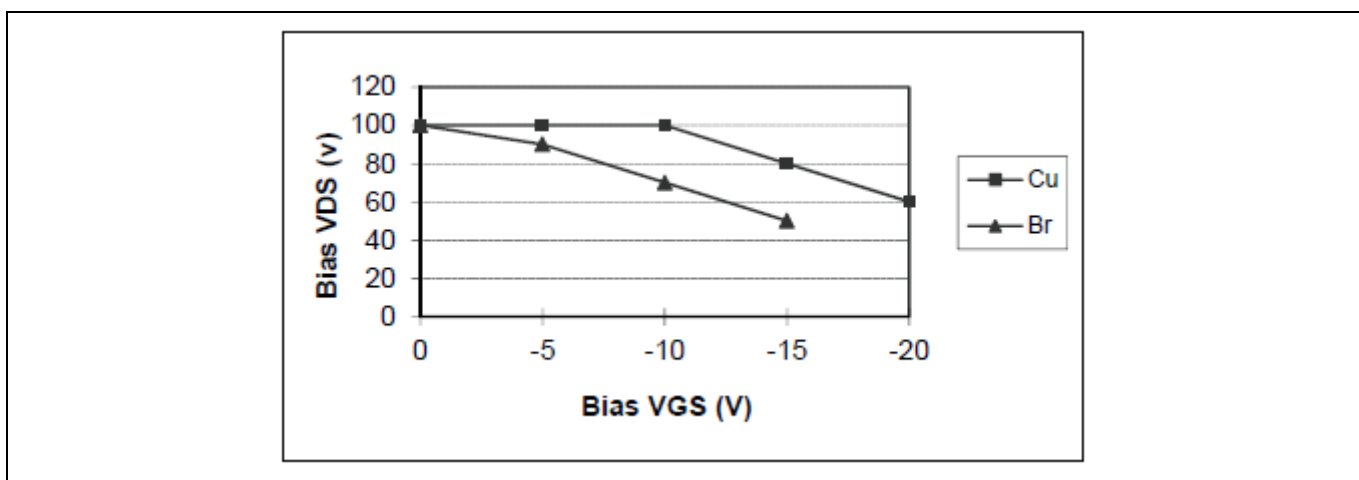


Figure 1 Typical Single Event Effect, Safe Operating Area

### 3 Electrical Characteristics Curves (Pre-irradiation)

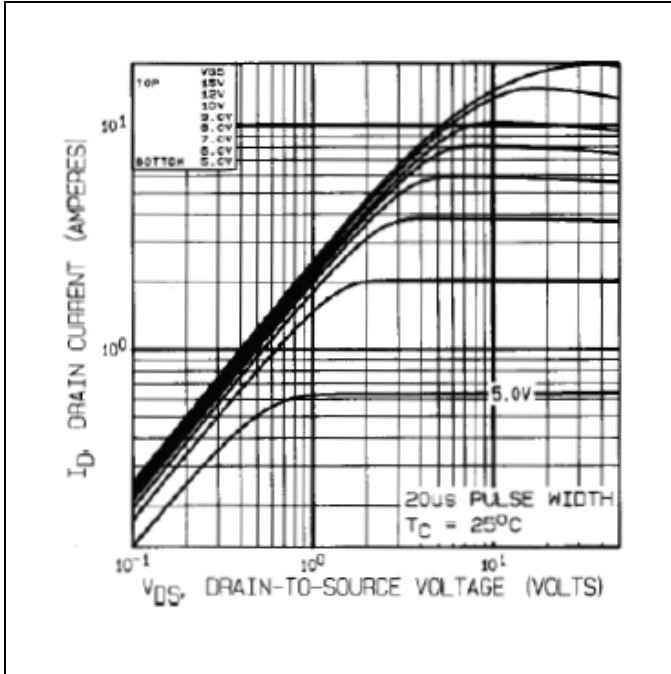


Figure 2 Typical Output Characteristics

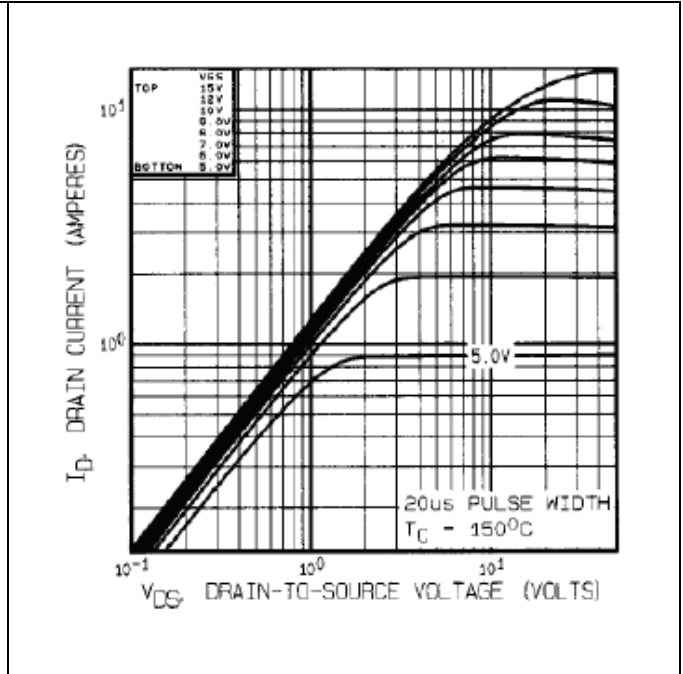


Figure 3 Typical Output Characteristics

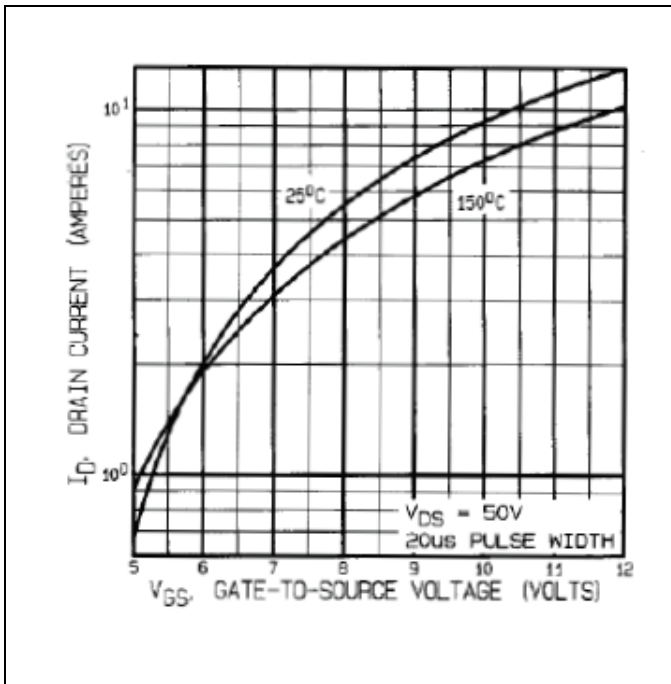


Figure 4 Typical Transfer Characteristics

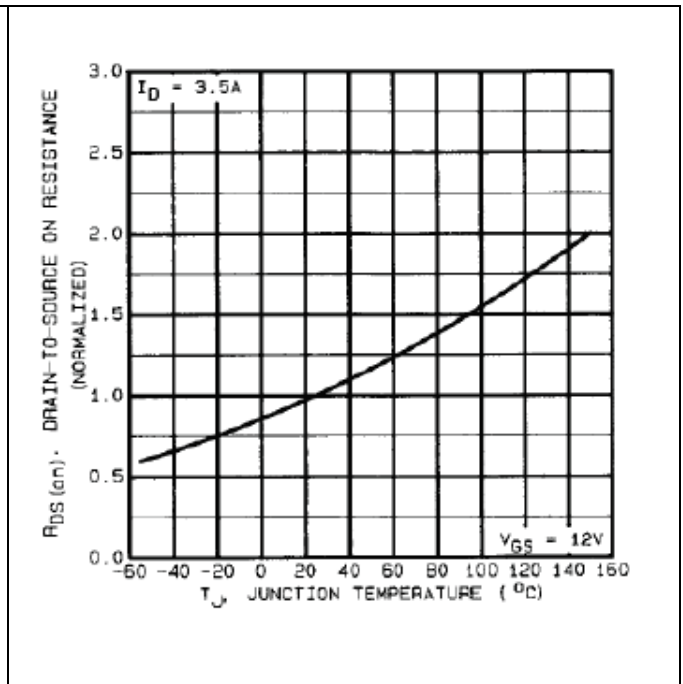
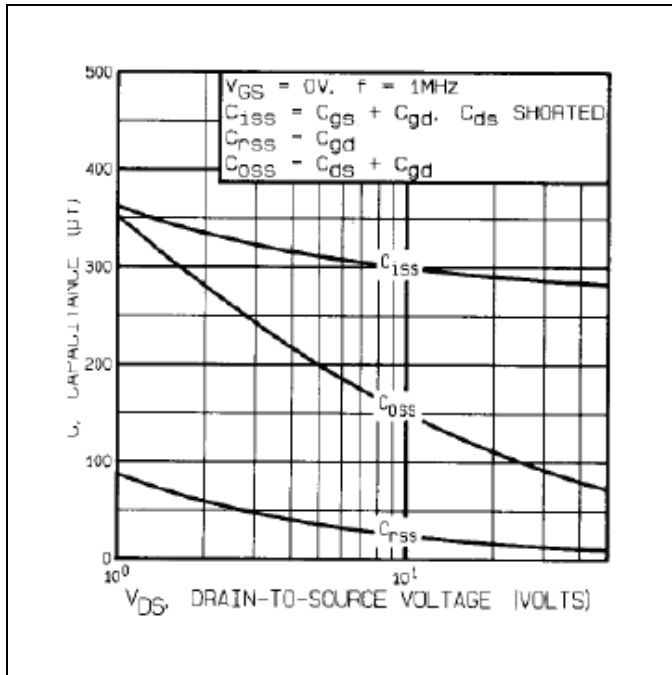


Figure 5 Normalized On-Resistance Vs. Temperature

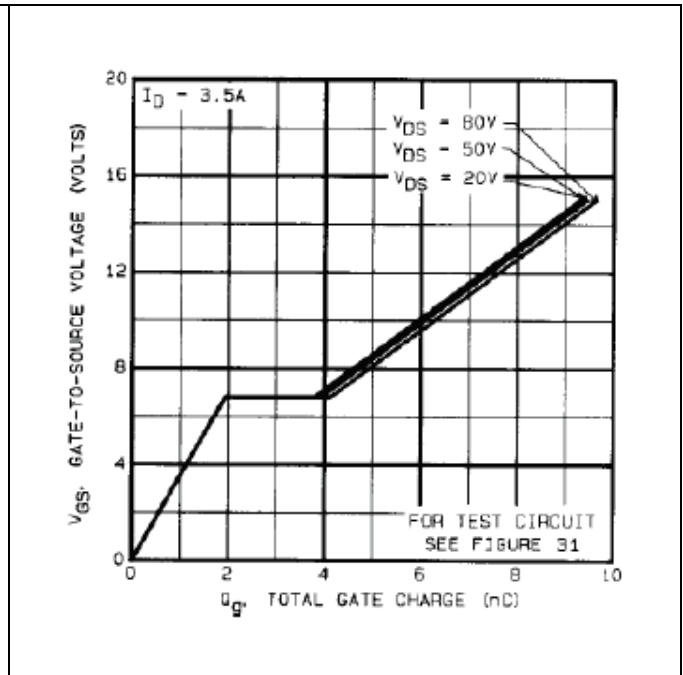
**IRHE7110**

**Radiation Hardened Power MOSFET Surface Mount (LCC-18)**

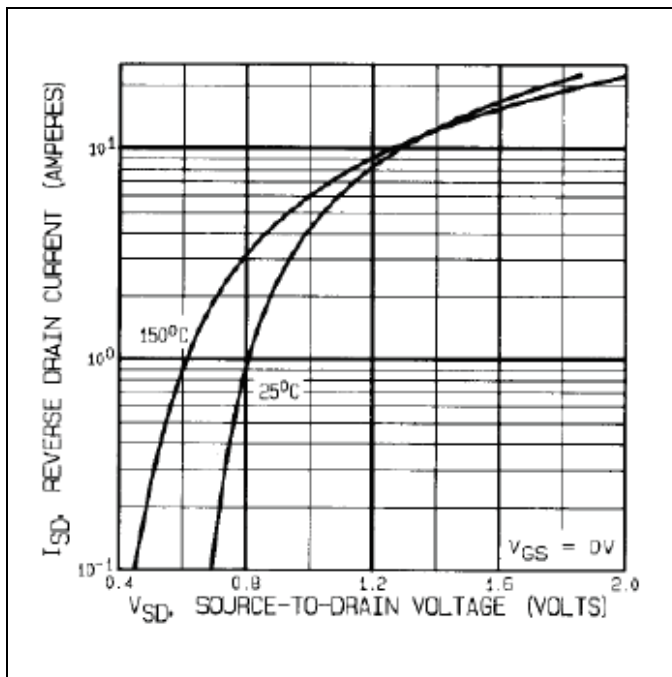
**Electrical Characteristics Curves (Pre-irradiation)**



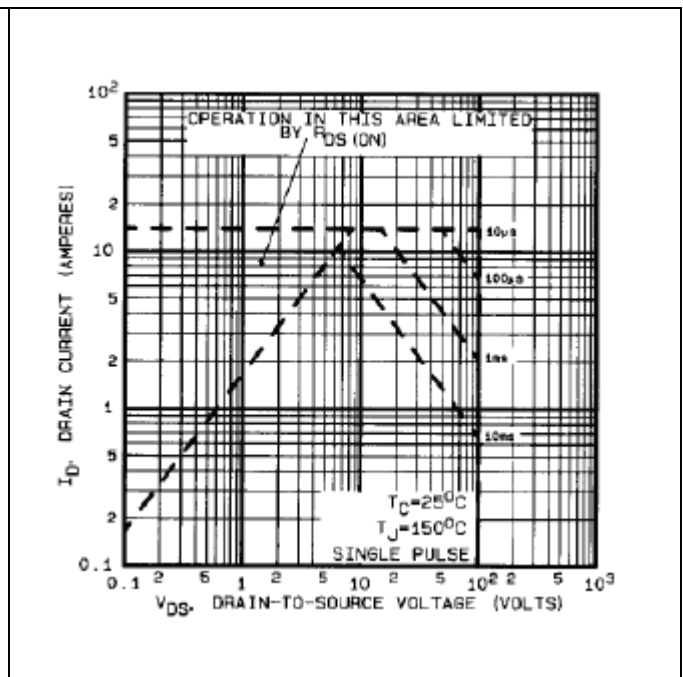
**Figure 6 Typical Capacitance Vs. Drain-to-Source Voltage**



**Figure 7 Typical Gate-to-Source Voltage Vs. Typical Gate Charge**



**Figure 8 Typical Source-Drain Current Vs. Diode Forward Voltage**



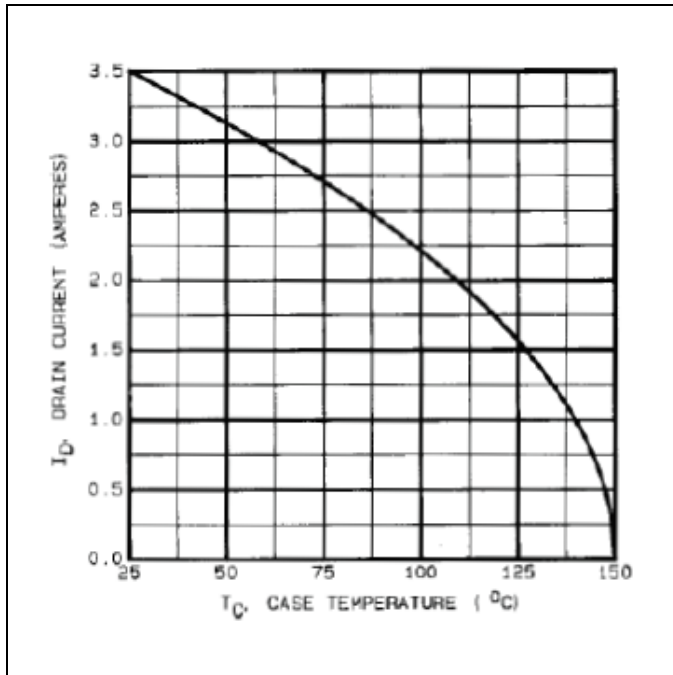
**Figure 9 Maximum Safe Operating Area**



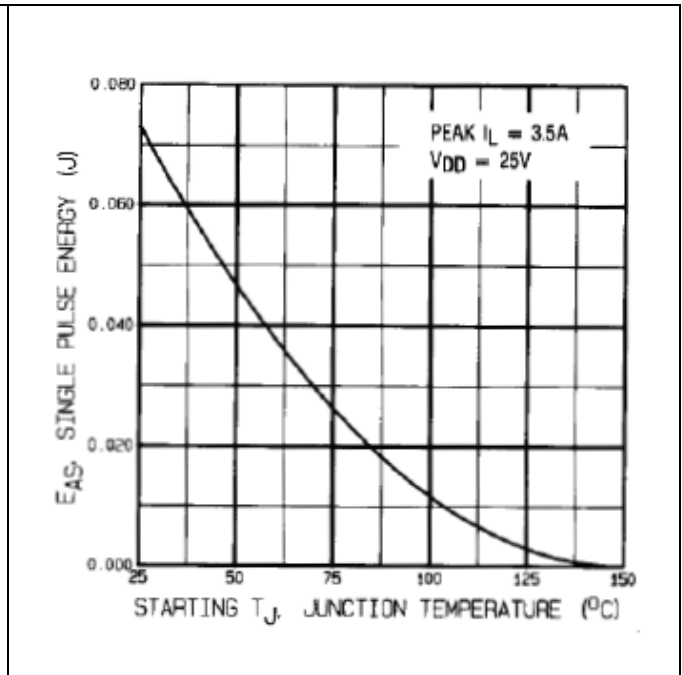
**IRHE7110**

**Radiation Hardened Power MOSFET Surface Mount (LCC-18)**

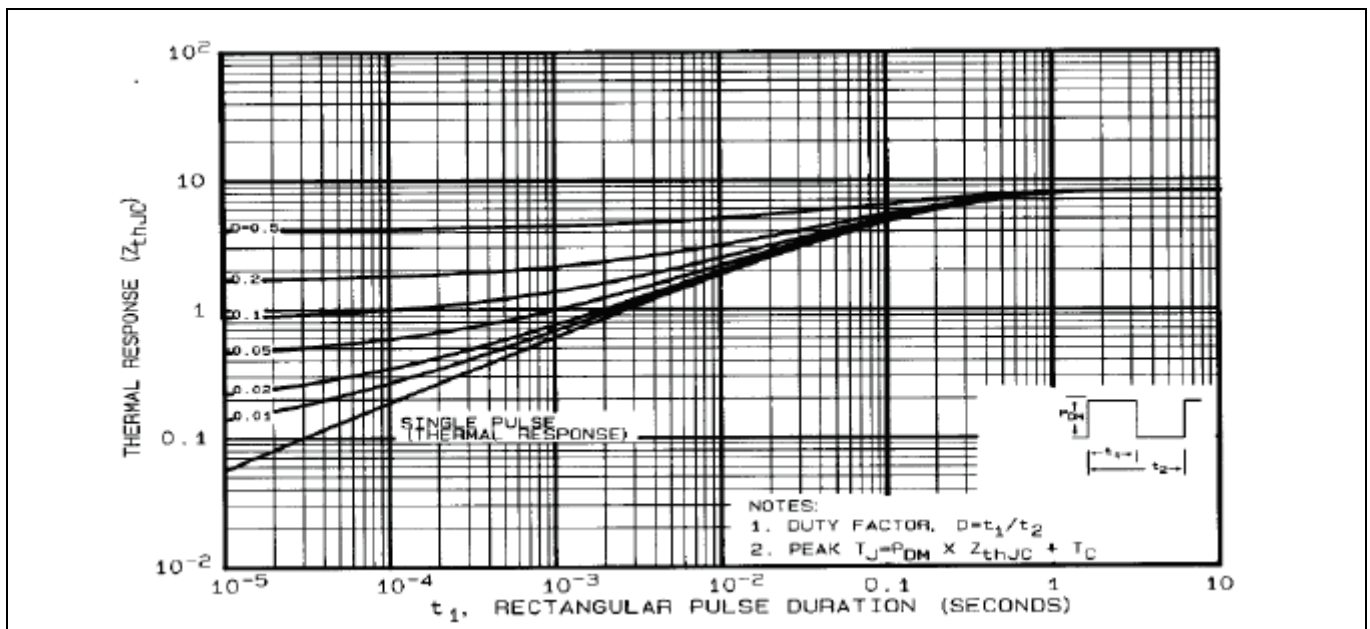
**Electrical Characteristics Curves (Pre-irradiation)**



**Figure 10 Maximum Drain Current Vs. Case Temperature**



**Figure 11 Maximum Avalanche Energy Vs. Junction Temperature**



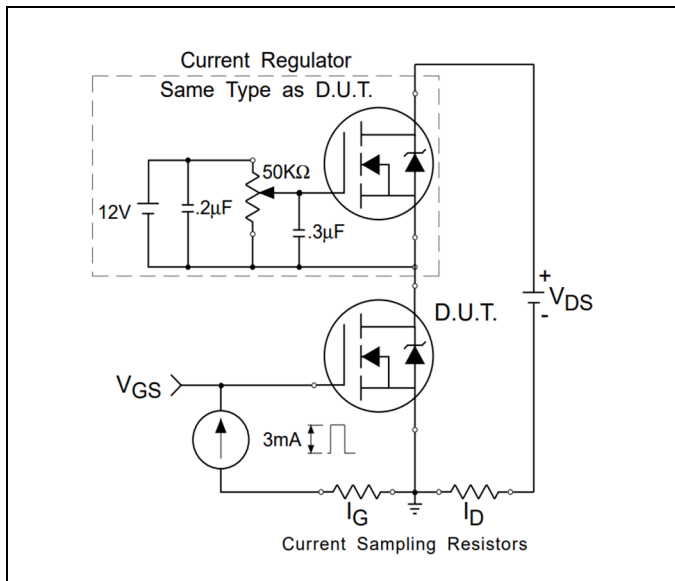
**Figure 12 Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**IRHE7110**

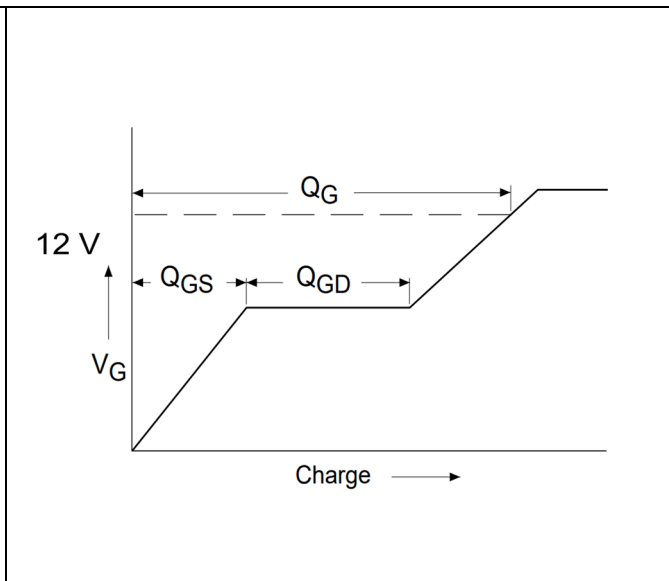
**Radiation Hardened Power MOSFET Surface Mount (LCC-18)**

**Test Circuits (Pre-irradiation)**

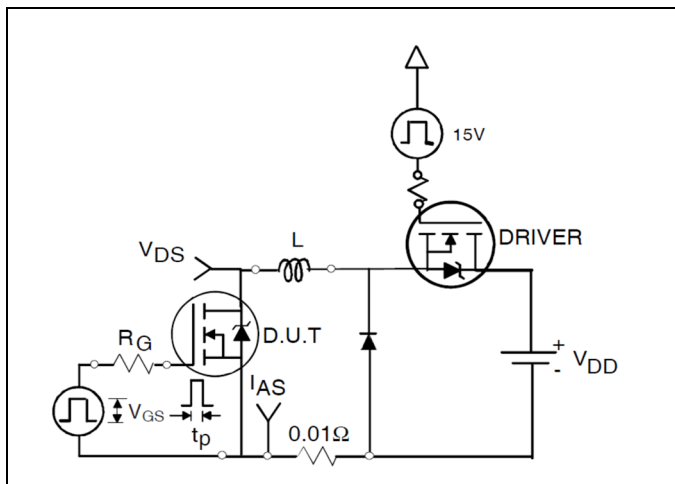
**4 Test Circuits (Pre-irradiation)**



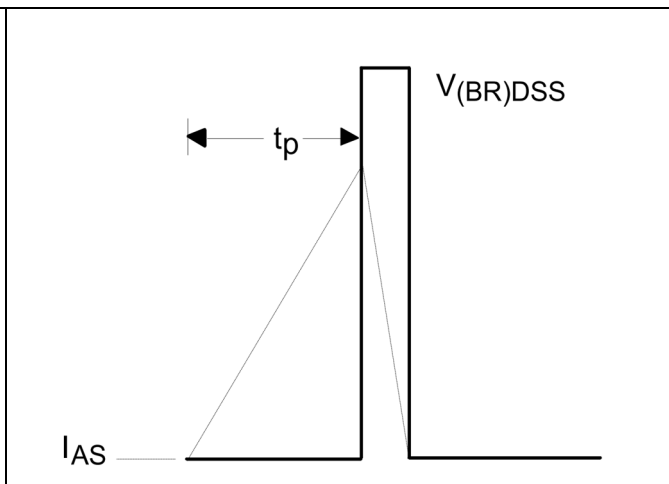
**Figure 13 Gate Charge Test Circuit**



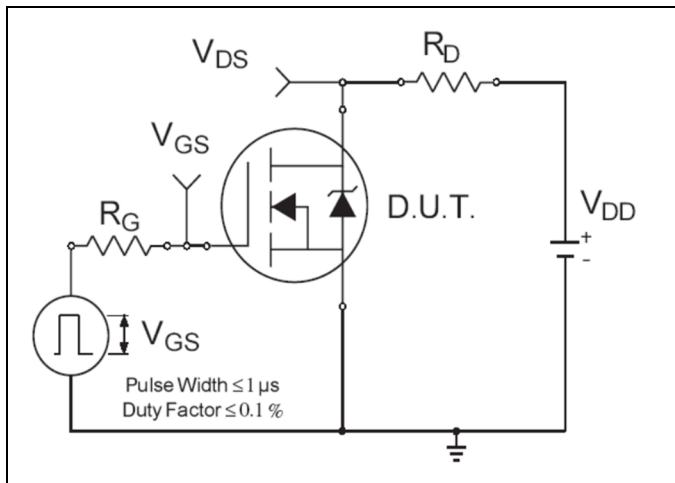
**Figure 14 Gate Charge Waveform**



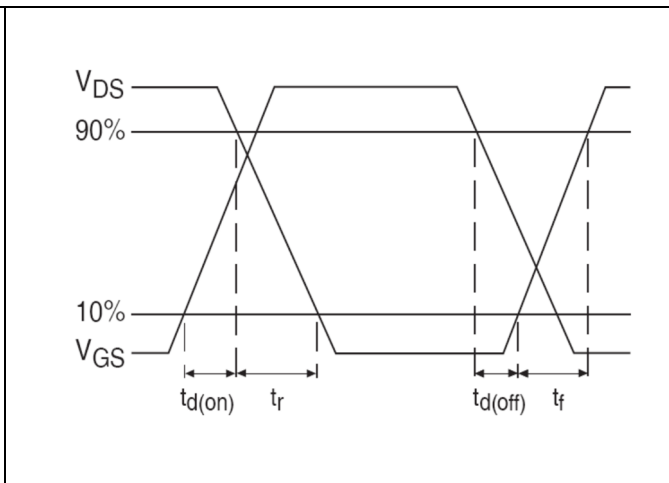
**Figure 15 Unclamped Inductive Test Circuit**



**Figure 16 Unclamped Inductive Waveform**



**Figure 17 Switching Time Test Circuit**

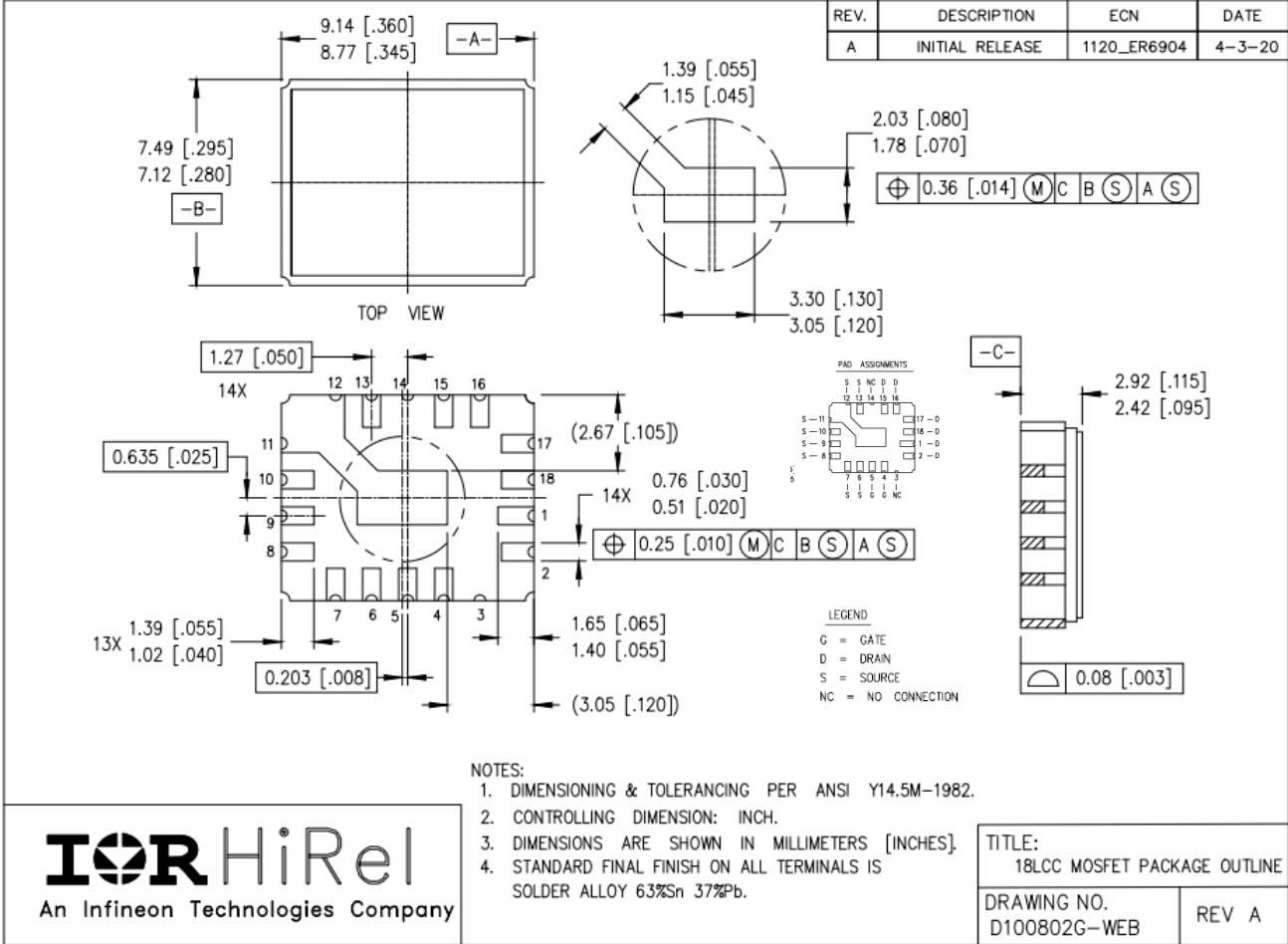


**Figure 18 Switching Time Waveforms**

Package Outline

# 5 Package Outline

Note: For the most updated package outline, please see the website: [LCC-18](#)



**Revision history****Revision history**

<b>Document version</b>	<b>Date of release</b>	<b>Description of changes</b>
	09/15/1998	Datasheet (PD-90732A)
Rev B	10/14/1998	Updated title "MEGA RAD HARD"
Rev C	10/27/1998	Corrected Rth-PCB-page2
Rev D	06/06/2001	Updated switchiing test condition-page2
Rev E	04/15/2002	Corrected typo-RthJC from 83C/W TO 8.3C/W
Rev F	12/11/2017	Updated based on ECN-1120_05393
Rev G	05/24/2022	Updated based on ECN-1120_09018

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**Edition 2022-05-24**

### Published by

**International Rectifier HiRel Products,  
Inc.**

**An Infineon Technologies company  
El Segundo, California 90245 USA**

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