
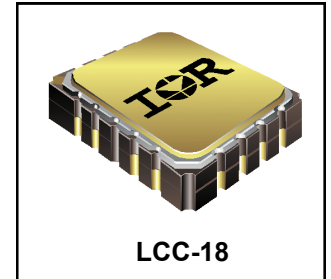


**RADIATION HARDENED
 POWER MOSFET
 SURFACE MOUNT (LCC-18)**

30V, N CHANNEL
 REF: MIL-PRF-19500/700
 **TECHNOLOGY**

Product Summary

Part Number	Radiation Level	RDS(on)	I _D	QPL Part Number
IRHE57Z30	100 kRads(Si)	0.07Ω	12A*	JANSR2N7494U5
IRHE53Z30	300 kRads(Si)	0.07Ω	12A*	JANSF2N7494U5
IRHE55Z30	500 kRads(Si)	0.07Ω	12A*	JANSG2N7494U5
IRHE58Z30	1000 kRads(Si)	0.07Ω	12A*	JANSH2N7494U5



Description

IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retail all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Package
- Surface Mount
- Light Weight
- ESD Rating: Class 1C per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Pre-Irradiation

Symbol	Parameter	Value	Units
I _{D1} @ V _{GS} = 12V, T _C = 25°C	Continuous Drain Current	12*	A
I _{D2} @ V _{GS} = 12V, T _C = 100°C	Continuous Drain Current	8.0	
I _{DM} @ T _C = 25°C	Pulsed Drain Current ①	48	
P _D @ T _C = 25°C	Maximum Power Dissipation	25	W
	Linear Derating Factor	0.2	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy ②	156	mJ
I _{AR}	Avalanche Current ①	12	A
E _{AR}	Repetitive Avalanche Energy ①	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.3	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Package Mounting Surface Temperature	300 (for 5s)	
	Weight	0.42 (Typical)	g

For Footnotes, refer to the page 2

Electrical Characteristics @ T_J = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.025	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.07	Ω	V _{GS} = 12V, I _{D2} = 8.0A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 1.0mA
G _{fs}	Forward Transconductance	8.0	—	—	S	V _{DS} = 15V, I _{D2} = 8.0A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	10	μA	V _{DS} = 24V, V _{GS} = 0V
		—	—	25		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _G	Total Gate Charge	—	—	65	nC	I _{D1} = 12A
Q _{GS}	Gate-to-Source Charge	—	—	20		V _{DS} = 15V
Q _{GD}	Gate-to-Drain ('Miller') Charge	—	—	10		V _{GS} = 12V
t _{d(on)}	Turn-On Delay Time	—	—	25	ns	V _{DD} = 15V
t _r	Rise Time	—	—	100		I _{D1} = 12A
t _{d(off)}	Turn-Off Delay Time	—	—	35		R _G = 7.5Ω
t _f	Fall Time	—	—	30		V _{GS} = 12V
L _s + L _D	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C _{iss}	Input Capacitance	—	2184	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	940	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	35	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	12*	A	
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	48		
V _{SD}	Diode Forward Voltage	—	—	1.8	V	T _J = 25°C, I _S = 12A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	102	ns	T _J = 25°C, I _F = 12A, V _{DD} ≤ 25V
Q _{rr}	Reverse Recovery Charge	—	—	196	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _s +L _D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	—	5.0	°C/W
R _{θJ-PCB}	Junction-to-PC Board	—	19	—	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V_{DD} = 20V, starting T_J = 25°C, L = 2.17mH, Peak I_L = 12A, V_{GS} = 12V
- ③ I_{SD} ≤ 12A, di/dt ≤ 110A/μs, V_{DD} ≤ 30V, T_J ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V_{GS} Bias. 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V_{DS} Bias. 24 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 500 kRads (Si) ¹		1000 kRads (Si) ²		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV _{DSS}	Drain-to-Source Breakdown Voltage	30	—	30	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.0	1.5	4.0	V	V _{DS} = V _{GS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100	nA	V _{GS} = -20V
I _{DSS}	Zero Gate Voltage Drain Current	—	10	—	25	μA	V _{DS} = 24V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ④	—	0.024	—	0.042	Ω	V _{GS} = 12V, I _{D2} = 8.0A
	On-State Resistance (TO-3)						
R _{DS(on)}	Static Drain-to-Source ④	—	0.07	—	0.088	Ω	V _{GS} = 12V, I _{D2} = 8.0A
	On-State Resistance (LCC-18)						
V _{SD}	Diode Forward Voltage ④	—	1.8	—	1.8	V	V _{GS} = 0V, I _S = 12A

1. Part numbers IRHE57Z30 (JANSR2N7494U5), IRHE53Z30 (JANSF2N7494U5) and IRHE55Z30 (JANSG2N7494U5)
2. Part numbers IRHE58Z30 (JANSH2N7494U5)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	V _{DS} (V)				
			@V _{GS} =0V	@V _{GS} =-5V	@V _{GS} =-10V	@V _{GS} =-15V	@V _{GS} =-20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	30	30	30	22.5	15
61 ± 5%	330 ± 7.5%	31 ± 10%	25	25	20	15	7.5
84 ± 5%	350 ± 10%	28 ± 7.5%	25	25	20	—	—

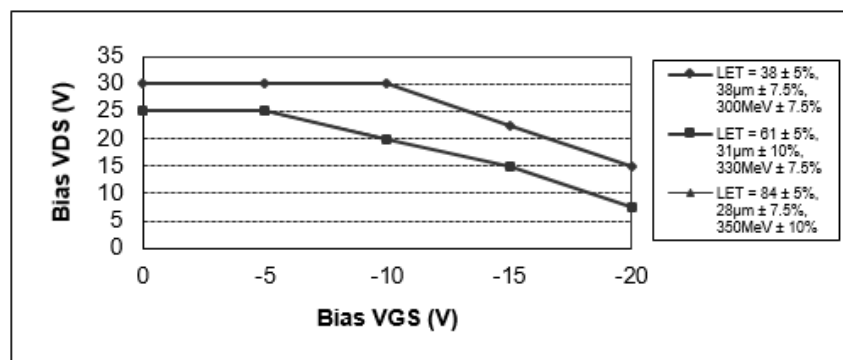
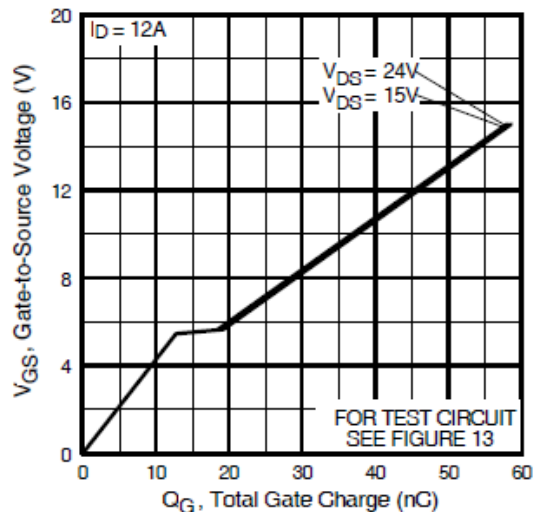
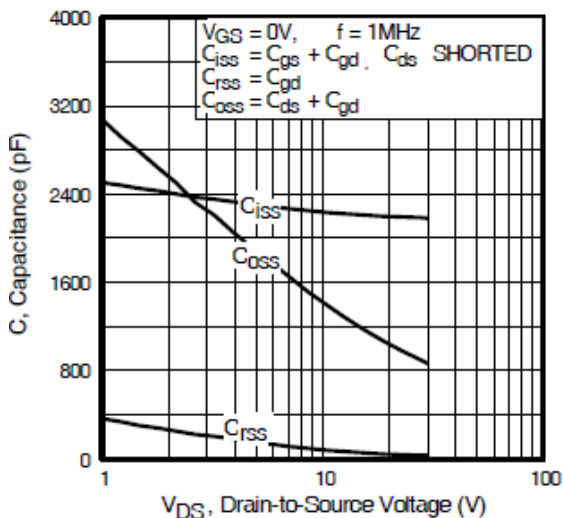
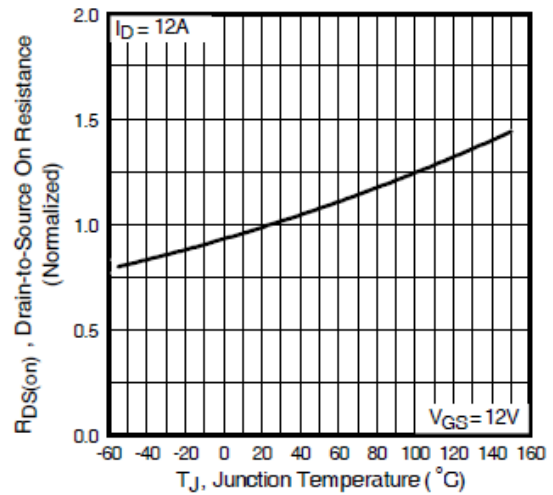
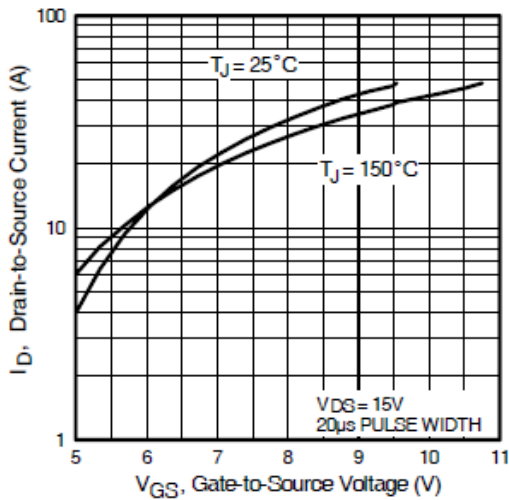
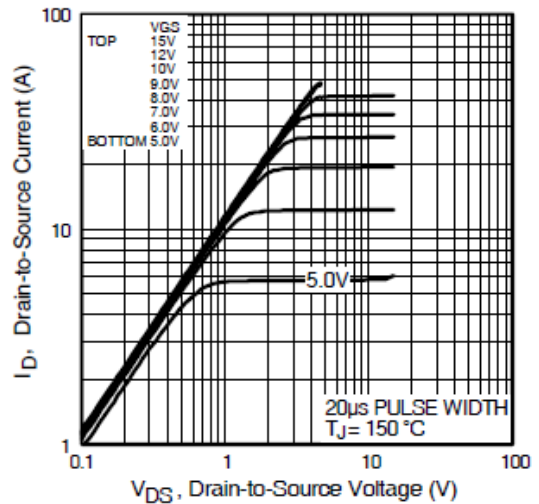
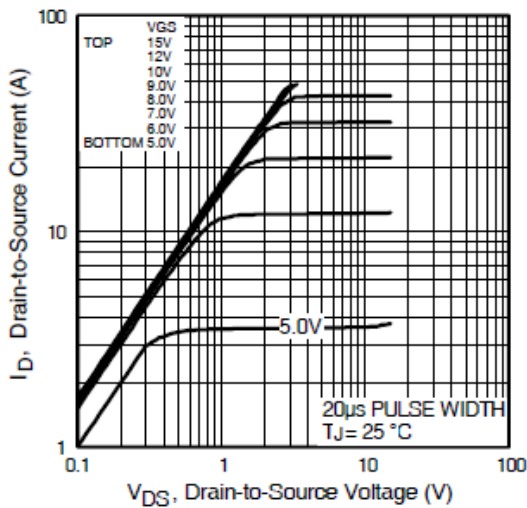


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2



Pre-Irradiation

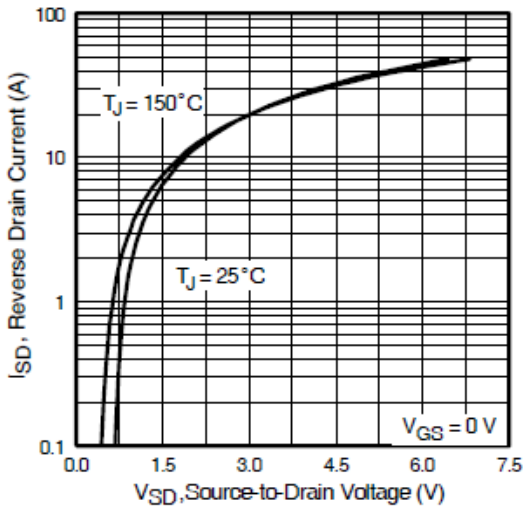


Fig 7. Typical Source-Drain Diode Forward Voltage

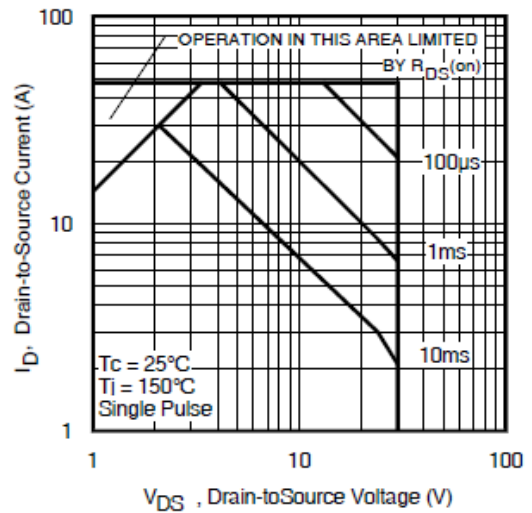


Fig 8. Maximum Safe Operating Area

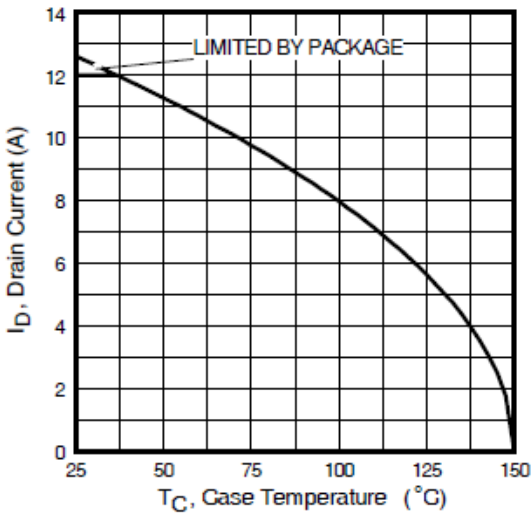


Fig 9. Maximum Drain Current Vs. Case Temperature

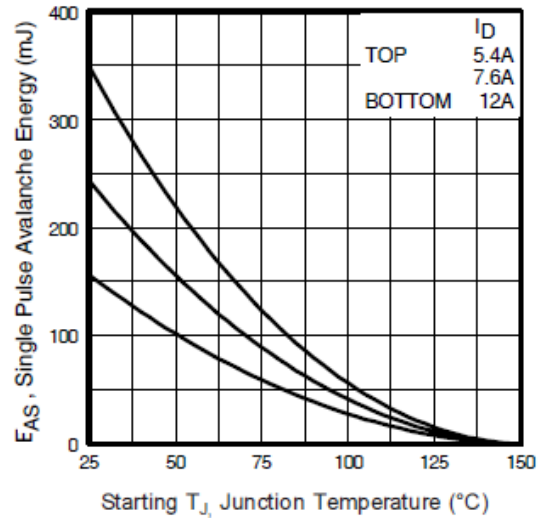


Fig 10. Maximum Avalanche Energy Vs. Drain Current

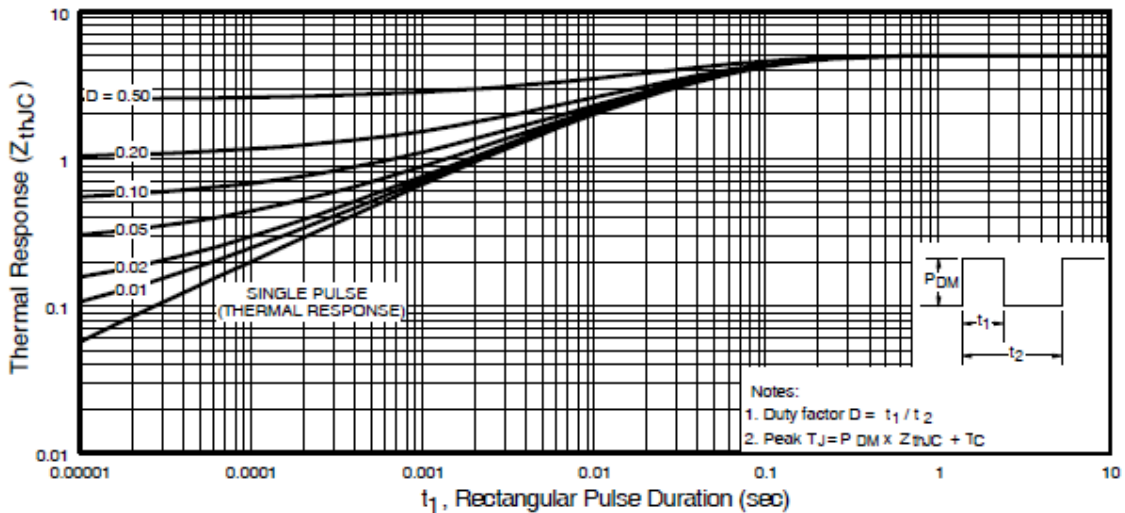


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

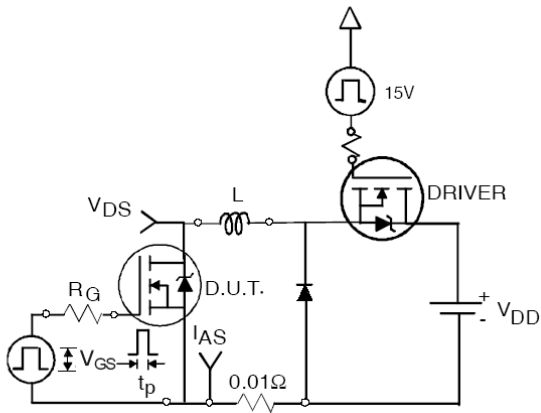


Fig 12a. Unclamped Inductive Test Circuit

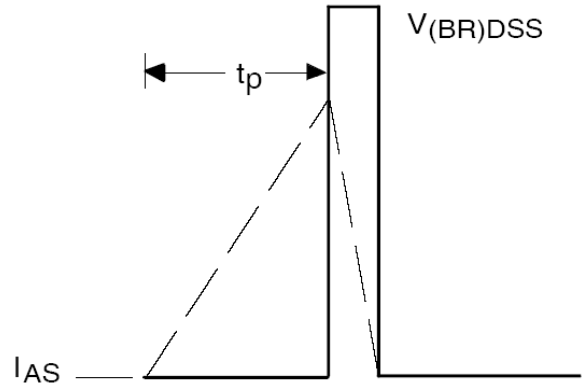


Fig 12b. Unclamped Inductive Waveforms

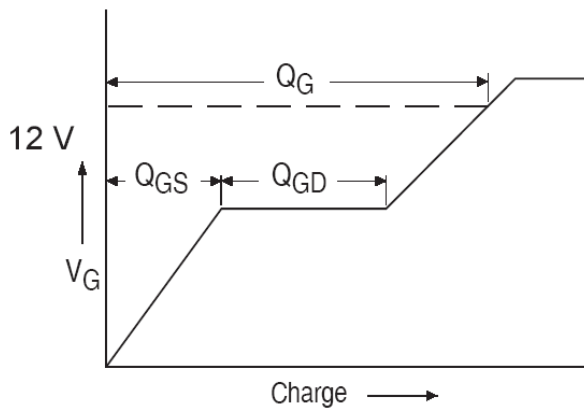


Fig 13a. Gate Charge Waveform

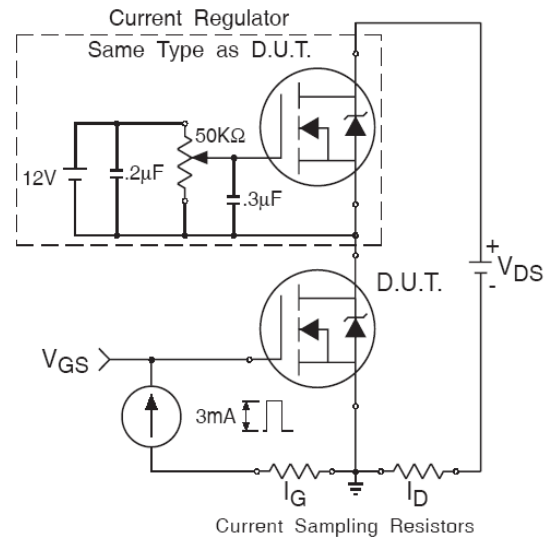


Fig 13b. Gate Charge Test Circuit

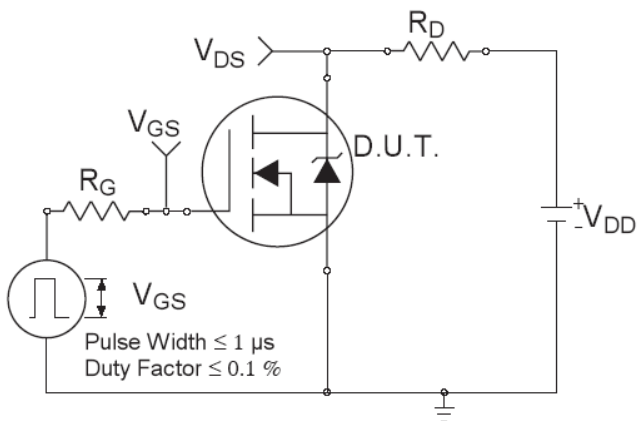


Fig 14a. Switching Time Test Circuit

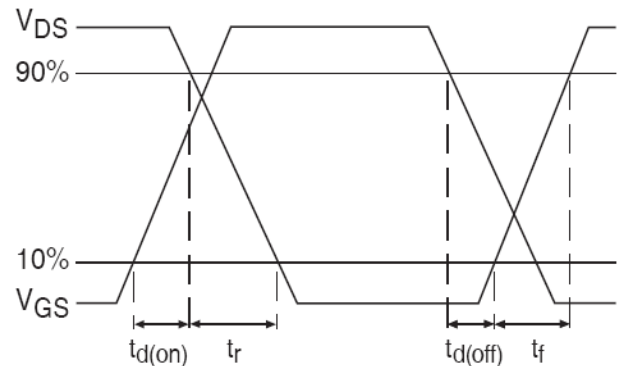
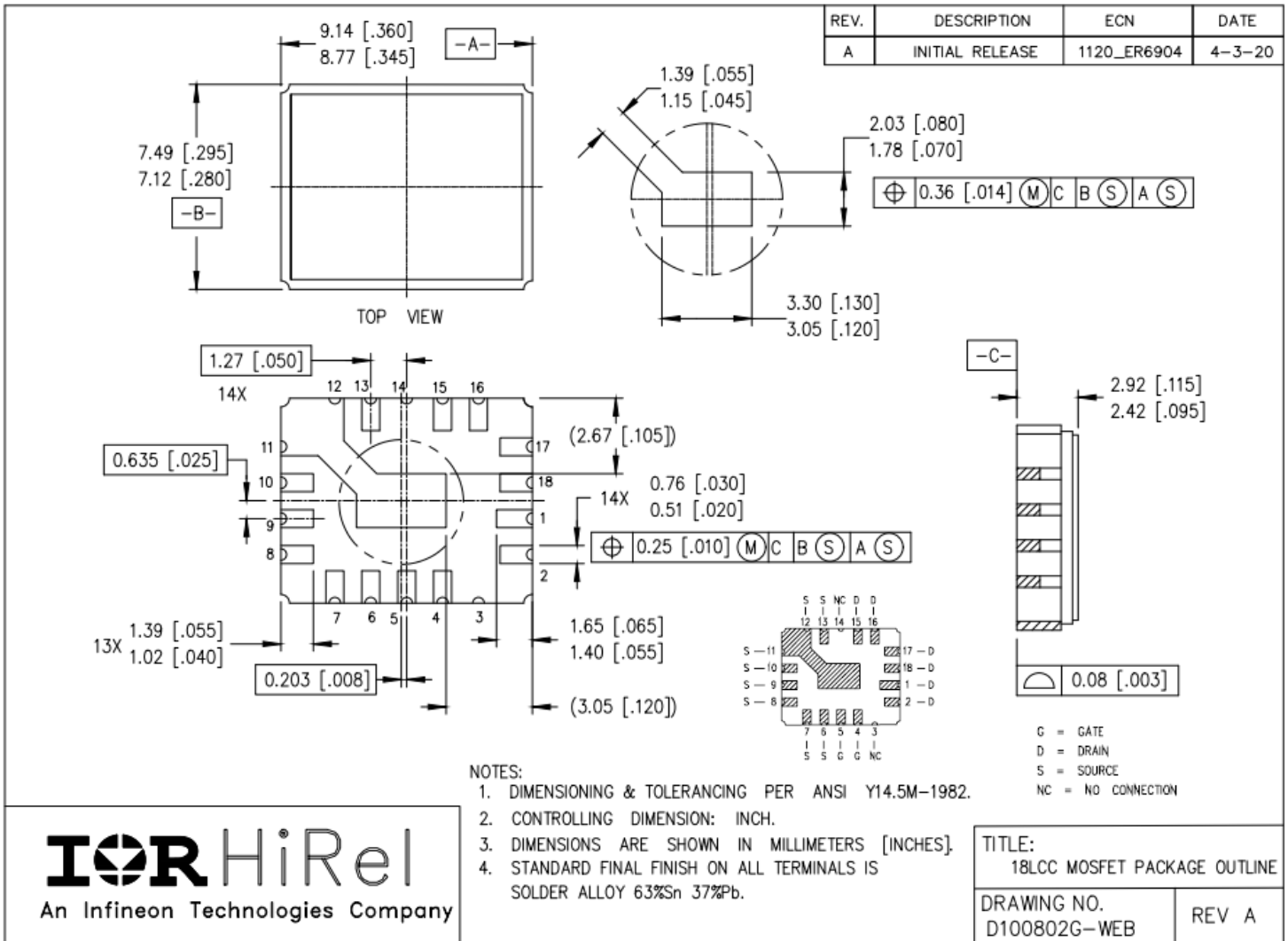


Fig 14b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: [LCC-18](#)

Case Outline and Dimensions — LCC-18



- NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.

IMPORTANT NOTICE

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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