Applications
- High frequency DC-DC converters
- Motor Control
- Uninterruptible Power Supplies

Benefits
- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective $C_{oss}$ to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DSS}$</td>
<td>100V</td>
<td></td>
</tr>
<tr>
<td>$R_{DS(on)}$ max</td>
<td>0.014Ω</td>
<td></td>
</tr>
<tr>
<td>$I_D$</td>
<td>75A</td>
<td></td>
</tr>
</tbody>
</table>

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_D$ @ $T_C = 25°C$</td>
<td>Continuous Drain Current, $V_{GS} @ 10V$</td>
<td>75</td>
</tr>
<tr>
<td>$I_D$ @ $T_C = 100°C$</td>
<td>Continuous Drain Current, $V_{GS} @ 10V$</td>
<td>53</td>
</tr>
<tr>
<td>$I_{DM}$</td>
<td>Pulsed Drain Current $\oplus$</td>
<td>300</td>
</tr>
<tr>
<td>$P_D @ T_A = 25°C$</td>
<td>Power Dissipation $\oplus$</td>
<td>3.8</td>
</tr>
<tr>
<td>$P_D @ T_C = 25°C$</td>
<td>Power Dissipation</td>
<td>200</td>
</tr>
<tr>
<td>Linear Derating Factor</td>
<td></td>
<td>1.4</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate-to-Source Voltage</td>
<td>± 20</td>
</tr>
<tr>
<td>$dv/dt$</td>
<td>Peak Diode Recovery $dv/dt$ $\oplus$</td>
<td>8.2</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating Junction and</td>
<td>-55 to +175</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage Temperature Range</td>
<td></td>
</tr>
<tr>
<td>Soldering Temperature, for 10 seconds</td>
<td>300 (1.6mm from case)</td>
<td></td>
</tr>
<tr>
<td>Mounting torque, 6-32 or M3 screw $\oplus$</td>
<td>10 lbf•in (1.1N•m)</td>
<td></td>
</tr>
</tbody>
</table>

Thermal Resistance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JJC}$</td>
<td>Junction-to-Case</td>
<td>——</td>
<td>0.74</td>
</tr>
<tr>
<td>$R_{JC}$</td>
<td>Case-to-Sink, Flat, Greased Surface $\oplus$</td>
<td>0.50</td>
<td>——</td>
</tr>
<tr>
<td>$R_{JA}$</td>
<td>Junction-to-Ambient $\oplus$</td>
<td>——</td>
<td>62</td>
</tr>
<tr>
<td>$R_{JA}$</td>
<td>Junction-to-Ambient $\oplus$</td>
<td>——</td>
<td>40</td>
</tr>
</tbody>
</table>
### Static @ T_J = 25°C (unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{BR\text{DSS}} )</td>
<td>100</td>
<td></td>
<td></td>
<td>V</td>
<td>( V_{GS} = 0V, I_D = 250\mu A )</td>
</tr>
<tr>
<td>( \Delta V_{BR\text{DSS}}/\Delta T_J )</td>
<td>0.11</td>
<td></td>
<td></td>
<td>V/°C</td>
<td>Reference to 25°C, ( I_D = 1mA )</td>
</tr>
</tbody>
</table>
| \( R_{DS\text{(on)}} \) Static Drain-to-Source On-Resistance | 0.011 | 0.014 |      | Ω     | \( V_{GS} = 10V, I_D = 45A \)  
| \( V_{GS\text{(th)}} \) Gate Threshold Voltage | 3.5  | 5.5  |      | V     | \( V_{DS} = V_{GS}, I_D = 250\mu A \) |
| \( I_{DSS} \) Drain-to-Source Leakage Current |      | 1.0  |      | μA    | \( V_{DS} = 95V, V_{GS} = 0V \)  
| \( I_{GSS} \) Gate-to-Source Forward Leakage |      | 100  |      | nA    | \( V_{GS} = 20V \)  
| \( I_{GSS} \) Gate-to-Source Reverse Leakage |      | -100 |      | V     | \( V_{GS} = -20V \)  

### Dynamic @ T_J = 25°C (unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
</table>
| \( g_f \) Forward Transconductance | 35   |      |      | S     | \( V_{DS} = 50V, I_D = 45A \)  
| \( Q_g \) Total Gate Charge |      | 110  | 170  | nC    | \( I_D = 45A \)  
| \( Q_{gs} \) Gate-to-Source Charge |      | 43   |      | nC    | \( V_{DS} = 50V \)  
| \( Q_{gd} \) Gate-to-Drain ("Miller") Charge |      | 40   |      | nC    | \( V_{GS} = 10V \)  
| \( t_{on} \) Turn-On Delay Time |      | 35   |      | ns    | \( V_{DD} = 50V \)  
| \( t_r \) Rise Time |      | 130  |      | ns    | \( I_D = 45A \)  
| \( t_{off} \) Turn-Off Delay Time |      | 41   |      | ns    | \( R_G = 4.5Ω \)  
| \( t_f \) Fall Time |      | 38   |      | ns    | \( V_{GS} = 10V \)  
| \( C_{iss} \) Input Capacitance |      | 6160 |      | pF    | \( V_{GS} = 0V \)  
| \( C_{oss} \) Output Capacitance |      | 440  |      | pF    | \( V_{DS} = 25V \)  
| \( C_{rss} \) Reverse Transfer Capacitance |      | 250  |      | pF    | \( f = 1.0MHz \)  
| \( C_{oss} \) Output Capacitance |      | 1580 |      | pF    | \( V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz \)  
| \( C_{oss} \) Output Capacitance |      | 280  |      | pF    | \( V_{GS} = 0V \)  
| \( C_{oss\text{eff.}} \) Effective Output Capacitance |      | 430  |      | pF    | \( V_{GS} = 0V, V_{DS} = 0V \) to 80V  

### Avalanche Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( E_{AS} ) Single Pulse Avalanche Energy</td>
<td></td>
<td>190</td>
<td>mJ</td>
</tr>
<tr>
<td>( I_{AR} ) Avalanche Current</td>
<td></td>
<td>45</td>
<td>A</td>
</tr>
<tr>
<td>( E_{AR} ) Repetitive Avalanche Energy</td>
<td></td>
<td>20</td>
<td>mJ</td>
</tr>
</tbody>
</table>

### Diode Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
</table>
| \( I_S \) Continuous Source Current (Body Diode) |      | 75   |      | A     | MOSFET symbol showing the integral reverse p-n junction diode.  
| \( I_{SM} \) Pulsed Source Current (Body Diode) |      | 300  |      | A     | MOSFET symbol showing the integral reverse p-n junction diode.  
| \( V_{SD} \) Diode Forward Voltage |      | 1.3  |      | V     | \( T_J = 25°C, I_S = 45A, V_{GS} = 0V \)  
| \( t_r \) Reverse Recovery Time |      | 74   | 110  | ns    | \( T_J = 25°C, I_F = 45A \)  
| \( Q_{rr} \) Reverse RecoveryCharge |      | 180  | 260  | nC    | di/dt = 100A/μs  
| \( I_{on} \) Forward Turn-On Time |      |      |      |       | Intrinsic turn-on time is negligible (turn-on is dominated by \( I_{on}\text{LD} \))  

2 www.irf.com
Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance Vs. Temperature
Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area
Fig 9. Maximum Drain Current Vs. Case Temperature

Fig 10a. Switching Time Test Circuit

Fig 10b. Switching Time Waveforms

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case
IRFB/IRFS/IRFL4710

Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Fig 13a. Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit
Peak Diode Recovery $\frac{dv}{dt}$ Test Circuit

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance
- Current Transformer

- $\frac{dv}{dt}$ controlled by $R_G$
- Driver same type as D.U.T.
- $I_{SD}$ controlled by Duty Factor "D"
- D.U.T. - Device Under Test

Driver Gate Drive
- P.W. Period
- $D = \frac{P.W.}{\text{Period}}$
- $V_{GS} = 10V$

D.U.T. $I_{SD}$ Waveform
- Reverse Recovery Current
- Body Diode Forward Current
- $\frac{dv}{dt}$

D.U.T. $V_{DS}$ Waveform
- Diode Recovery $\frac{dv}{dt}$
- $V_{DD}$

Re-Applied Voltage
- Inductor Current
- Body Diode Forward Drop
- Ripple $\leq 5\%$
- $I_{SD}$

* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs
IRFB/IRFS/IRFL4710

TO-220AB Package Outline
Dimensions are shown in millimeters (inches)

NOTES:
2. CONTROLLING DIMENSION: INCH
3. OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4. HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010 WITH ASSEMBLY LOT CODE 9B1M

PART NUMBER
INTERNATIONAL RECTIFIER LOGO
ASSEMBLY LOT CODE
DATE CODE (YYWW)
YY = YEAR
WW = WEEK
D^2Pak Package Outline

NOTES:
1 DIMENSIONS AFTER SOLDER DIP.
3 CONTROLLING DIMENSION : INCH.
4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

D^2Pak Part Marking Information

INTERNATIONAL RECTIFIER
LOGO
ASSEMBLY LOT CODE
PART NUMBER
DATE CODE (YYWW)
YY = YEAR
WW = WEEK

www.irf.com
IRFB/IRFS/IRFL4710

TO-262 Package Outline

LEAD ASSIGNMENTS
1 = GATE  3 = SOURCE
2 = DRAIN  4 = DRAIN

NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

INTERNATIONAL
RECTIFIER
LOGO

IRL3103L
719C
17
89

PART NUMBER

DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C

www.irf.com
Repetitive rating; pulse width limited by max. junction temperature.

\[ \text{ISD} \leq 45 \text{A}, \text{di/dt} \leq 420 \text{A/µs}, \text{V}_{\text{DD}} \leq \text{V(BR)DSS} \]

\[ \text{T}_\text{J} \leq 175°C \]

Notes:
1. Starting \( T_J = 25°C \), \( L = 190\mu\text{H} \)
2. \( R_S = 25\Omega \), \( I_{\text{AS}} = 45\text{A} \), \( V_{\text{GS}} = 10\text{V} \)
3. \( \text{ISO} \leq 45\text{A}, \text{di/dt} \leq 420\text{A/µs}, \text{V}_{\text{DD}} \leq \text{V(BR)DSS}, \text{T}_J \leq 175°C \)
4. Pulse width \( \leq 400\mu\text{s}; \text{duty cycle} \leq 2\% \).
5. \( C_{\text{oss eff.}} \) is a fixed capacitance that gives the same charging time as \( C_{\text{oss}} \) while \( V_{\text{DS}} \) is rising from 0 to 80% \( V_{\text{DSS}} \)
6. This is only applied to TO-220AB package

This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR’s Web site.
Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/