

**HEXFET® POWER MOSFET
 SURFACE MOUNT (SMD-2)**

**IRF7NA2907
 75V, N-CHANNEL**

Product Summary

Part Number	BV _{DSS}	R _{DS(on)}	I _D
IRF7NA2907	75V	0.0045Ω	75A*



SMD-2

Seventh Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon unit area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

These devices are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high-energy pulse circuits.

Features:

- Low R_{DS(on)}
- Avalanche Energy Ratings
- Dynamic dv/dt Rating
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Light Weight

Absolute Maximum Ratings

	Parameter		Units
I _D @ V _{GS} = 10V, T _C = 25°C	Continuous Drain Current	75*	A
I _D @ V _{GS} = 10V, T _C = 100°C	Continuous Drain Current	75*	
I _{DM}	Pulsed Drain Current ①	300	
P _D @ T _C = 25°C	Max. Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V _{GS}	Gate-to-Source Voltage	±20	V
E _{AS}	Single Pulse Avalanche Energy ②	500	mJ
I _{AR}	Avalanche Current ①	75	A
E _{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.4	V/ns
T _J	Operating Junction	-55 to 150	°C
T _{STG}	Storage Temperature Range		
	Package Mounting Surface Temp.	300 (for 5s)	
	Weight	3.3 (Typical)	g

* Current is limited by package

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	75	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔBVDSS/ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.08	—	V/°C	Reference to 25°C, I _D = 1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	0.0045	Ω	V _{GS} = 10V, I _D = 75A ④
VGS(th)	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
gfs	Forward Transconductance	130	—	—	S	V _{DS} = 15V, I _{DS} = 75A ④
IDSS	Zero Gate Voltage Drain Current	—	—	20	μA	V _{DS} = 75V, V _{GS} = 0V
		—	—	250		V _{DS} = 60V, V _{GS} = 0V, T _J = 125°C
IGSS	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
IGSS	Gate-to-Source Leakage Reverse	—	—	-100	nA	V _{GS} = -20V
Qg	Total Gate Charge	—	—	375	nC	V _{GS} = 10V, I _D = 45A
Qgs	Gate-to-Source Charge	—	—	60		V _{DS} = 60V
Qgd	Gate-to-Drain ('Miller') Charge	—	—	150		
td(on)	Turn-On Delay Time	—	—	40	ns	V _{DD} = 38V, I _D = 45A, V _{GS} = 10V, R _G = 1.2Ω
tr	Rise Time	—	—	125		
td(off)	Turn-Off Delay Time	—	—	175		
tf	Fall Time	—	—	75		
LS + LD	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to the center of source pad
Ciss	Input Capacitance	—	12000	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
Coss	Output Capacitance	—	2280	—		
Crss	Reverse Transfer Capacitance	—	610	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	75*	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	300		
V _{SD}	Diode Forward Voltage	—	—	1.65	V	T _j = 25°C, I _S = 75A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	175	ns	T _j = 25°C, I _F = 45A, di/dt ≤ 100A/μs
QRR	Reverse Recovery Charge	—	—	850	nC	V _{DD} ≤ 25V ④
ton	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

* Current is limited by package

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	0.5	°C/W	

Note: Corresponding Spice and Saber models are available on the international Rectifier Website.

For footnotes refer to the last page

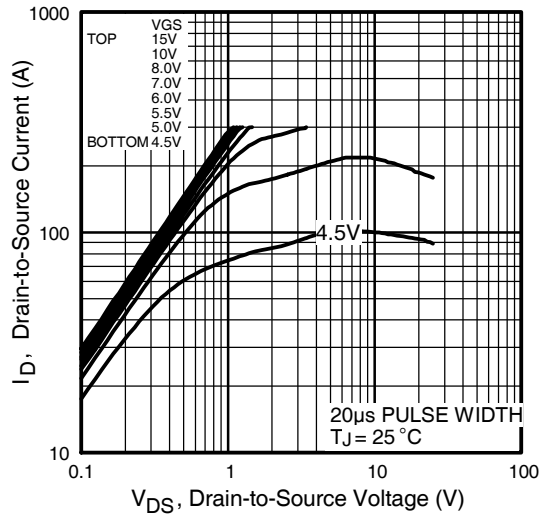


Fig 1. Typical Output Characteristics

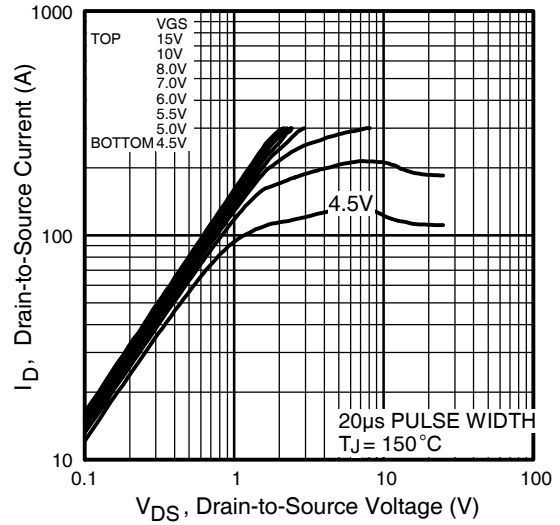


Fig 2. Typical Output Characteristics

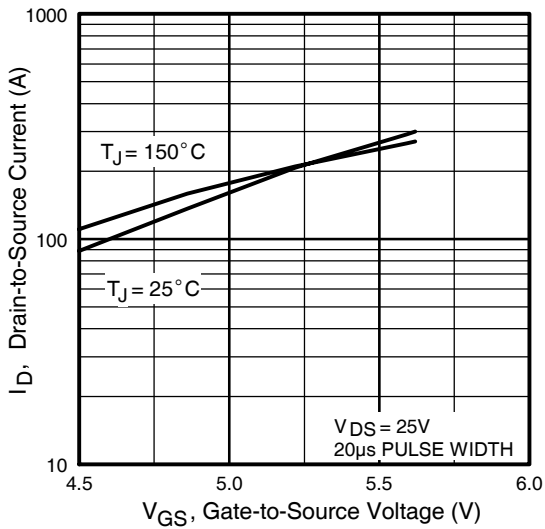


Fig 3. Typical Transfer Characteristics

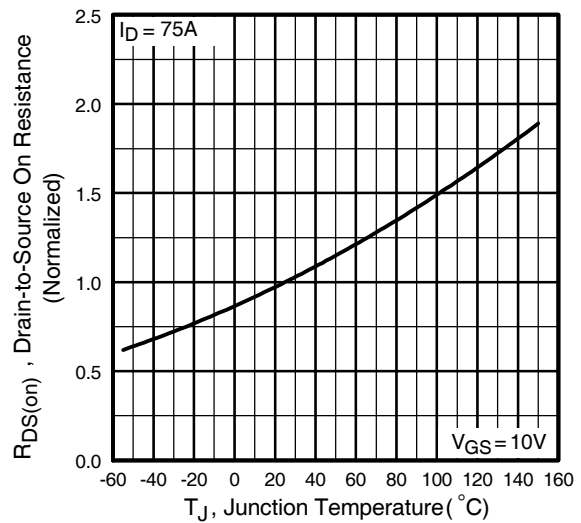


Fig 4. Normalized On-Resistance Vs. Temperature

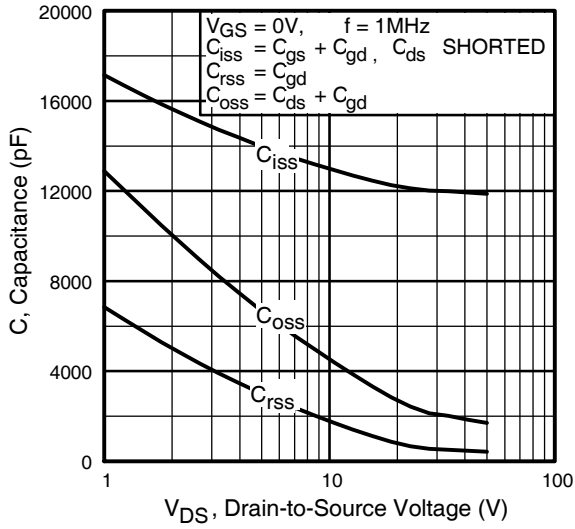


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

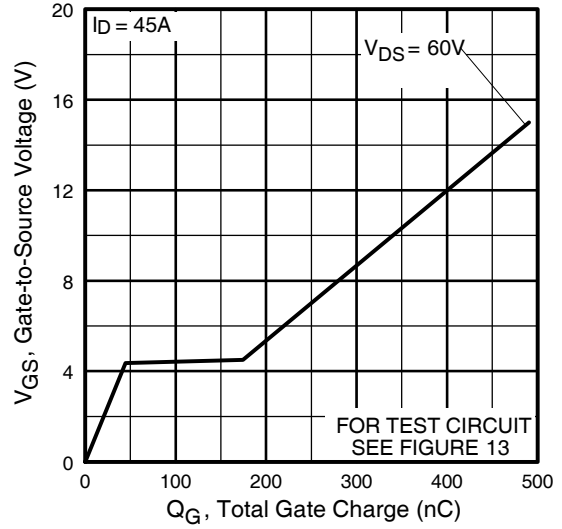


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

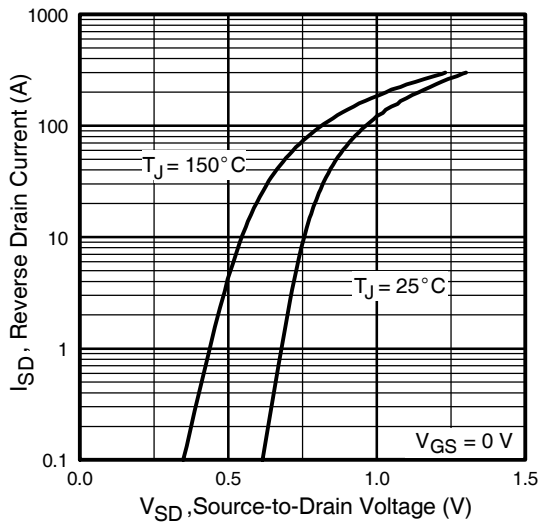


Fig 7. Typical Source-Drain Diode Forward Voltage

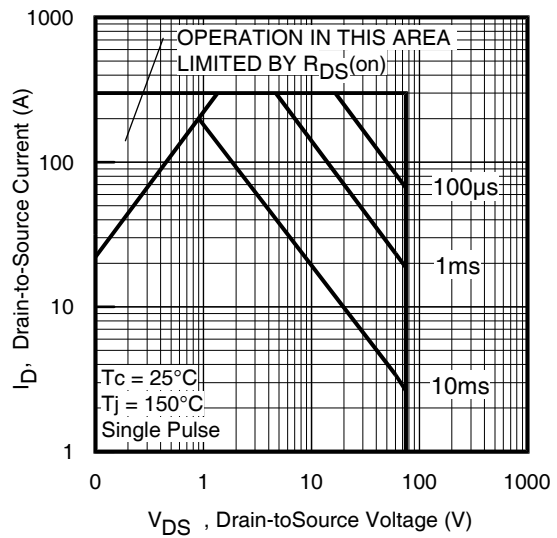


Fig 8. Maximum Safe Operating Area

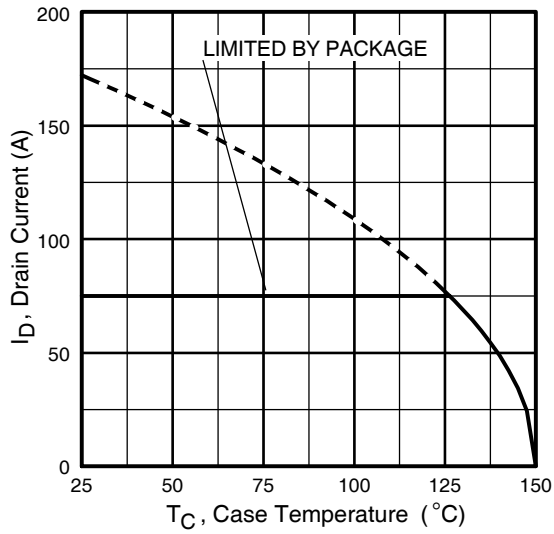


Fig 9. Maximum Drain Current Vs. Case Temperature

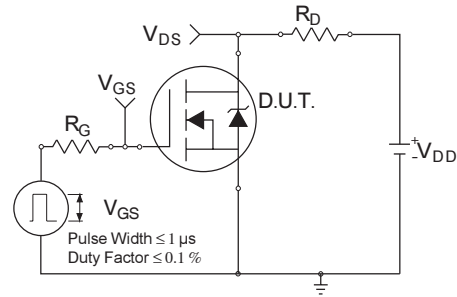


Fig 10a. Switching Time Test Circuit

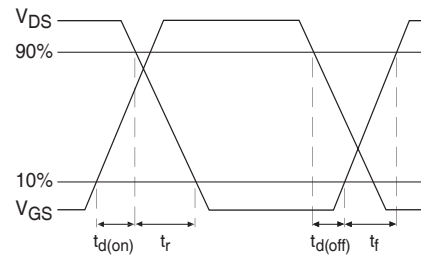


Fig 10b. Switching Time Waveforms

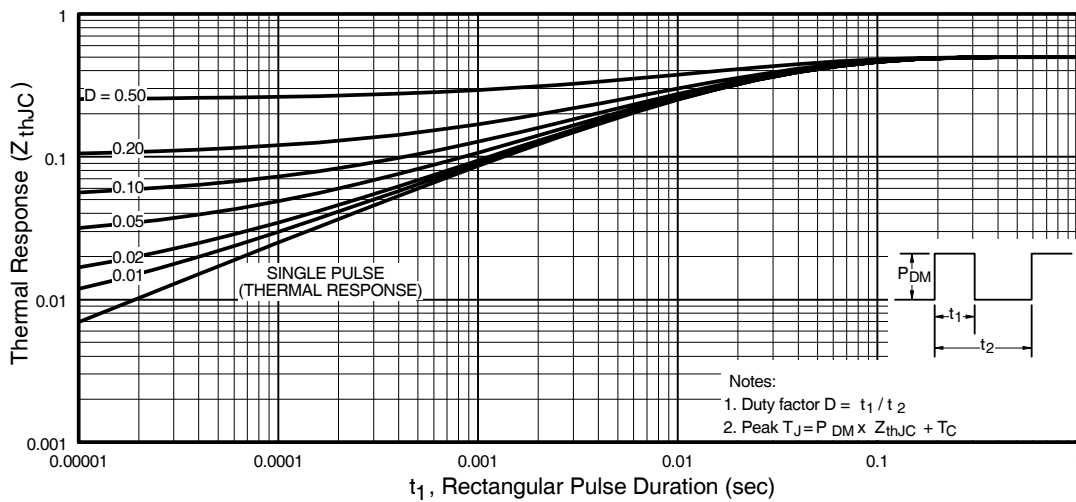


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

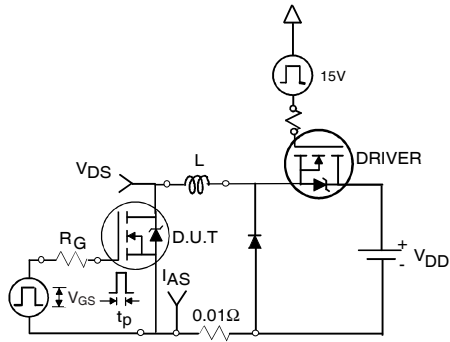


Fig 12a. Unclamped Inductive Test Circuit

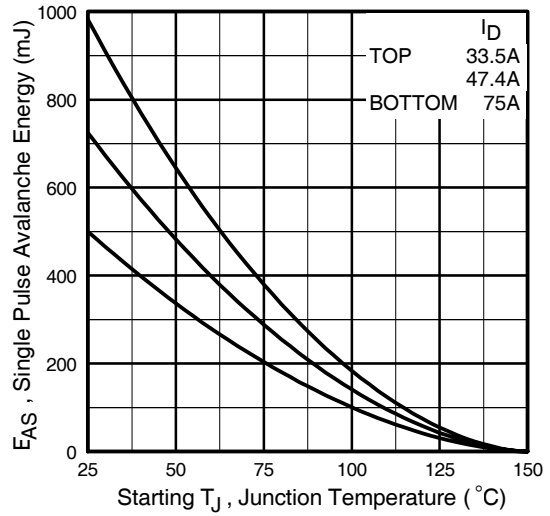


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

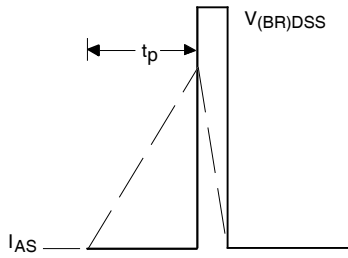


Fig 12b. Unclamped Inductive Waveforms

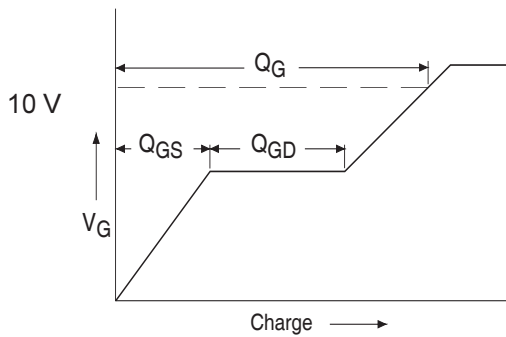


Fig 13a. Basic Gate Charge Waveform

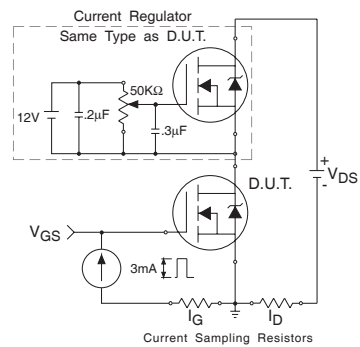
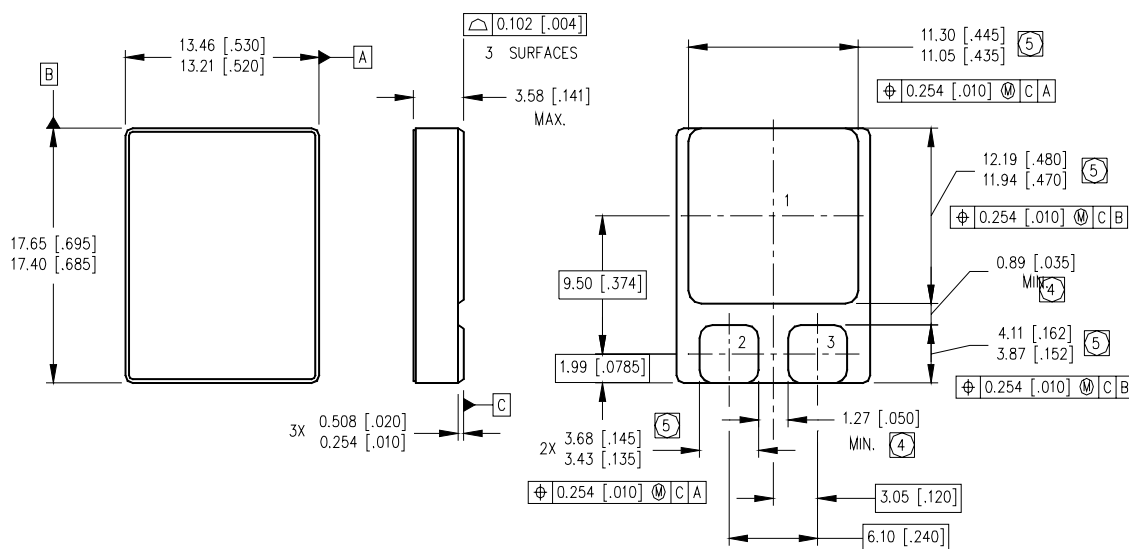


Fig 13b. Gate Charge Test Circuit

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25\text{ V}$, Starting $T_J = 25^\circ\text{C}$, $L = 0.17\text{mH}$
 Peak $I_{AS} = 75\text{A}$, $V_{GS} = 10\text{V}$, $R_G = 25\Omega$
- ③ $I_{SD} \leq 45\text{A}$, $di/dt \leq 260\text{A}/\mu\text{s}$,
 $V_{DD} \leq 75\text{V}$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\ \mu\text{s}$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions — SMD-2



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

- ④ DIMENSION INCLUDES METALLIZATION FLASH.
- ⑤ DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

- 1 = DRAIN
- 2 = GATE
- 3 = SOURCE