

IRF7484QPbF

HEXFET® Power MOSFET

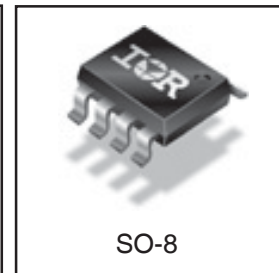
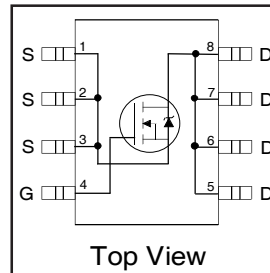
Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Fast Switching
- Repetitive Avalanche Allowed up to T_{jmax}
- Lead-Free
- RoHS Compliant (Halogen Free)

V_{DSS}	$R_{DS(on)}$ max (m Ω)	I_D
40V	10 @ $V_{GS} = 7.0V$	14A

Description

This Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	14	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	11	
I_{DM}	Pulsed Drain Current ①	110	A
$P_D @ T_A = 25^\circ C$	Power Dissipation ③	2.5	W
	Linear Derating Factor	0.02	W/°C
V_{GS}	Gate-to-Source Voltage	± 8.0	V
E_{AS}	Single Pulse Avalanche Energy ④	230	mJ
I_{AR}	Avalanche Current ①	See Fig.16c, 16d, 19, 20	A
E_{AR}	Repetitive Avalanche Energy ④		mJ
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	—	20	°C/W
$R_{\theta JA}$	Junction-to-Ambient ③	—	50	

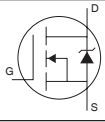
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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.040	—	V/°C	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	10	mΩ	$V_{GS} = 7.0V, I_D = 14A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	40	—	—	S	$V_{DS} = 10V, I_D = 14A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 32V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 8.0V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -8.0V$
Q_g	Total Gate Charge	—	69	100	nC	$I_D = 14A$
Q_{gs}	Gate-to-Source Charge	—	9.0	—		$V_{DS} = 32V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	16	—		$V_{GS} = 7.0V$
$t_{d(on)}$	Turn-On Delay Time	—	9.3	—	ns	$V_{DD} = 20V$ ②
t_r	Rise Time	—	5.0	—		$I_D = 1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	180	—		$R_G = 6.2\Omega$
t_f	Fall Time	—	58	—		$V_{GS} = 7.0V$
C_{iss}	Input Capacitance	—	3520	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	660	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	76	—		$f = 1.0MHz$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	110		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 2.3A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	—	59	89	ns	$T_J = 25^\circ\text{C}, I_F = 2.3A$
Q_{rr}	Reverse Recovery Charge	—	110	170	nC	$di/dt = 100A/\mu s$ ②

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ③ Surface mounted on 1 in square Cu board.
- ④ Starting $T_J = 25^\circ\text{C}$, $L = 2.3mH$, $R_G = 25\Omega$, $I_{AS} = 14A$. (See Figure 12).
- ⑤ $I_{SD} \leq 14A$, $di/dt \leq 140A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.
- ⑥ Limited by T_{Jmax} , see Fig.16c, 16d, 19, 20 for typical repetitive avalanche performance.

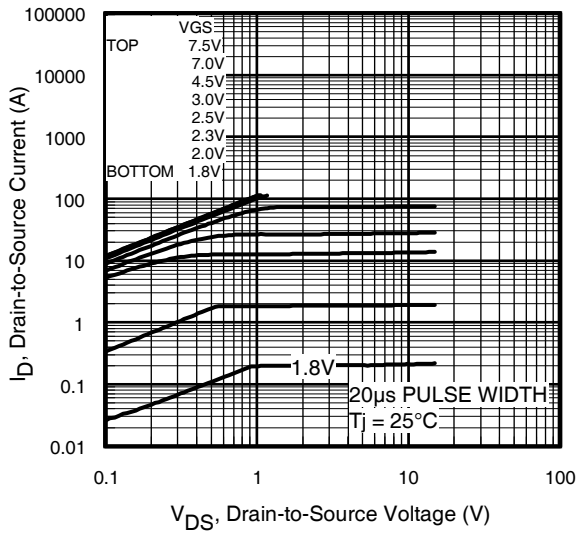


Fig 1. Typical Output Characteristics

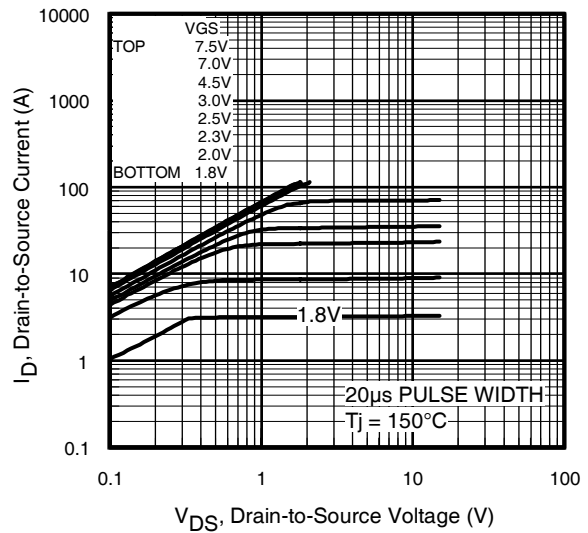


Fig 2. Typical Output Characteristics

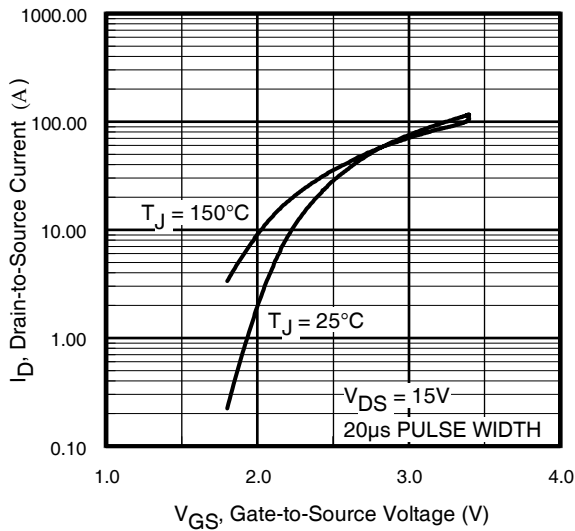


Fig 3. Typical Transfer Characteristics

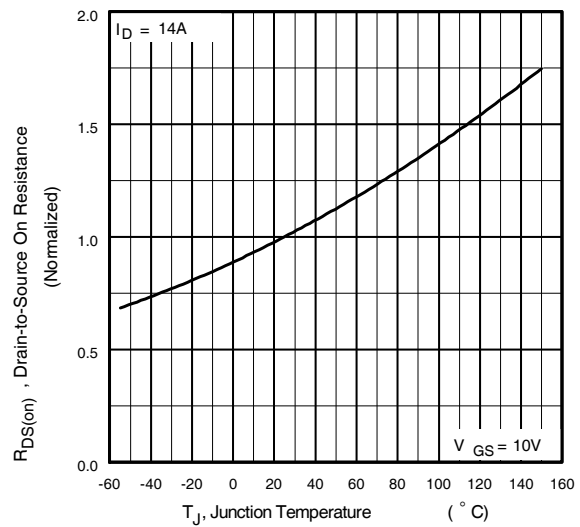


Fig 4. Normalized On-Resistance Vs. Temperature

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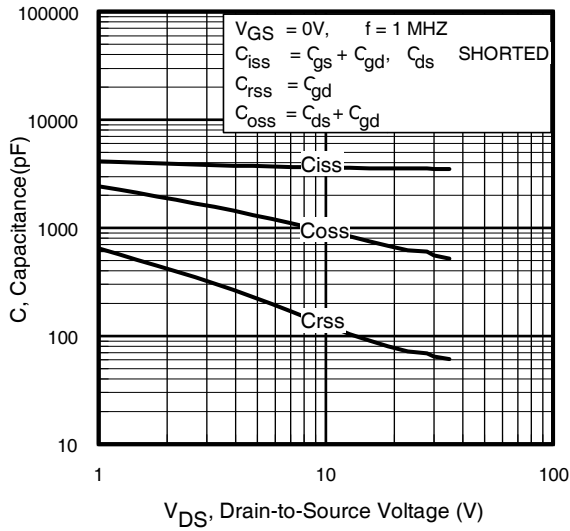


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

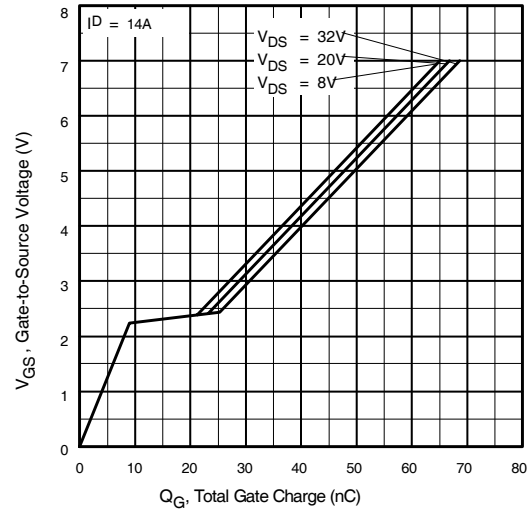


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

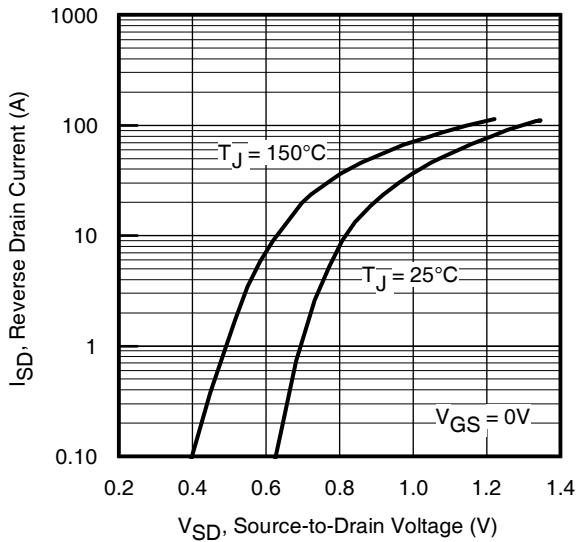


Fig 7. Typical Source-Drain Diode Forward Voltage

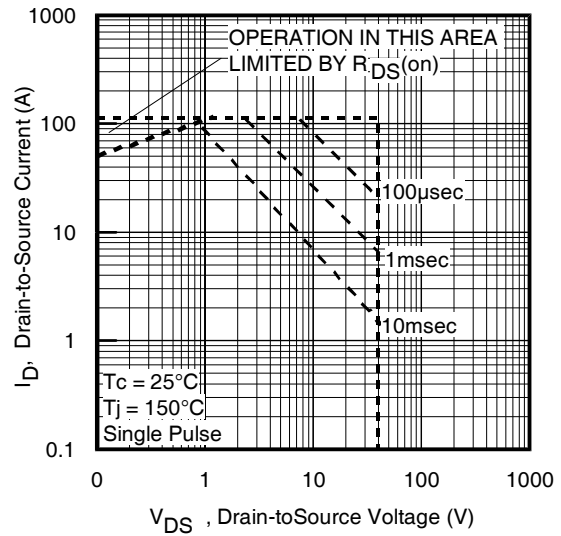


Fig 8. Maximum Safe Operating Area

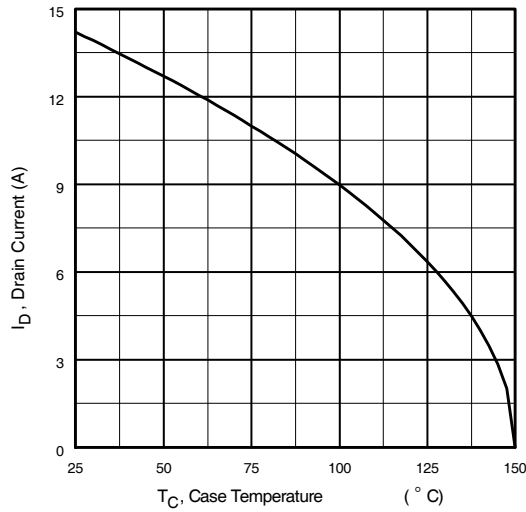


Fig 9. Maximum Drain Current Vs. Case Temperature

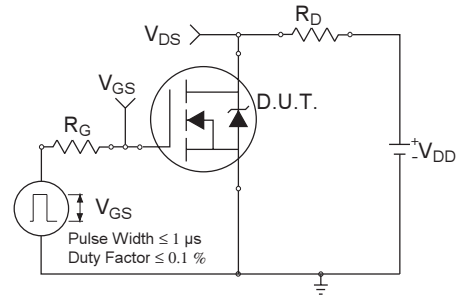


Fig 10a. Switching Time Test Circuit

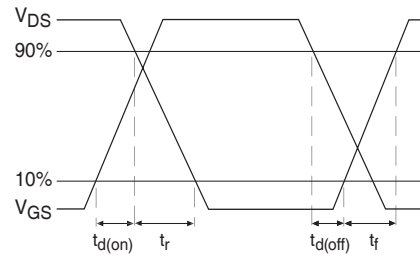


Fig 10b. Switching Time Waveforms

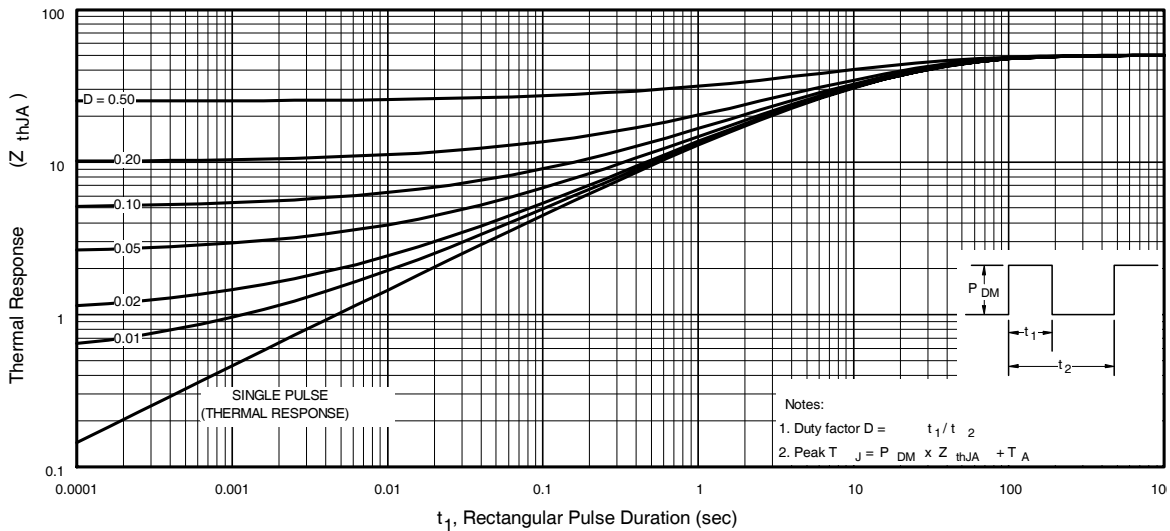


Fig 11. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

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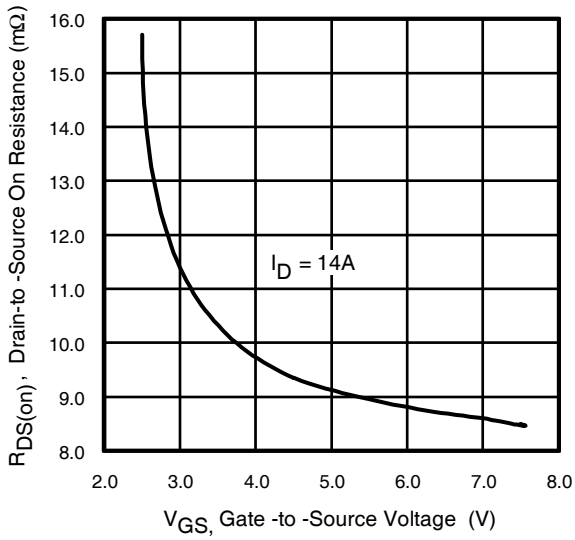


Fig 12. Typical On-Resistance Vs. Gate Voltage

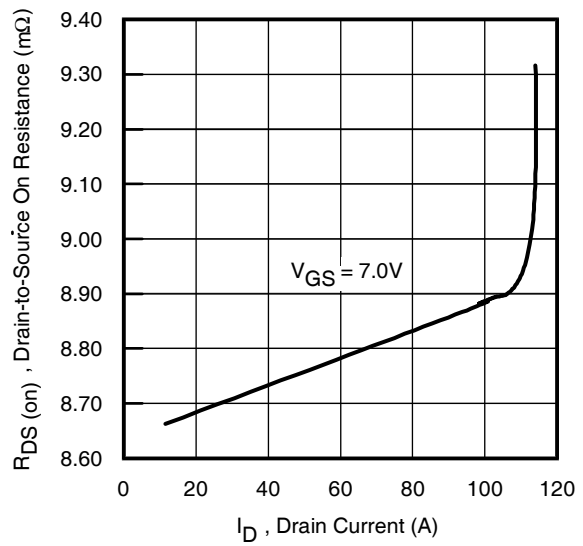


Fig 13. Typical On-Resistance Vs. Drain Current

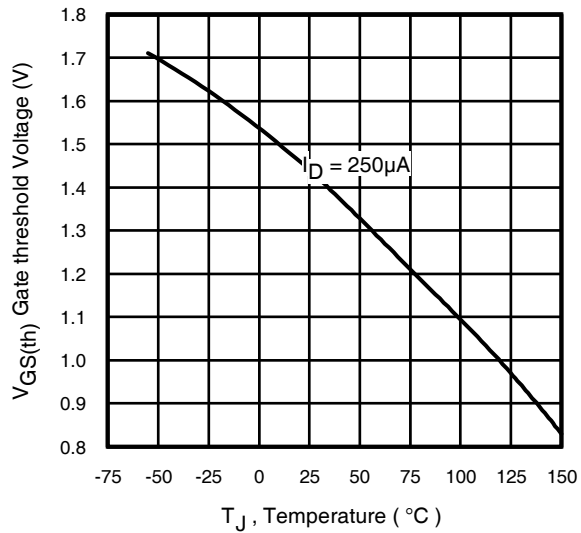


Fig 14. Typical Threshold Voltage Vs. Junction Temperature

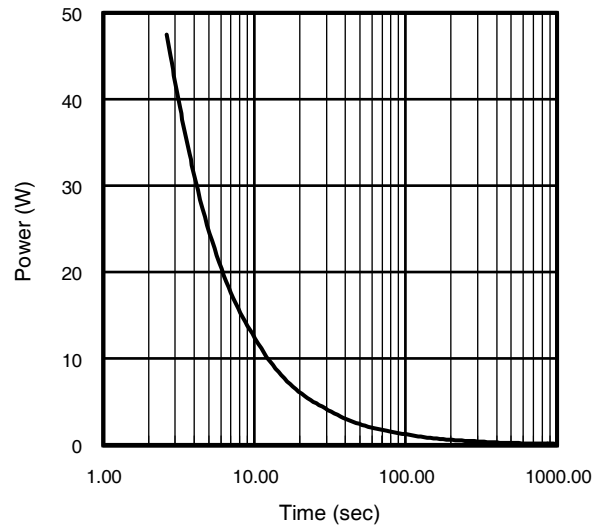


Fig 15. Typical Power Vs. Time

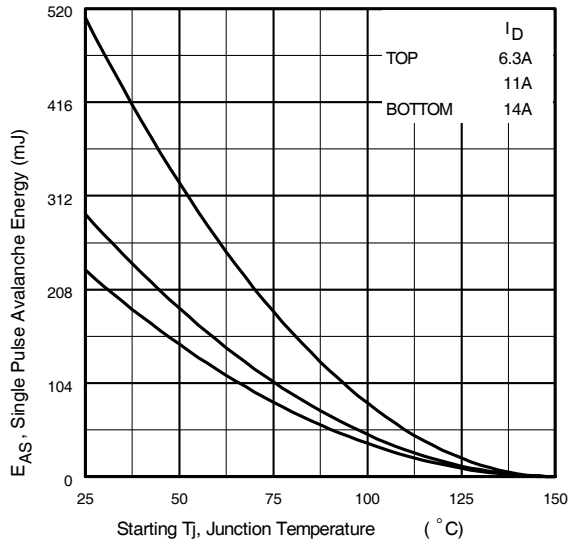


Fig 16a. Maximum Avalanche Energy Vs. Drain Current

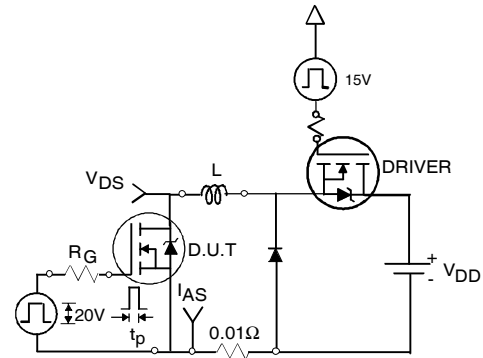


Fig 16c. Unclamped Inductive Test Circuit

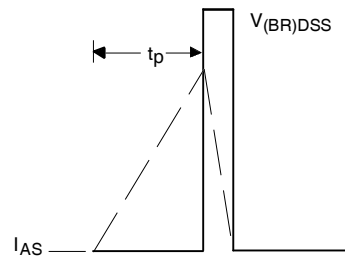


Fig 16d. Unclamped Inductive Waveforms

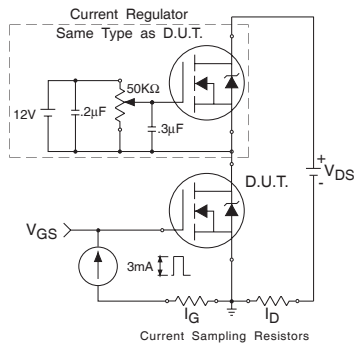


Fig 17. Gate Charge Test Circuit

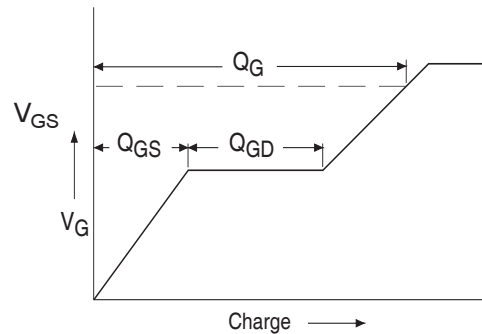


Fig 18. Basic Gate Charge Waveform

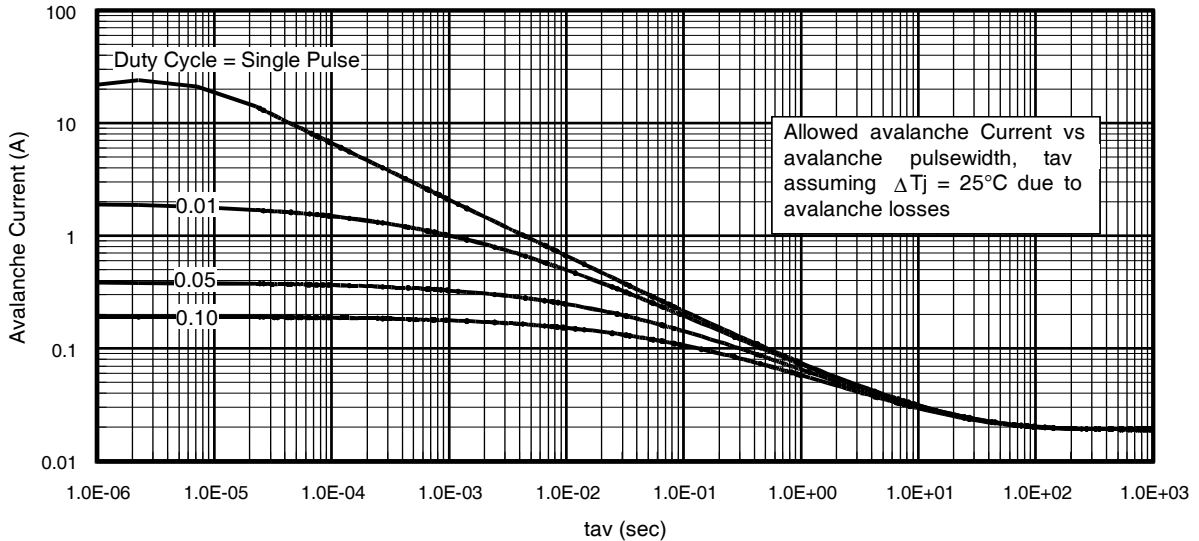


Fig 19. Typical Avalanche Current Vs.Pulsewidth

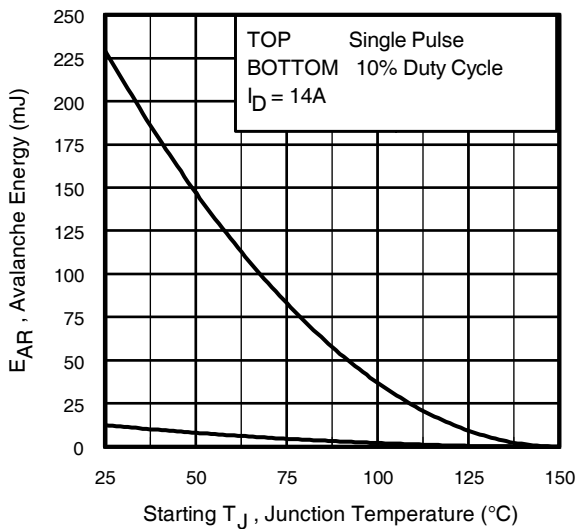


Fig 20. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

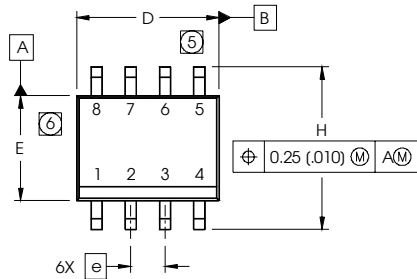
$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

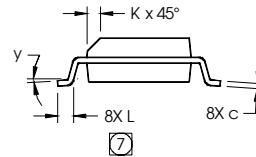
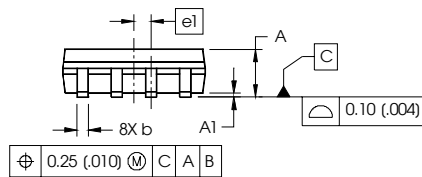
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

SO-8 Package Outline (MOSFET & Fetky)

Dimensions are shown in millimeters (inches)

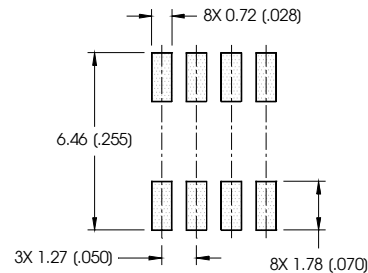


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



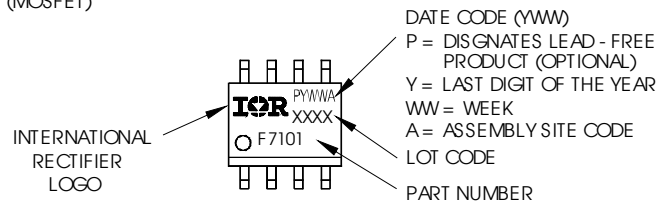
- NOTES:
- DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
 - CONTROLLING DIMENSION: MILLIMETER
 - DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 - OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
 - DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
 - DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
 - DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking Information

EXAMPLE: THIS IS AN IRF7101 (MOSFET)



Notes:

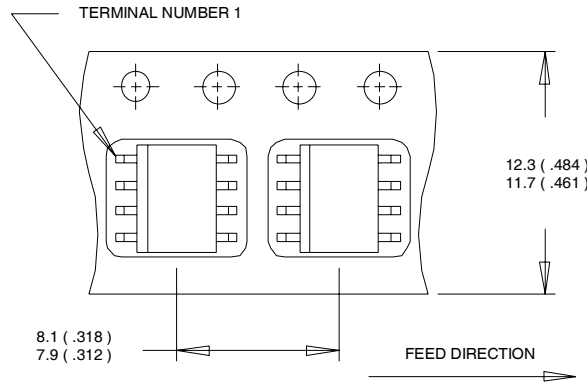
- For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
- For the most current drawing please refer to IR website at <http://www.irf.com/package/>

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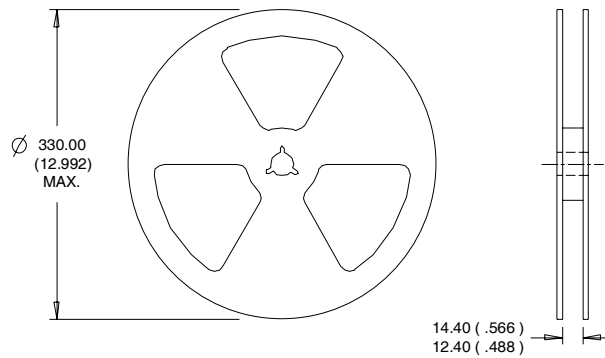
SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

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