PD -95492

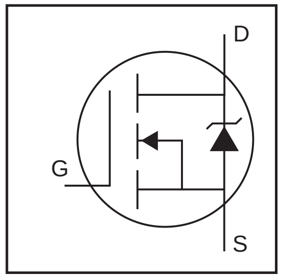
International
IOR Rectifier

AUTOMOTIVE MOSFET IRF1704PbF

HEXFET® Power MOSFET

Benefits

- 200°C Operaing Temperature
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- Fast Switching
- Repetitive Avalanche Allowed up to Tj Max
- Automotive Qualified (Q101)
- Lead-Free



V_{DSS} = 40V

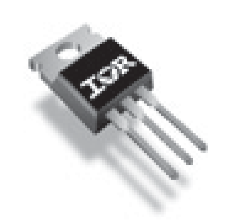
$R_{DS(on)}$ = 0.004Ω

I_D = 170A⑥

Description

Specifically designed for Automotive applications, this HEXFET® power MOSFET has a 200°C max operating temperature with a Stripe Planar design that utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET® power MOSFET are fast switching speed and improved repetitive avalanche rating.

The continuing technology leadership of Internationl Rectifier provides 200°C operating temperature in a plastic package. At high ambient temperatures, the IRF1704 can carry up to 20% more current than similar 175 °C Tj max devices in the same package outline. This makes this part ideal for existing and emerging under-the-hood automotive applications such as Electric Power Steering (EPS), Fuel / Water Pump Control and wide variety of other applications.



TO-220AB

Absolute Maximum Ratings

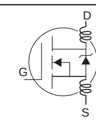
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	170⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	120	
I_{DM}	Pulsed Drain Current ①	680	
P_D @T_C = 25°C	Power Dissipation	230	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	670	mJ
I_{AR}	Avalanche Current①	100	A
E_{AR}	Repetitive Avalanche Energy①	23	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.9	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 200	°C
T_{LEAD}	Lead Temperature⑦	175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	°C
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

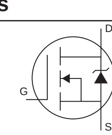
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

07/01/04

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.036	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	0.004	Ω	V_{GS} = 10V, I_D = 100A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	–––	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
		1.0	–––	–––		V_{DS} = V_{GS}, I_D = 5.0mA, T_J = 200°C
g_{fs}	Forward Transconductance	110	–––	–––	S	V_{DS} = 25V, I_D = 100A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	20	µA	V_{DS} = 40V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 32V, V_{GS} = 0V, T_J = 175°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-200		V_{GS} = -20V
Q_g	Total Gate Charge	–––	170	260	nC	I_D = 100A
Q_{gs}	Gate-to-Source Charge	–––	42	63		V_{DS} = 32V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	39	59		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	–––	16	–––	ns	V_{DD} = 20V
t_r	Rise Time	–––	120	–––		I_D = 100A
$t_{d(off)}$	Turn-Off Delay Time	–––	73	–––		R_G = 2.5Ω
t_f	Fall Time	–––	37	–––		V_{GS} = 10V,See Fig. 10 ④
L_D	Internal Drain Inductance	–––	4.5	–––	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	–––	7.5	–––		
C_{iss}	Input Capacitance	–––	6950	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	1660	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	200	–––		f = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	–––	6250	–––		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	–––	1470	–––		V_{GS} = 0V, V_{DS} = 32V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	–––	2320	–––		V_{GS} = 0V, V_{DS} = 0V to 32V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	170⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	680		
V_{SD}	Diode Forward Voltage	–––	–––	1.3	V	T_J = 25°C, I_S = 100A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	73	110	ns	T_J = 25°C, I_F = 100A
Q_{rr}	Reverse RecoveryCharge	–––	200	300	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)

② Starting T_J = 25°C, L = 0.13mH, V_{GS} = 10V R_G = 25Ω, I_{AS} = 100A. (See Figure 12)

③ $I_{SD} \le$ 100A, di/dt $\le$ 150A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 200°C

④ Pulse width $\le$ 400µs; duty cycle $\le$ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A

⑦ At the point of termination of the leads at the PCB, the temp. should be limited to 175°C. The device case temperature is allowed to be higher

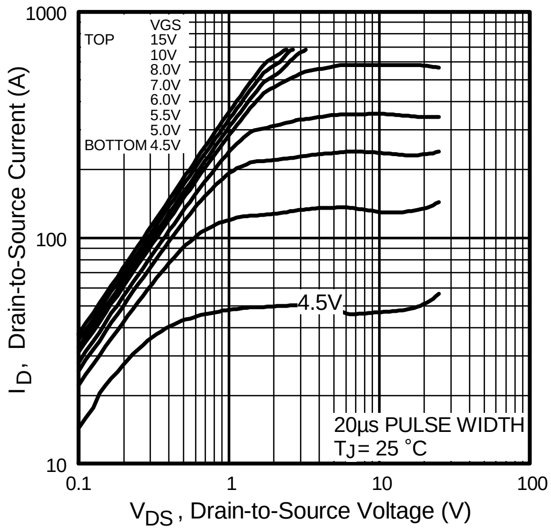


Fig 1. Typical Output Characteristics

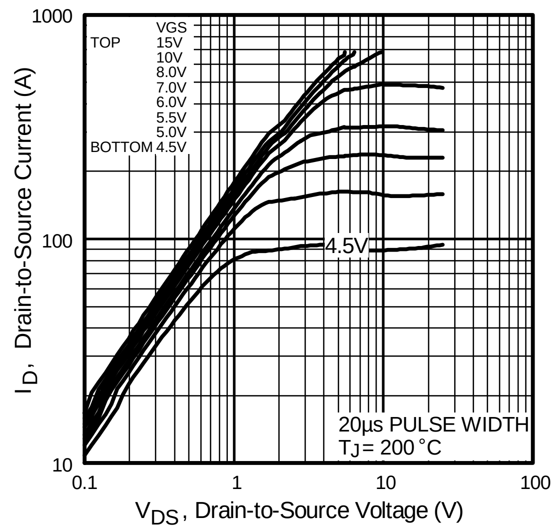


Fig 2. Typical Output Characteristics

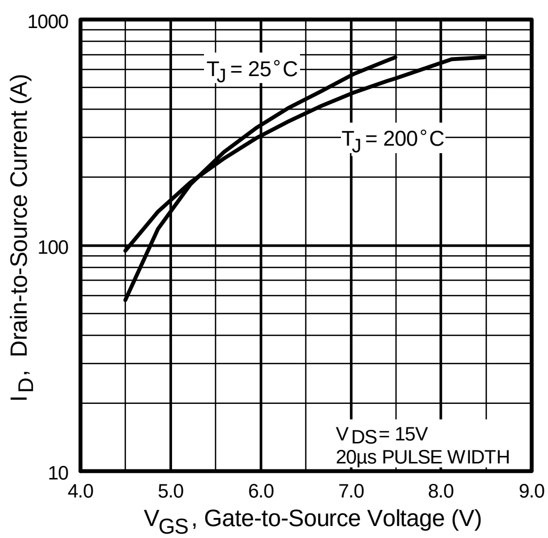


Fig 3. Typical Transfer Characteristics

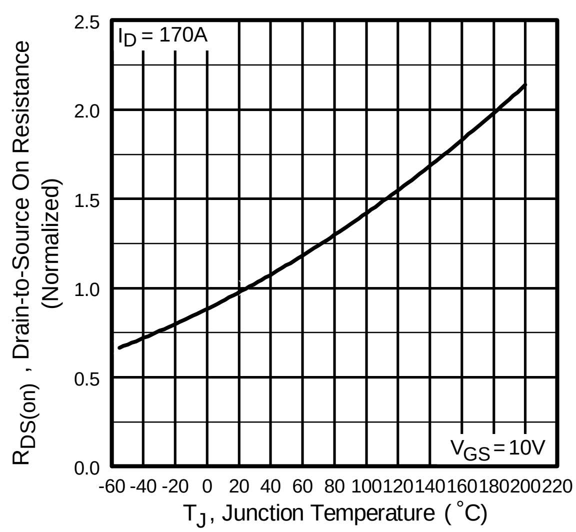


Fig 4. Normalized On-Resistance Vs. Temperature

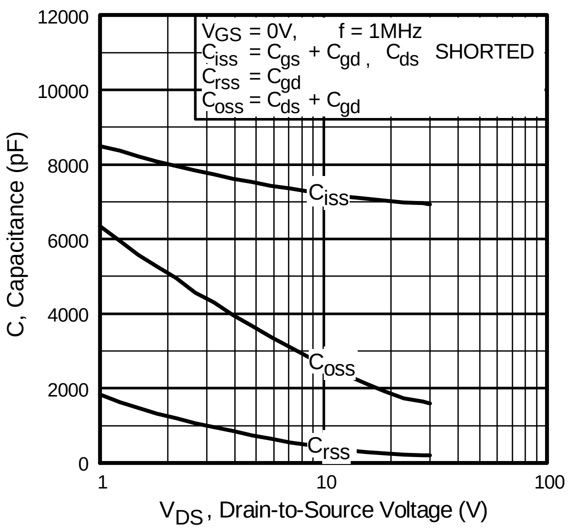


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

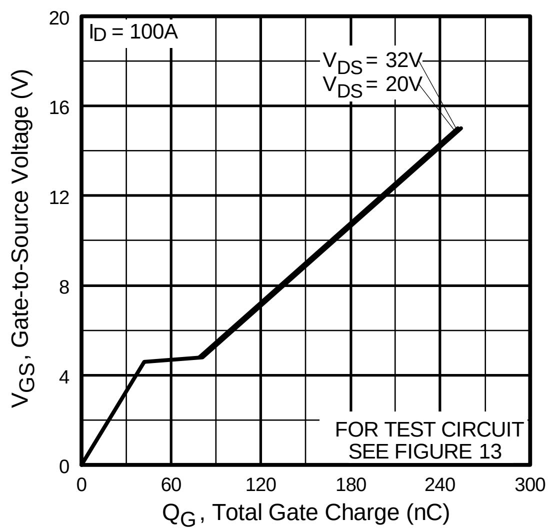


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

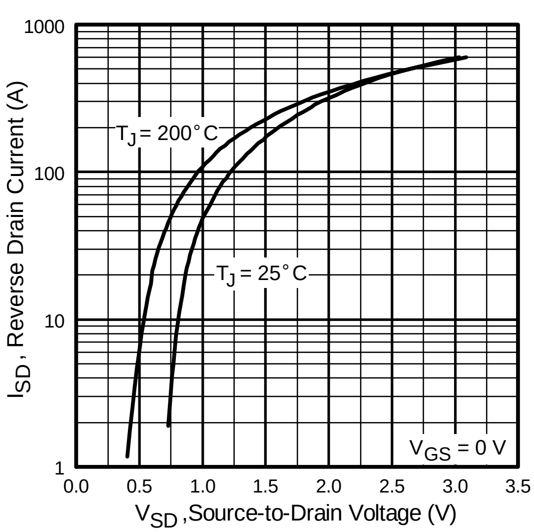


Fig 7. Typical Source-Drain Diode Forward Voltage

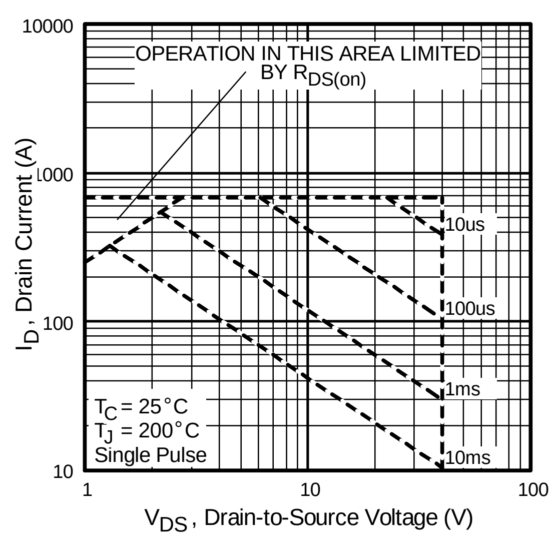


Fig 8. Maximum Safe Operating Area

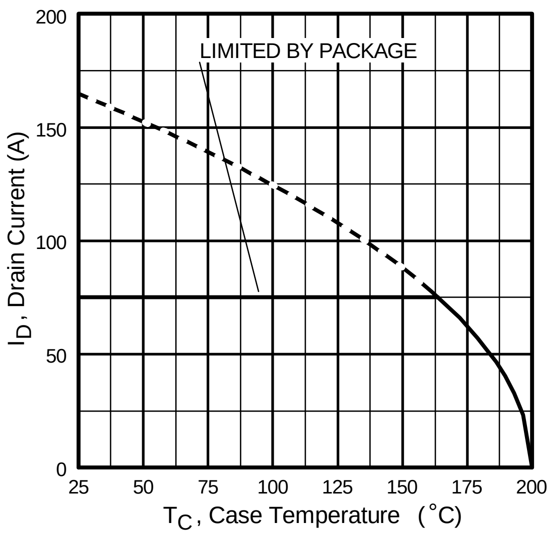
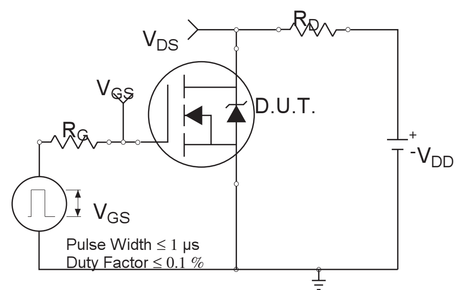
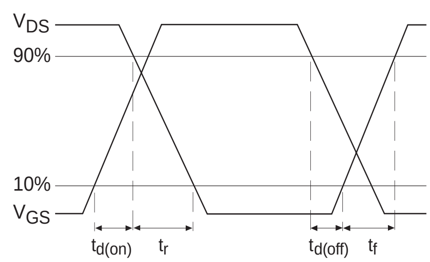


Fig 9. Maximum Drain Current Vs. Case Temperature





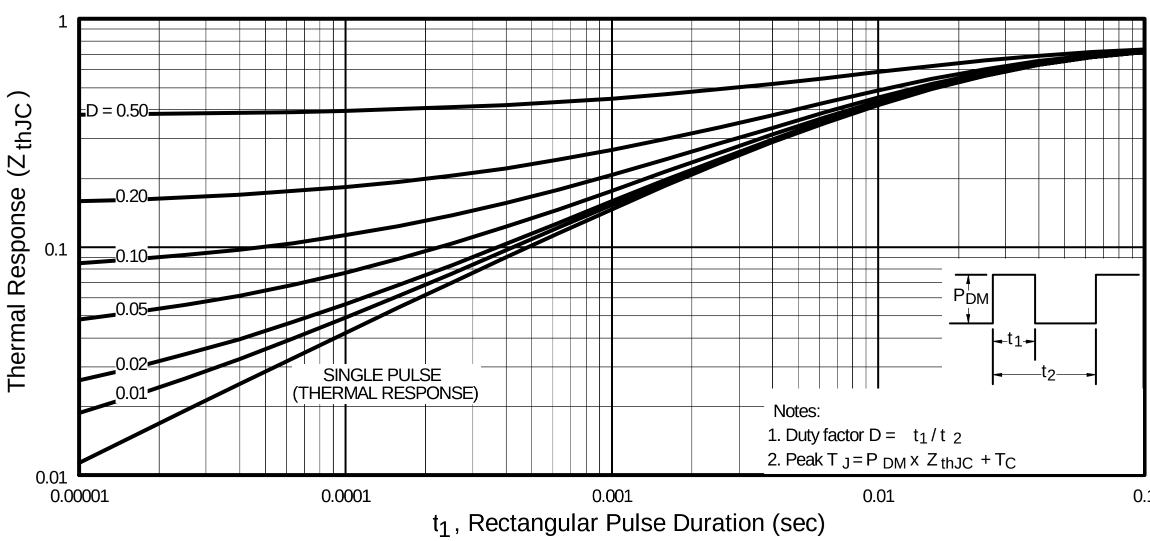


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

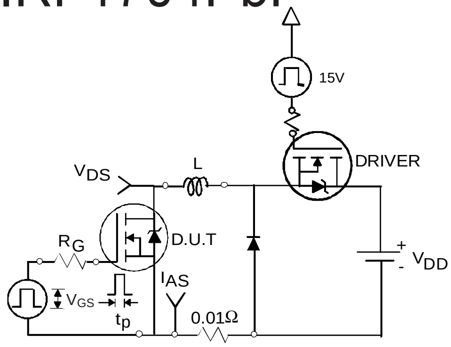


Fig 12a. Unclamped Inductive Test Circuit

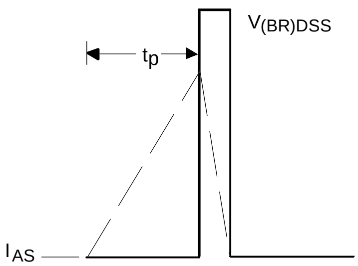


Fig 12b. Unclamped Inductive Waveforms

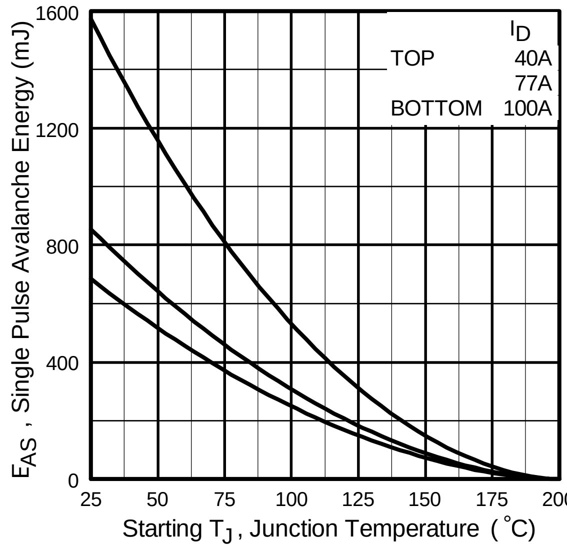


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

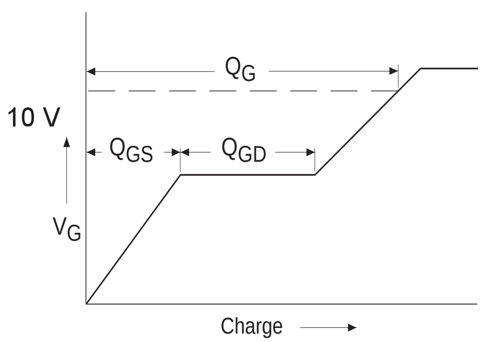


Fig 13a. Basic Gate Charge Waveform

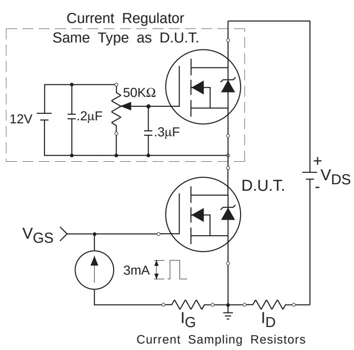


Fig 13b. Gate Charge Test Circuit

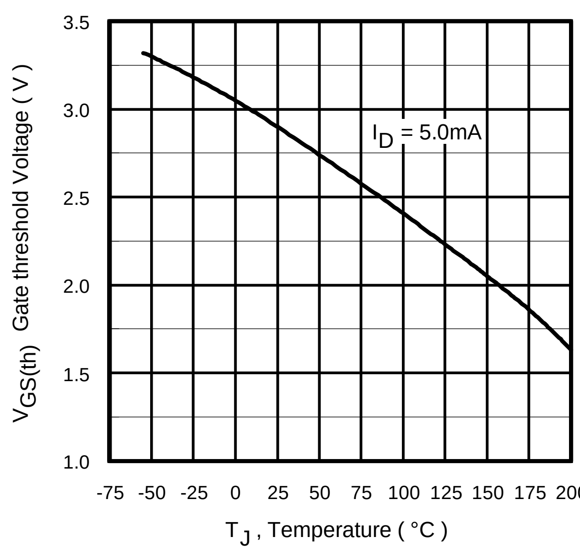
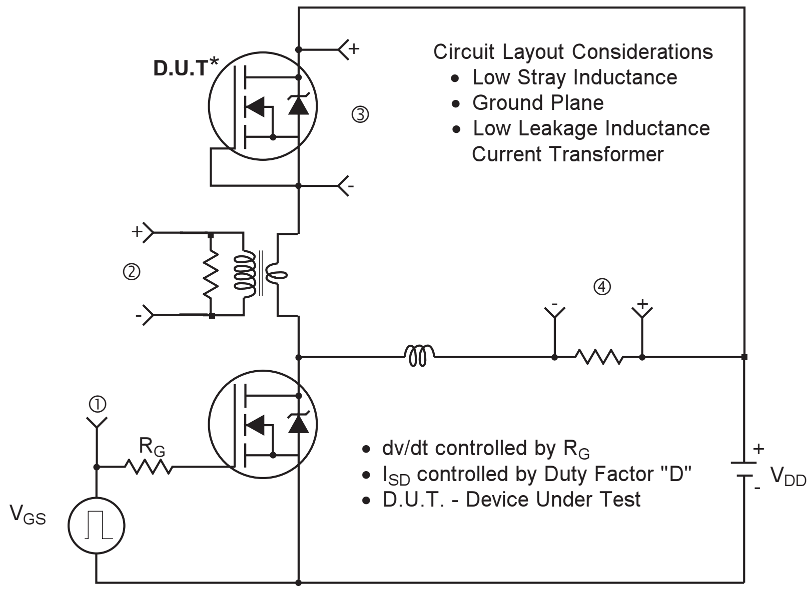
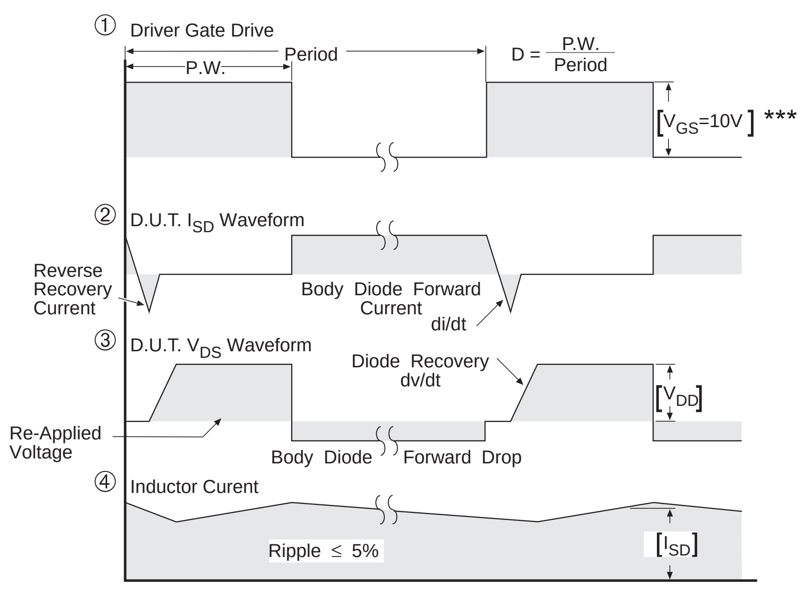


Fig 14. Threshold Voltage Vs Temperature

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel

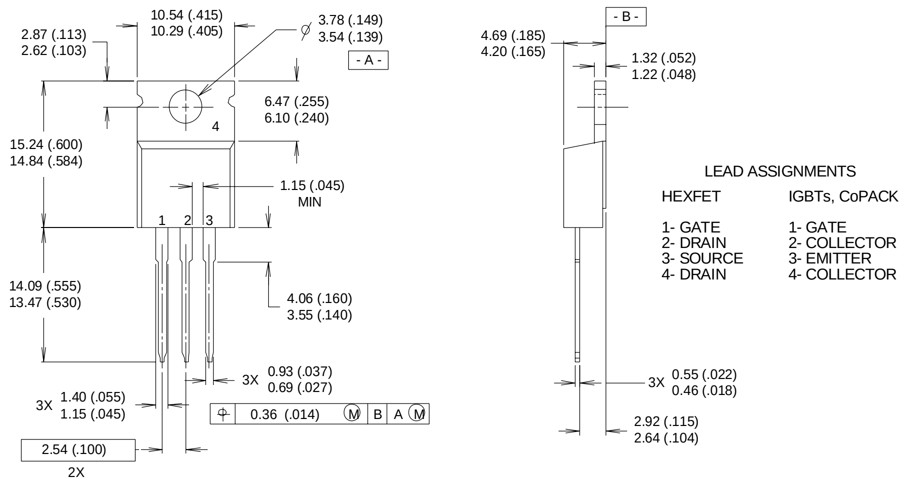


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



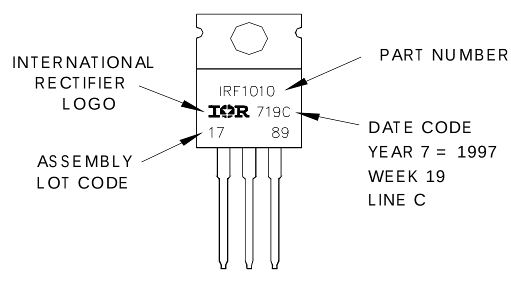
NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101]market.
Qualification Standards can be found on IR's Web site.

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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/