International
IOR Rectifier

END OF LIFE

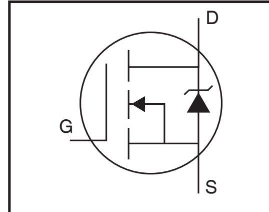
PD - 95407A

IRF1302SPbF

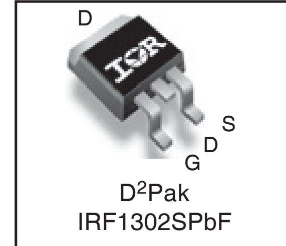
HEXFET® Power MOSFET

Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free



V_{DSS} = 20V
$R_{DS(on)}$ = 4.0mΩ
I_D = 174A⑥



D²Pak
IRF1302SPbF

Description

This Stripe Planar design of HEXFET® Power MOSFET utilizes the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.

G	D	S
Gate	Drain	Source

Ordering Information

Base Part Number	Orderable Part Number	Package Type	Standard Pack		EOL Notice	Replacement Part Number
			Form	Quantity		
IRF1302SPbF	IRF1302SPbF	D2Pak	Tube	50	141B	Please search the EOL part number on IR's website for guidance

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	174⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	120⑥	
I_{DM}	Pulsed Drain Current ①	700	
P_D @T_C = 25°C	Power Dissipation	200	W
	Linear Derating Factor	1.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	350	mJ
I_{AR}	Avalanche Current①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy⑦		mJ
dv/dt	Peak Diode Recovery dv/dt ③	TBD	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case	——	0.75	°C/W
$R_{θJA}$	Junction-to-Ambient (PCB mount)⑧	——	40	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	–––	–––	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.021	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	3.3	4.0	mΩ	V_{GS} = 10V, I_D = 104A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	–––	4.0	V	V_{DS} = 10V, I_D = 250μA
g_{fs}	Forward Transconductance	59	–––	–––	S	V_{DS} = 15V, I_D = 104A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	20	μA	V_{DS} = 20V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 16V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-200		V_{GS} = -20V
Q_g	Total Gate Charge	–––	79	120	nC	I_D = 104A
Q_{gs}	Gate-to-Source Charge	–––	18	27		V_{DS} = 16V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	31	46		V_{GS} = 10V④
$t_{d(on)}$	Turn-On Delay Time	–––	28	–––	ns	V_{DD} = 11V
t_r	Rise Time	–––	130	–––		I_D = 104A
$t_{d(off)}$	Turn-Off Delay Time	–––	47	–––		R_G = 4.5Ω
t_f	Fall Time	–––	16	–––		V_{GS} = 10V ④
L_D	Internal Drain Inductance	–––	4.5	–––	nH	Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance	–––	7.5	–––		from package and center of die contact
C_{iss}	Input Capacitance	–––	3600	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	2370	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	520	–––		ƒ = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	–––	5710	–––		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	–––	2370	–––		V_{GS} = 0V, V_{DS} = 16V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance ⑤	–––	3540	–––		V_{GS} = 0V, V_{DS} = 0V to 16V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	174⑥	A	MOSFET symbol showing the
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	700		integral reverse p-n junction diode.
V_{SD}	Diode Forward Voltage	–––	–––	1.3	V	T_J = 25°C, I_S = 104A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	66	100	ns	T_J = 25°C, I_F = 104A
Q_{rr}	Reverse RecoveryCharge	–––	130	200	nC	di/dt = 100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).

② Starting T_J = 25°C, L = 0.063mH R_G = 25Ω, I_{AS} = 104A. (See Figure 12).

③ I_{SD} ≤ 104A, di/dt ≤ 100A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

⑦ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.

⑧ This is applied to D^2Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

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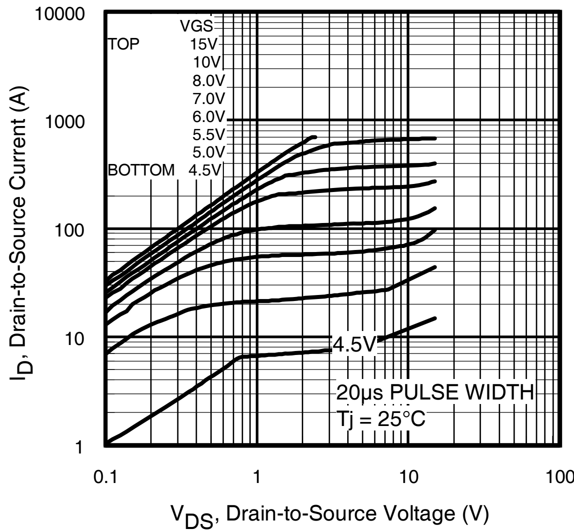

Fig 1. Typical Output Characteristics

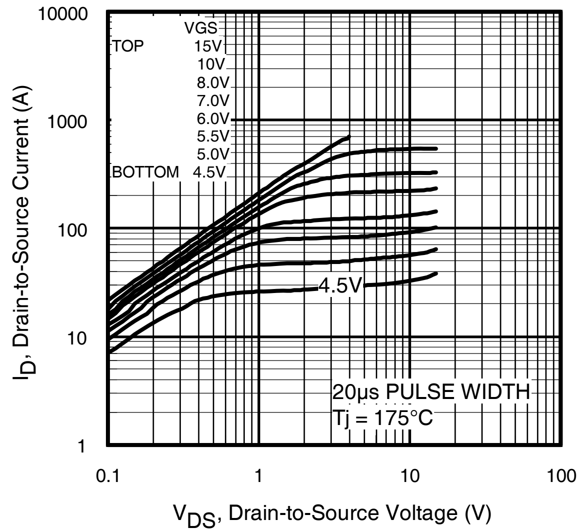

Fig 2. Typical Output Characteristics

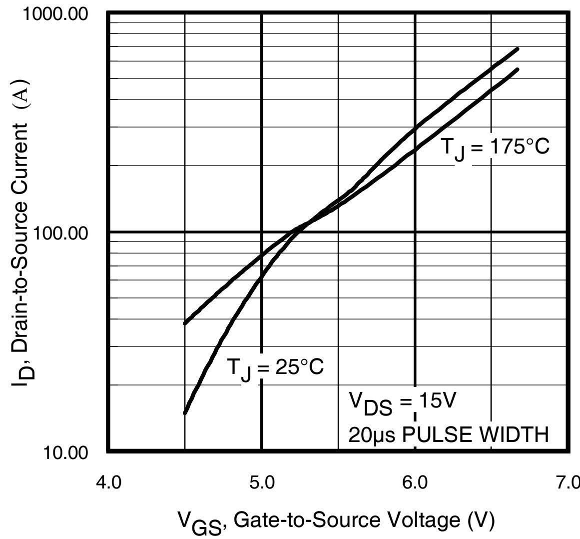

Fig 3. Typical Transfer Characteristics

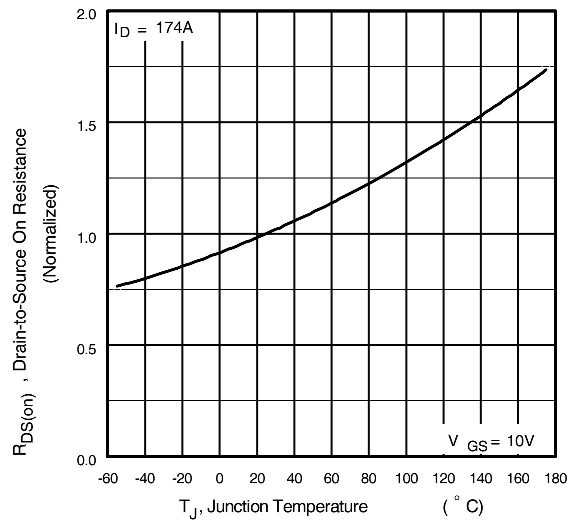

Fig 4. Normalized On-Resistance Vs. Temperature

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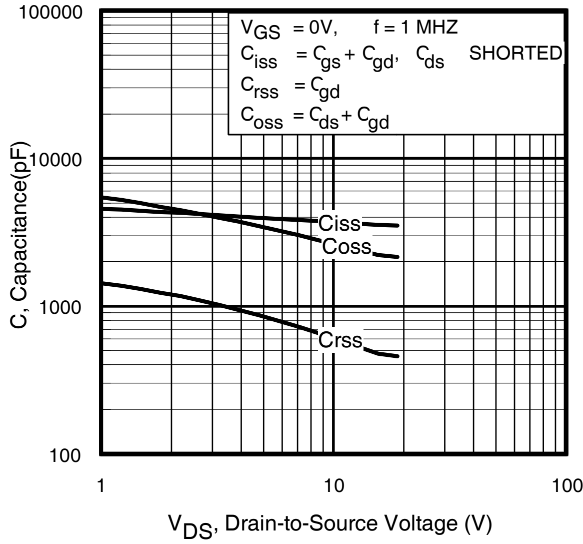

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

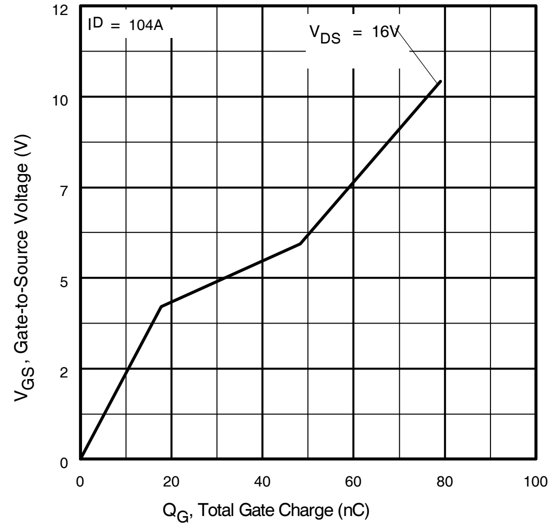

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

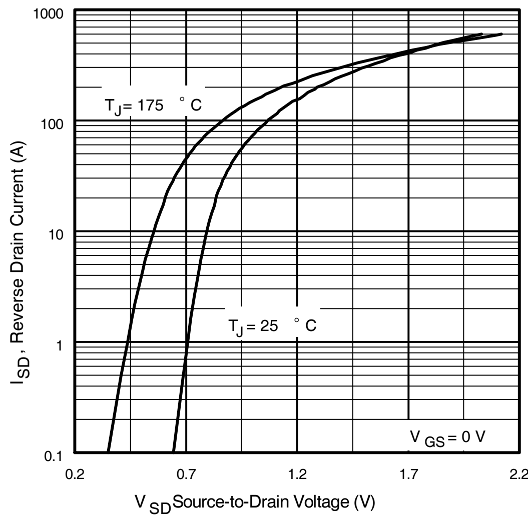

Fig 7. Typical Source-Drain Diode Forward Voltage

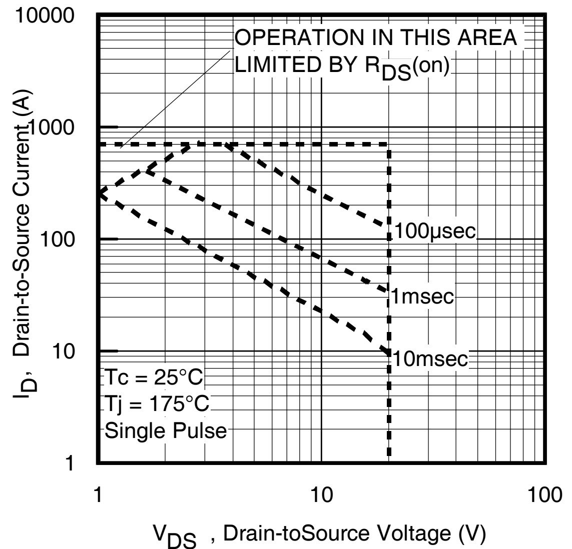

Fig 8. Maximum Safe Operating Area

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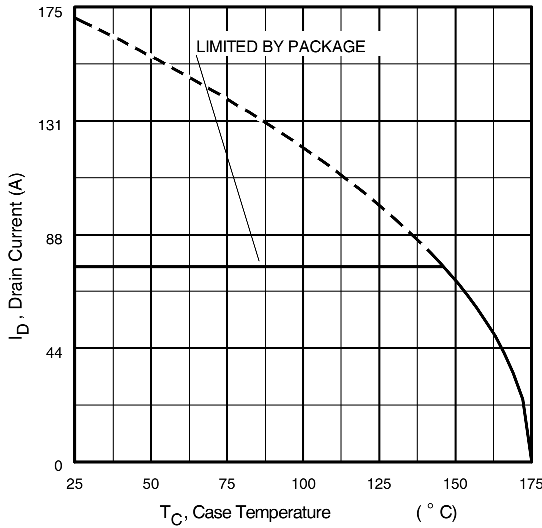

Fig 9. Maximum Drain Current Vs. Case Temperature

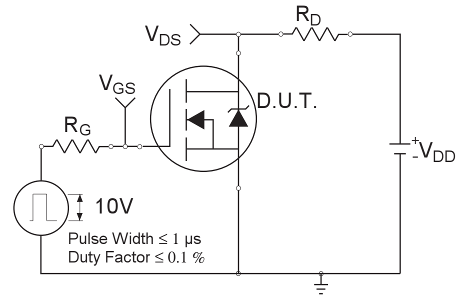

Fig 10a. Switching Time Test Circuit

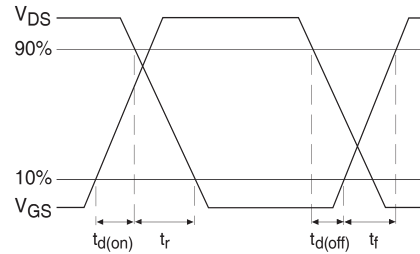

Fig 10b. Switching Time Waveforms

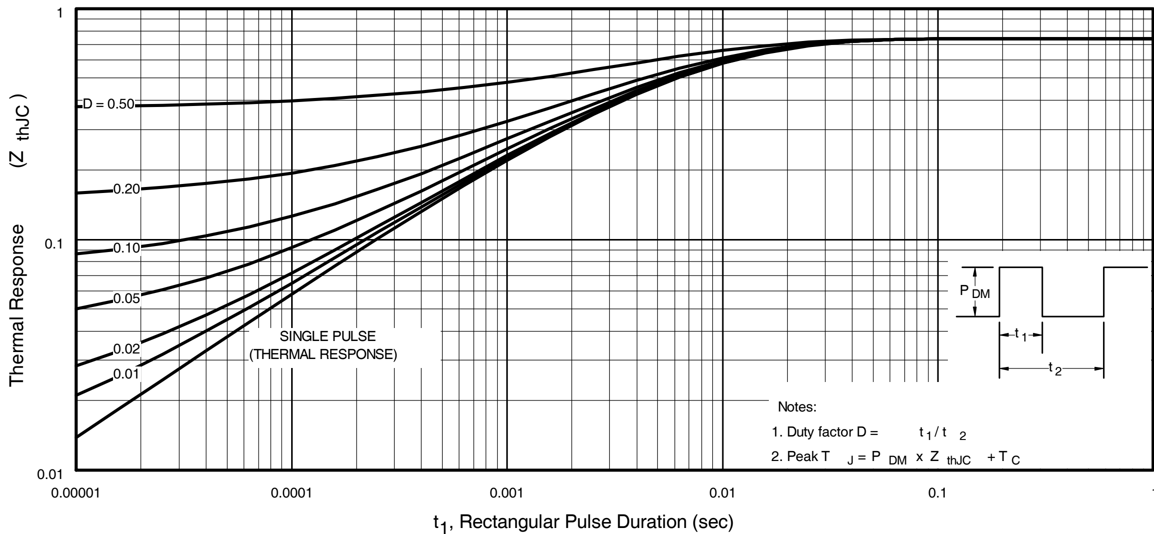

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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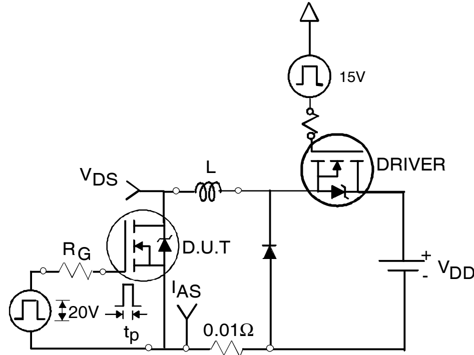

Fig 12a. Unclamped Inductive Test Circuit

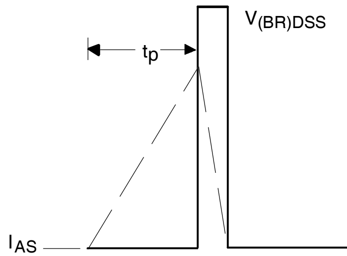

Fig 12b. Unclamped Inductive Waveforms

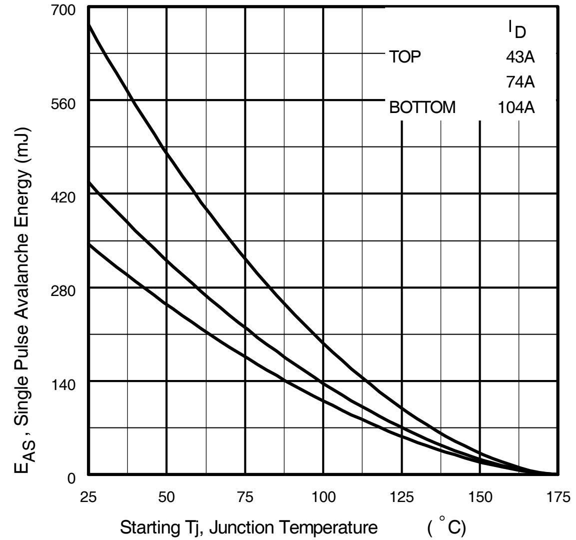

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

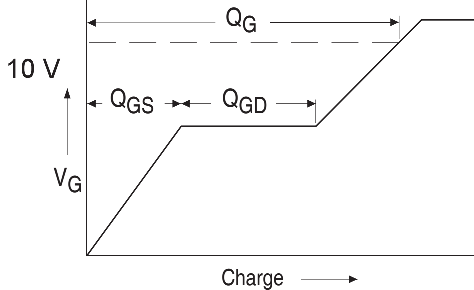

Fig 13a. Basic Gate Charge Waveform

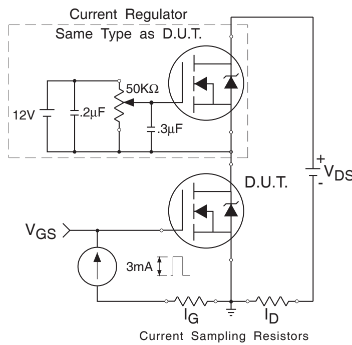

Fig 13b. Gate Charge Test Circuit

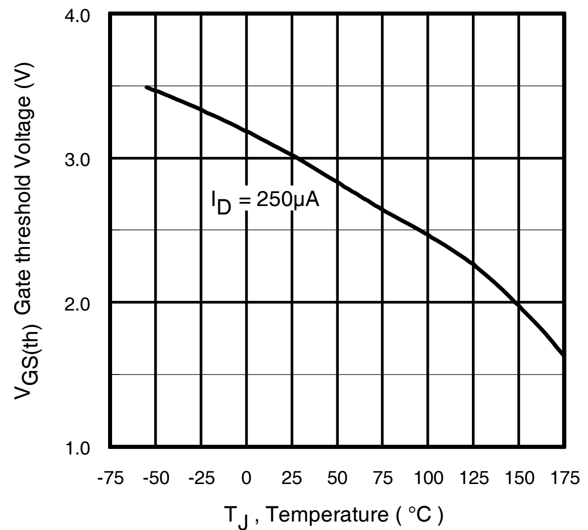

Fig 14. Threshold Voltage Vs. Temperature

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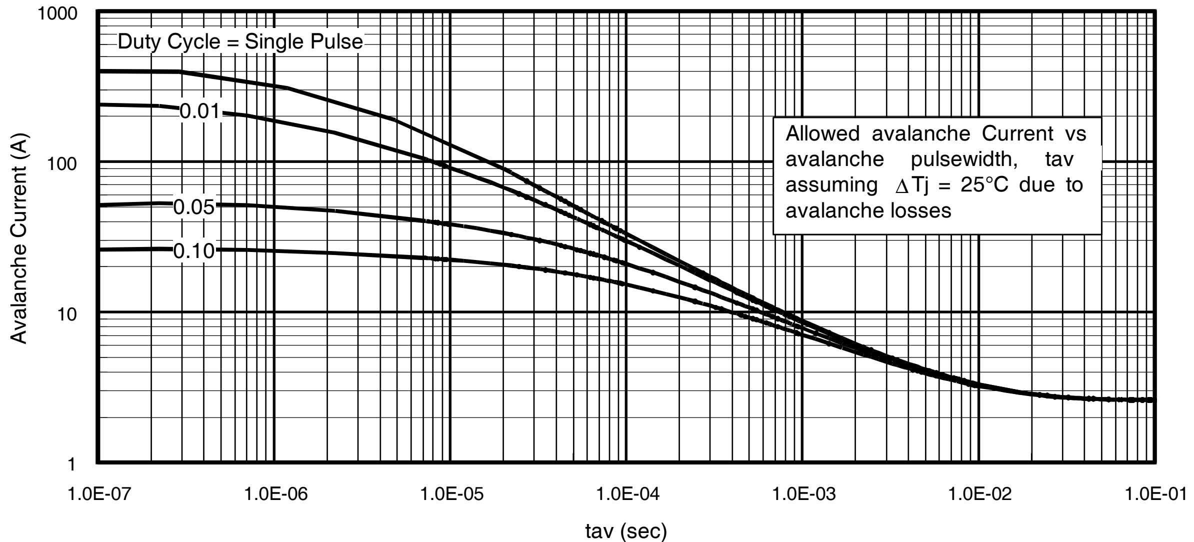

Fig 15. Typical Avalanche Current Vs.Pulsewidth

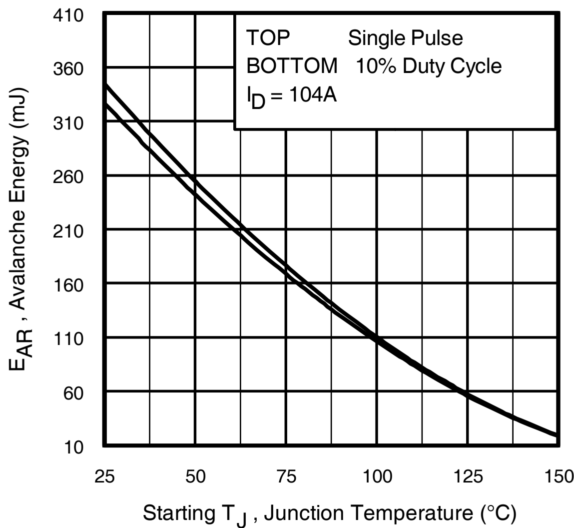

Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

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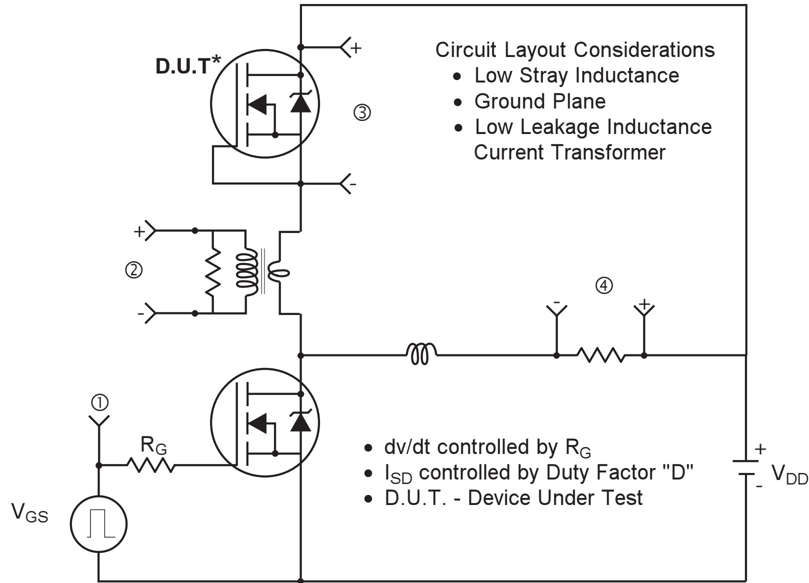
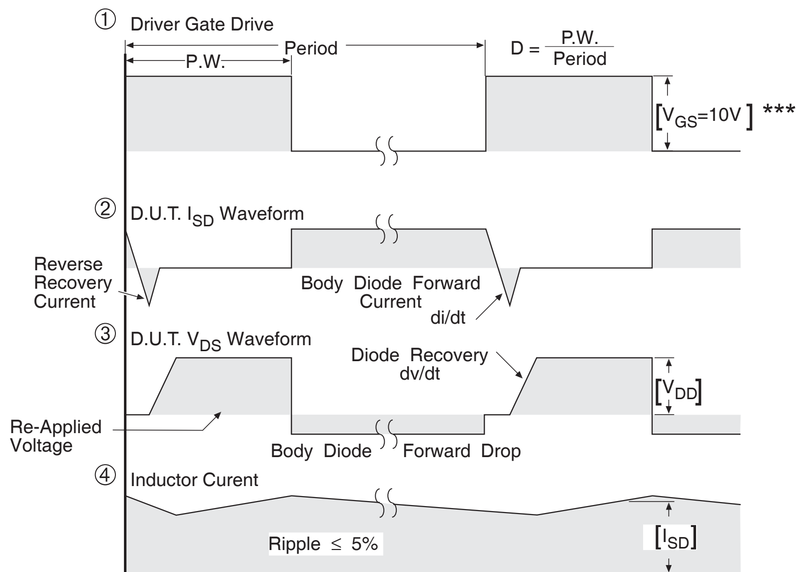
Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 17. For N-channel HEXFET® power MOSFETs

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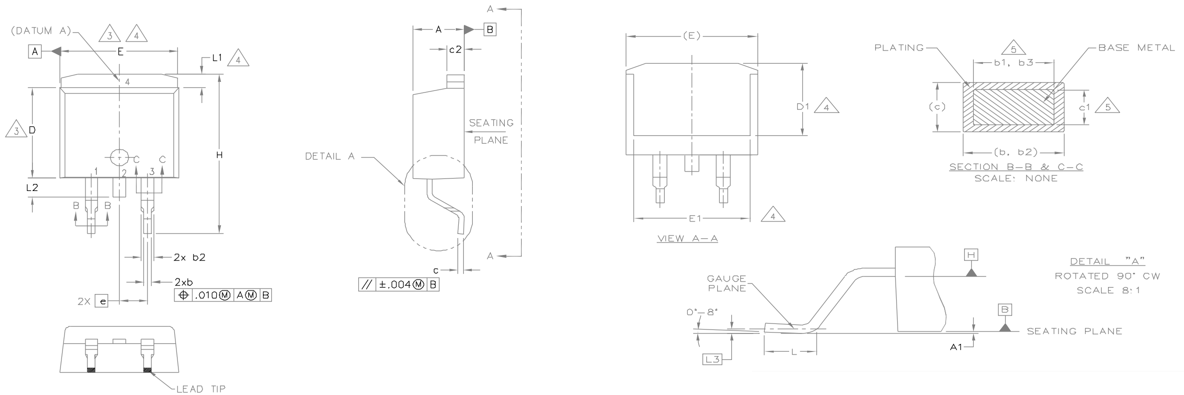
D²Pak Package Outline (Dimensions are shown in millimeters (inches))



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245	–	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. △ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. △ THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. △ DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO–263AB.

LEAD ASSIGNMENTS

DIODES

1.– ANODE (TWO DIE) / OPEN (ONE DIE)
2, 4.– CATHODE
3.– ANODE

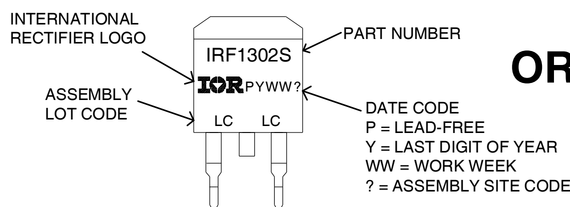
HEXFET

1.– GATE
2, 4.– DRAIN
3.– SOURCE

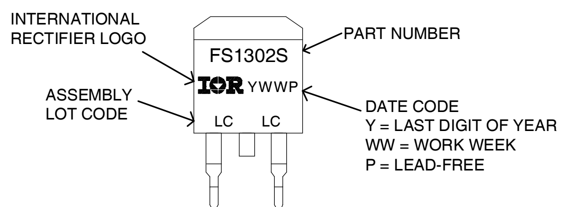
IGBTs, CoPACK

1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

D²Pak Part Marking Information



OR



For the most current drawing please refer to IR website at http://www.irf.com/package/

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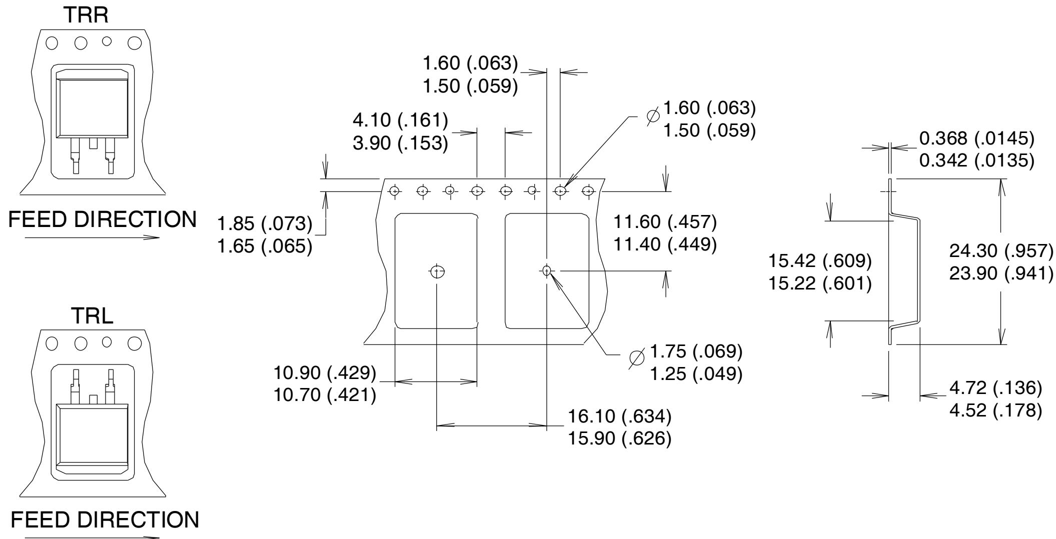
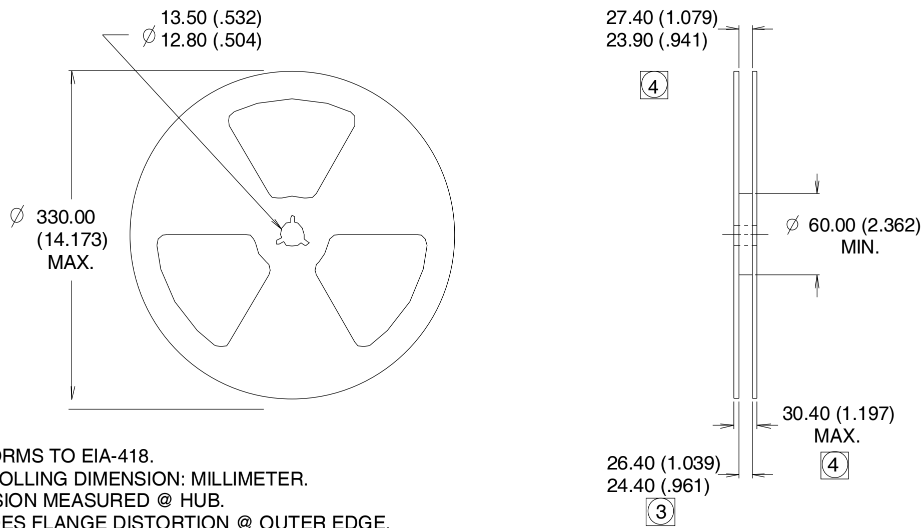
D^2Pak Tape & Reel Information





NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

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Qualification information†

Qualification level	Industrial† (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	D^2Pak	MSL1
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comment
11/12/2014	* Updated data sheet with new IR corporate template * Deleted Device- IRF1302LPBF from page 1 and Package Drg .
2/18/2015	* Added Ordering Information to reflect the End-Of-Life

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IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA
To contact International Rectifier, please visit http://www.irf.com/whoto-call/

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