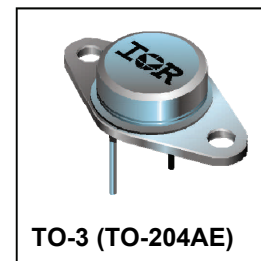


REPETITIVE AVALANCHE AND dv/dt RATED HEXFET[®] TRANSISTORS THRU-HOLE -TO-3 (TO-204AE)

60V, N-CHANNEL

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D
IRF044	60V	0.028 Ω	44A



Description

HEXFET[®] MOSFET technology is the key to IR HiRel advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest “State of the Art” design achieves: very low on-state resistance combined with high trans conductance; superior reverse energy and diode recovery dv/dt capability.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

Features

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Hermetically Sealed
- Simple Drive Requirements

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{D1} @ $V_{GS} = 10V$, $T_C = 25^\circ C$	Continuous Drain Current	44	A
I_{D2} @ $V_{GS} = 10V$, $T_C = 100^\circ C$	Continuous Drain Current	27	
I_{DM} @ $T_C = 25^\circ C$	Pulsed Drain Current ①	176	
P_D @ $T_C = 25^\circ C$	Maximum Power Dissipation	125	W
	Linear Derating Factor	1.0	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	340	mJ
I_{AR}	Avalanche Current ①	44	A
E_{AR}	Repetitive Avalanche Energy ①	12.5	mJ
dv/dt	Peak Diode Recovery ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	$^\circ C$
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	11.5 (Typical)	

For footnotes refer to the page 2.

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 1.0mA$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.68	—	V/°C	Reference to 25°C, $I_D = 1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.028	Ω	$V_{GS} = 10V, I_{D2} = 27A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	$V_{DS} = 48V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 48V, V_{GS} = 0V, T_J = 125^\circ C$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
Q_G	Total Gate Charge	39	—	88	nC	$I_{D1} = 44A$
Q_{GS}	Gate-to-Source Charge	6.7	—	15		$V_{DS} = 30V$
Q_{GD}	Gate-to-Drain ('Miller') Charge	18	—	52		$V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	—	23	ns	$V_{DD} = 30V$
t_r	Rise Time	—	—	130		$I_{D1} = 44A$
$t_{d(off)}$	Turn-Off Delay Time	—	—	81		$R_G = 9.1\Omega$
t_f	Fall Time	—	—	79		$V_{GS} = 10V$
$L_S + L_D$	Total Inductance	—	6.1	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm / 0.25 in from package)
C_{iss}	Input Capacitance	—	2400	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1100	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	230	—		$f = 1.0MHz$

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	44	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	176		
V_{SD}	Diode Forward Voltage	—	—	2.5	V	$T_J = 25^\circ C, I_S = 44A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	—	220	ns	$T_J = 25^\circ C, I_F = 44A, V_{DD} \leq 50V$
Q_{rr}	Reverse Recovery Charge	—	—	1.6	μC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	30	

Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ C$, $L = 0.35mH$, Peak $I_L = 44A$, $V_{GS} = 10V$.
- ③ $I_{SD} \leq 44A$, $di/dt \leq 250A/\mu s$, $V_{DD} \leq 60V$, $T_J \leq 150^\circ C$. Suggested $R_G = 9.1\Omega$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

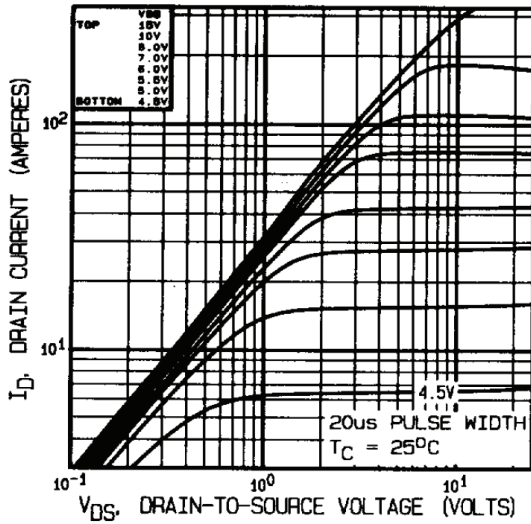


Fig 1. Typical Output Characteristics

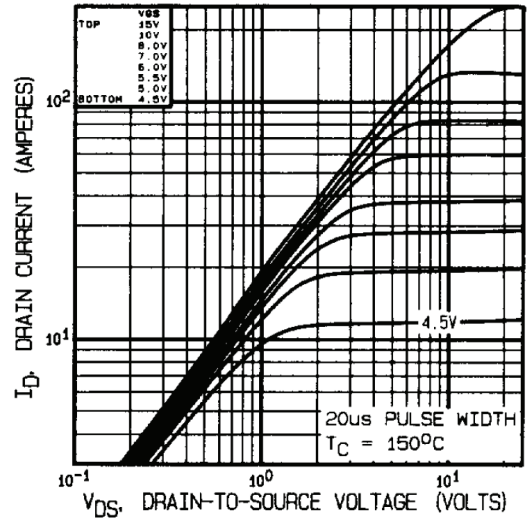


Fig 2. Typical Output Characteristics

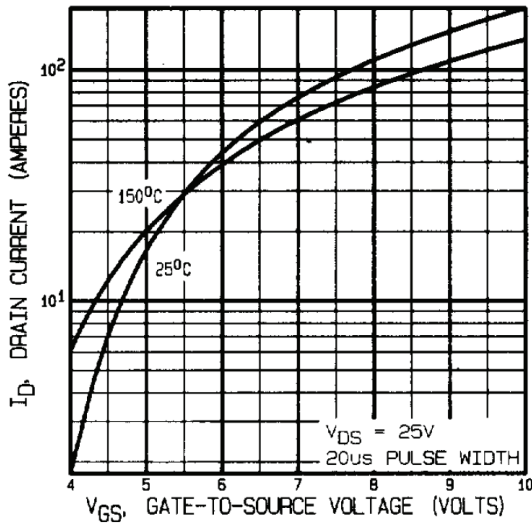


Fig 3. Typical Transfer Characteristics

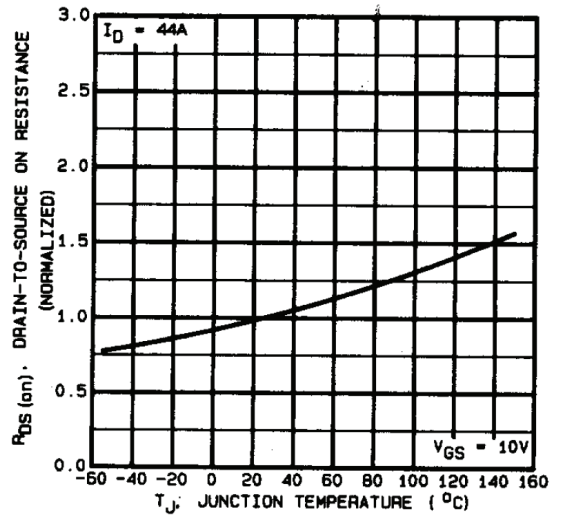


Fig 4. Normalized On-Resistance Vs. Temperature

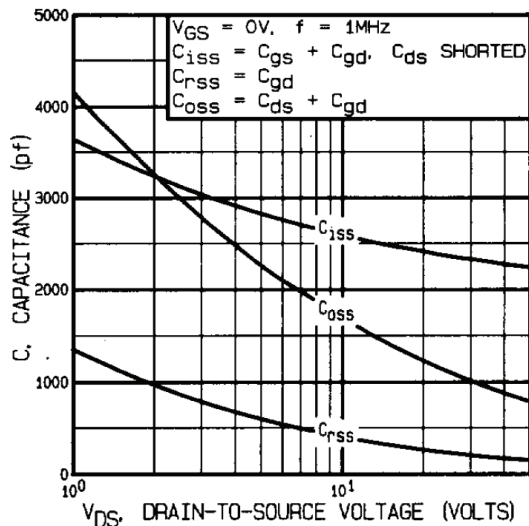


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

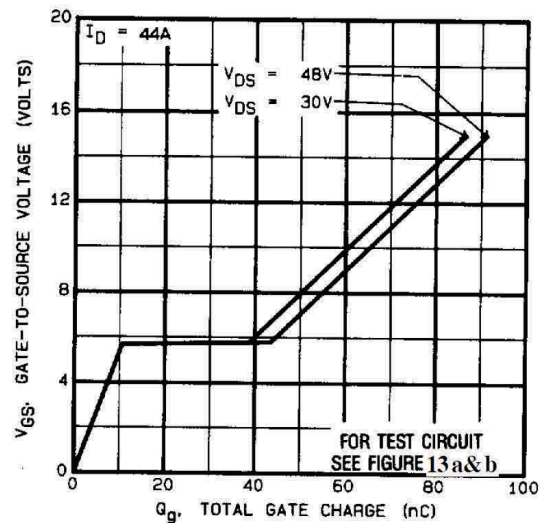


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

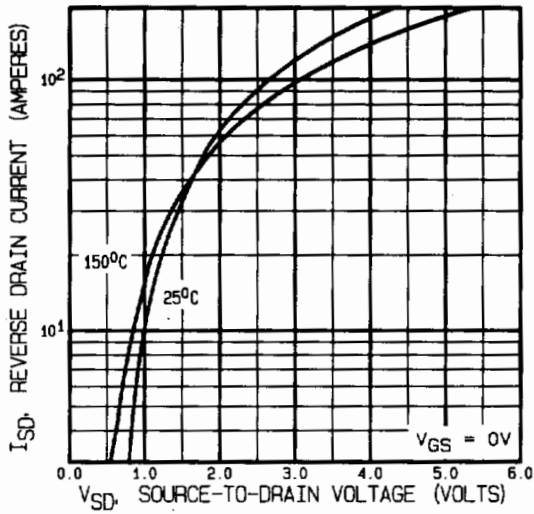


Fig 7. Typical Source-Drain Diode Forward Voltage

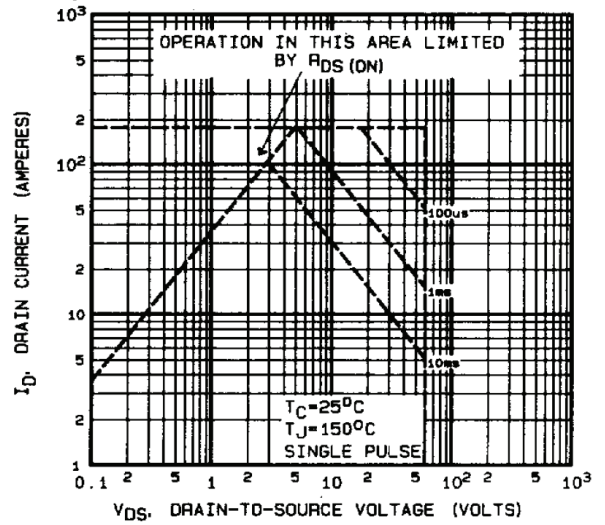


Fig 8. Maximum Safe Operating Area

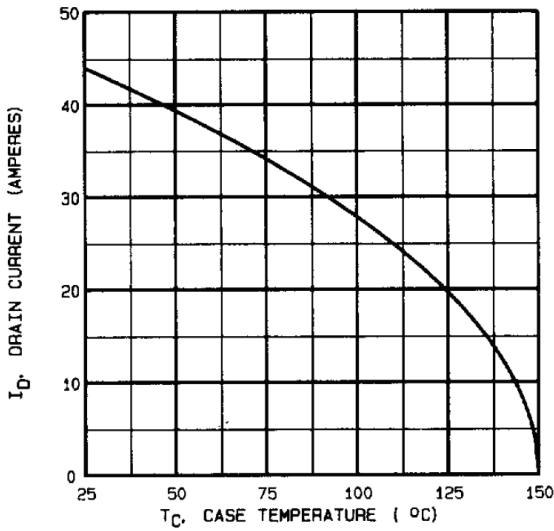


Fig 9. Maximum Drain Current Vs. Case Temperature

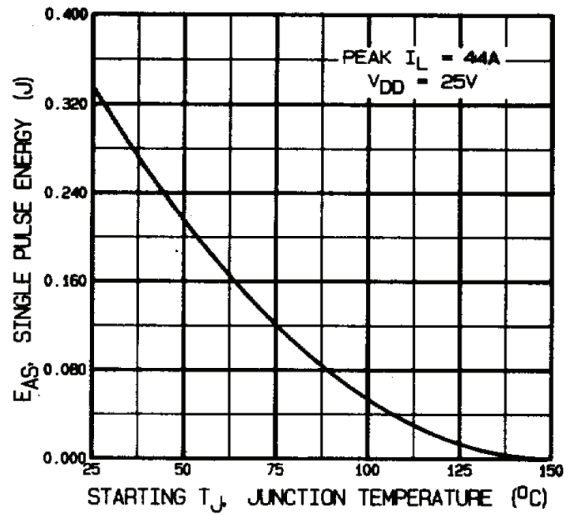


Fig 10. Maximum Avalanche Energy Vs. Drain Current

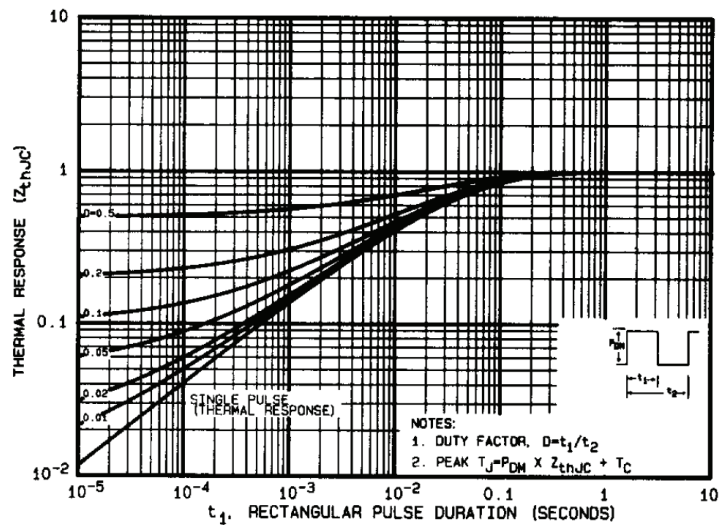


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

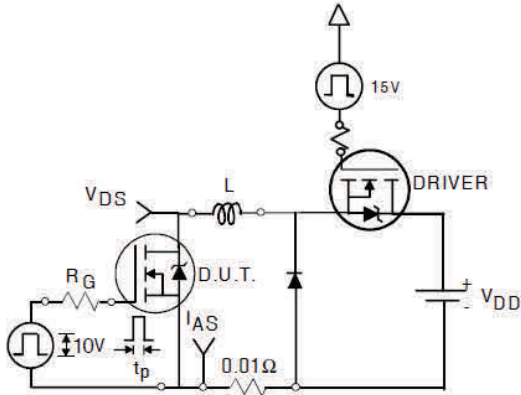


Fig 12a. Unclamped Inductive Test Circuit

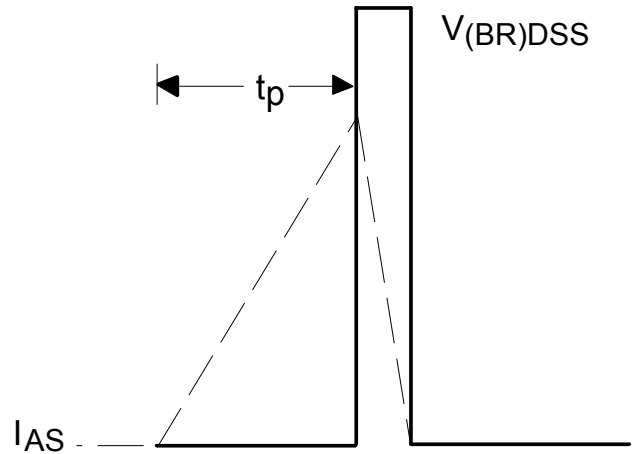


Fig 12b. Unclamped Inductive Waveforms

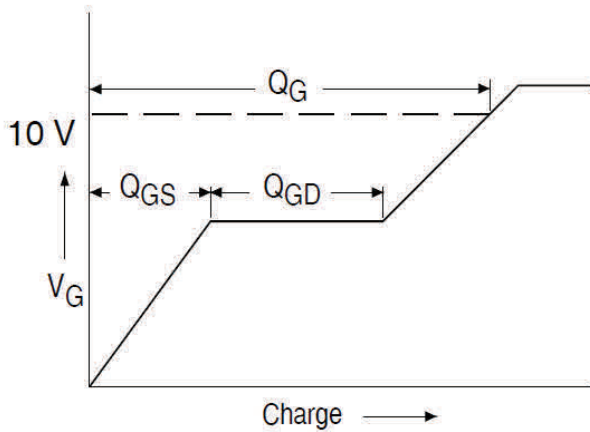


Fig 13a. Gate Charge Waveform

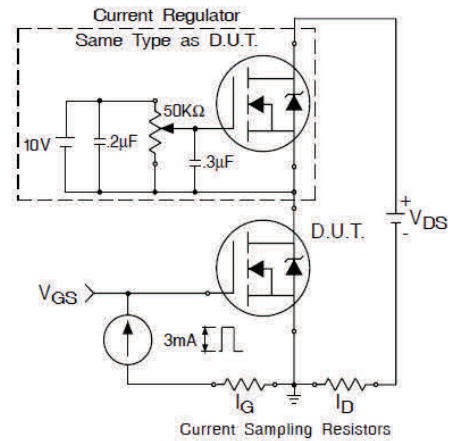


Fig 13b. Gate Charge Test Circuit

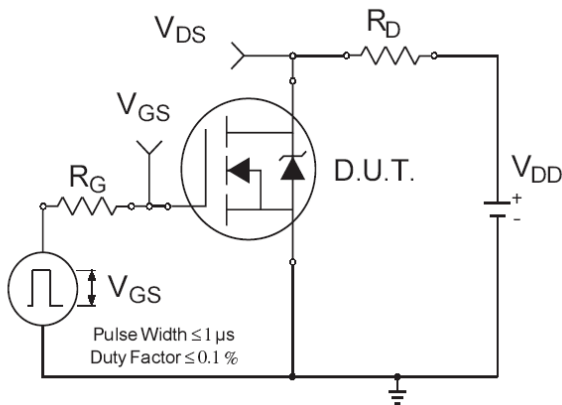


Fig 14a. Switching Time Test Circuit

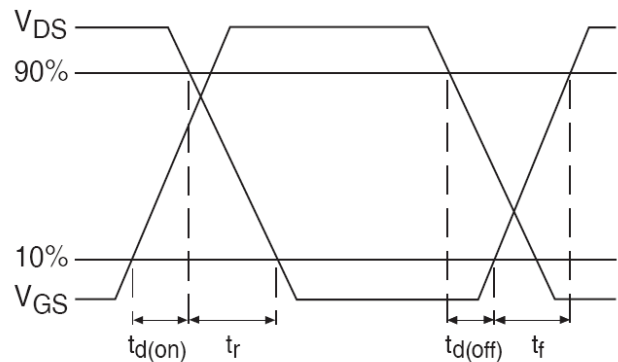
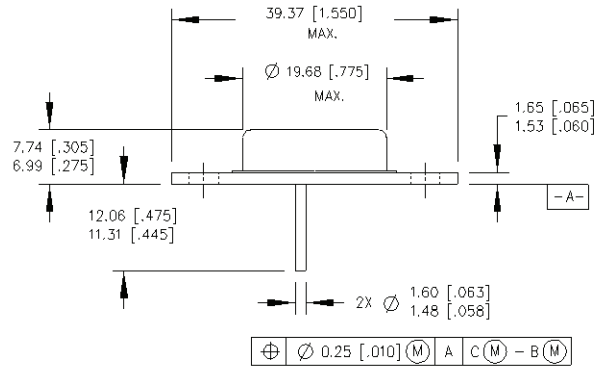


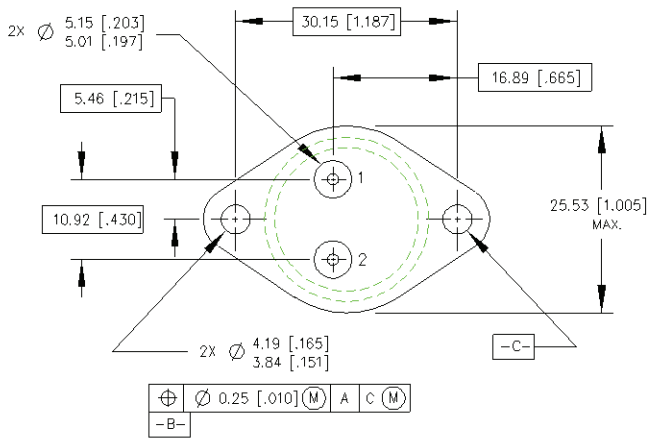
Fig 14b. Switching Time Waveforms

Case Outline and Dimensions - TO-204AE (Modified TO-3)



PIN ASSIGNMENTS

HEXFET	SCHOTTKY	IGBT
1 - SOURCE	1 - ANODE 1	1 - GATE
2 - GATE	2 - ANODE 2	2 - EMITTER
3 - DRAIN (CASE)	3 - COMMON CATHOD (CASE)	3 - COLLECTOR (CASE)



- NOTES:
 1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M -1982.
 2. CONTROLLING DIMENSION : INCH.
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE TO -204-AE.

IMPORTANT NOTICE

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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