Features
- Floating channel designed for bootstrap operation
  - Fully operational to +400V
  - Tolerant to negative transient voltage
  - dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V
  - Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Description
The IR2110L4 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 400 volts.

Absolute Maximum Ratings
Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_B</td>
<td>High Side Floating Supply Voltage</td>
<td>-0.5</td>
<td>V_S + 20</td>
<td>V</td>
</tr>
<tr>
<td>V_S</td>
<td>High Side Floating Supply Offset Voltage</td>
<td>—</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td>V_HO</td>
<td>High Side Floating Output Voltage</td>
<td>V_S - 0.5</td>
<td>V_B + 0.5</td>
<td></td>
</tr>
<tr>
<td>V_CC</td>
<td>Low Side Fixed Supply Voltage</td>
<td>-0.5</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>V_LO</td>
<td>Low Side Output Voltage</td>
<td>-0.5</td>
<td>V_CC + 0.5</td>
<td></td>
</tr>
<tr>
<td>V_DD</td>
<td>Logic Supply Voltage</td>
<td>-0.5</td>
<td>V_SS + 20</td>
<td></td>
</tr>
<tr>
<td>V_SS</td>
<td>Logic Supply Offset Voltage</td>
<td>V_CC - 20</td>
<td>V_CC + 0.5</td>
<td></td>
</tr>
<tr>
<td>V_IN</td>
<td>Logic Input Voltage (HIN, LIN &amp; SD)</td>
<td>Vss - 0.5</td>
<td>Vdd + 0.5</td>
<td></td>
</tr>
<tr>
<td>dV/dt</td>
<td>Allowable Offset Supply Voltage Transient</td>
<td>—</td>
<td>50</td>
<td>V/ns</td>
</tr>
<tr>
<td>P_D</td>
<td>Package Power Dissipation @ T_AEL +25°C</td>
<td>—</td>
<td>1.6</td>
<td>W</td>
</tr>
<tr>
<td>R_INJA</td>
<td>Thermal Resistance, Junction to Ambient</td>
<td>—</td>
<td>75</td>
<td>°C/W</td>
</tr>
<tr>
<td>T_J</td>
<td>Junction Temperature</td>
<td>-55</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>T_S</td>
<td>Storage Temperature</td>
<td>-55</td>
<td>150</td>
<td></td>
</tr>
<tr>
<td>T_L</td>
<td>Lead Temperature (Soldering, 10 seconds)</td>
<td>—</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>Weight</td>
<td></td>
<td>1.5</td>
<td>(typical)</td>
<td>g</td>
</tr>
</tbody>
</table>
IR2110L4

Recommended Operating Conditions
The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The VS and VSS offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Figures 36 and 37.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VB</td>
<td>High Side Floating Supply Absolute Voltage</td>
<td>VS + 10</td>
<td>VS + 20</td>
<td>V</td>
</tr>
<tr>
<td>VS</td>
<td>High Side Floating Supply Offset Voltage</td>
<td>-4</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td>VHO</td>
<td>High Side Floating Output Voltage</td>
<td>VS</td>
<td>VB</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>Low Side Fixed Supply Voltage</td>
<td>10</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>VLO</td>
<td>Low Side Output Voltage</td>
<td>0</td>
<td>VCC</td>
<td></td>
</tr>
<tr>
<td>VDD</td>
<td>Logic Supply Voltage</td>
<td>VSS + 5</td>
<td>VSS + 20</td>
<td></td>
</tr>
<tr>
<td>VSS</td>
<td>Logic Supply Offset Voltage</td>
<td>-5</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>VIN</td>
<td>Logic Input Voltage (HIN, LIN &amp; SD)</td>
<td>VSS</td>
<td>VDD</td>
<td></td>
</tr>
</tbody>
</table>

Dynamic Electrical Characteristics
VBIAS (VCC, VBS, VDD) = 15V, and VSS = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>ton</td>
<td>Turn-On Propagation Delay</td>
<td>—</td>
<td>120</td>
<td>150</td>
<td>ns</td>
<td>Vs = 0V</td>
</tr>
<tr>
<td>toff</td>
<td>Turn-Off Propagation Delay</td>
<td>—</td>
<td>94</td>
<td>125</td>
<td>—</td>
<td>Vs = 400V</td>
</tr>
<tr>
<td>tsd</td>
<td>Shutdown Propagation Delay</td>
<td>—</td>
<td>110</td>
<td>140</td>
<td>—</td>
<td>Vs = 400V</td>
</tr>
<tr>
<td>tr</td>
<td>Turn-On Rise Time</td>
<td>—</td>
<td>25</td>
<td>35</td>
<td>—</td>
<td>Cl = 1000pf</td>
</tr>
<tr>
<td>tf</td>
<td>Turn-Off Fall Time</td>
<td>—</td>
<td>17</td>
<td>25</td>
<td>—</td>
<td>Cl = 1000pf</td>
</tr>
<tr>
<td>MT</td>
<td>Delay Matching, HS &amp; LS Turn-On/Off</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

Typical Connection

[Diagram of typical connection]
## Static Electrical Characteristics

VB\textsubscript{BIAS} (V\textsubscript{CC}, V\textsubscript{BS}, V\textsubscript{DD}) = 15V, T\textsubscript{A} = 25°C and V\textsubscript{SS} = COM unless otherwise specified. The V\textsubscript{IN}, V\textsubscript{TH} and I\textsubscript{IN} parameters are referenced to V\textsubscript{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V\textsubscript{O} and I\textsubscript{O} parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ.</th>
<th>Max.</th>
<th>Min.</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\textsubscript{IH}</td>
<td>Logic “1” Input Voltage</td>
<td>9.5</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>V\textsubscript{DD} = 15V</td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{IL}</td>
<td>Logic “0” Input Voltage</td>
<td>—</td>
<td>—</td>
<td>6.0</td>
<td>—</td>
<td>5.7</td>
<td>V\textsubscript{DD} = 15V</td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{OH}</td>
<td>High Level Output Voltage, V\textsubscript{BIAS} - V\textsubscript{O}</td>
<td>—</td>
<td>0.7</td>
<td>1.2</td>
<td>—</td>
<td>1.5</td>
<td>V\textsubscript{IN} = V\textsubscript{IH}, IO = 0A</td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{OL}</td>
<td>Low Level Output Voltage, VO</td>
<td>—</td>
<td>—</td>
<td>0.1</td>
<td>—</td>
<td>0.1</td>
<td>V\textsubscript{IN} = V\textsubscript{IL}, IO = 0A</td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{ILK}</td>
<td>Offset Supply Leakage Current</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>250</td>
<td>V\textsubscript{B} = V\textsubscript{S} = 400V</td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{QBS}</td>
<td>Quiescent V\textsubscript{BS} Supply Current</td>
<td>—</td>
<td>125</td>
<td>230</td>
<td>—</td>
<td>500</td>
<td>V\textsubscript{IN} = V\textsubscript{IH} or V\textsubscript{IL}</td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{QCC}</td>
<td>Quiescent V\textsubscript{CC} Supply Current</td>
<td>—</td>
<td>180</td>
<td>340</td>
<td>—</td>
<td>600</td>
<td>V\textsubscript{IN} = V\textsubscript{IH} or V\textsubscript{IL}</td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{QDD}</td>
<td>Quiescent V\textsubscript{DD} Supply Current</td>
<td>—</td>
<td>5</td>
<td>30</td>
<td>—</td>
<td>60</td>
<td>V\textsubscript{IN} = V\textsubscript{IH} or V\textsubscript{IL}</td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{IN+}</td>
<td>Logic “1” Input Bias Current</td>
<td>—</td>
<td>15</td>
<td>40</td>
<td>—</td>
<td>70</td>
<td>V\textsubscript{IN} = 15V</td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{IN-}</td>
<td>Logic “0” Input Bias Current</td>
<td>—</td>
<td>—</td>
<td>1.0</td>
<td>—</td>
<td>10</td>
<td>V\textsubscript{IN} = 0V</td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{BSUV+}</td>
<td>V\textsubscript{BS} Supply Undervoltage Positive Going Threshold</td>
<td>7.5</td>
<td>8.6</td>
<td>9.7</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{BSUV-}</td>
<td>V\textsubscript{BS} Supply Undervoltage Negative Going Threshold</td>
<td>7.0</td>
<td>8.2</td>
<td>9.4</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{CCUV+}</td>
<td>V\textsubscript{CC} Supply Undervoltage Positive Going Threshold</td>
<td>7.4</td>
<td>8.5</td>
<td>9.6</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>V\textsubscript{CCUV-}</td>
<td>V\textsubscript{CC} Supply Undervoltage Negative Going Threshold</td>
<td>7.0</td>
<td>8.2</td>
<td>9.4</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{O+}</td>
<td>Output High Short Circuit Pulsed Current</td>
<td>2.0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{O-}</td>
<td>Output Low Short Circuit Pulsed Current</td>
<td>2.0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>A</td>
<td></td>
</tr>
</tbody>
</table>

V\textsubscript{O} = 0V, V\textsubscript{IN} = V\textsubscript{DD}, PW < = 10\textmu S

V\textsubscript{O} = 15V, V\textsubscript{IN} = 0V, PW < = 10\textmu S
Figure 1. Input/Output Timing Diagram

Figure 2. Floating Supply Voltage Transient Test Circuit

Figure 3. Switching Time Test Circuit

Figure 4. Switching Time Waveform Definition

Figure 5. Shutdown Waveform Definitions

Figure 6. Delay Matching Waveform Definitions
Figure 10A. Turn-On Rise Time vs. Temperature

Figure 10B. Turn-On Rise Time vs. Voltage

Figure 11A. Turn-Off Fall Time vs. Temperature

Figure 11B. Turn-Off Fall Time vs. Voltage

Figure 12A. Logic “1” Input Threshold vs. Temperature

Figure 12B. Logic “1” Input Threshold vs. Voltage
Figure 16A. Offset Supply Current vs. Temperature

Figure 16B. Offset Supply Current vs. Voltage

Figure 17A. V_{BS} Supply Current vs. Temperature

Figure 17B. V_{BS} Supply Current vs. Voltage

Figure 18A. V_{CC} Supply Current vs. Temperature

Figure 18B. V_{CC} Supply Current vs. Voltage
IR2110L4

Figure 22. $V_{BS}$ Undervoltage (+) vs. Temperature

Figure 23. $V_{BS}$ Undervoltage (-) vs. Temperature

Figure 24. $V_{CC}$ Undervoltage (+) vs. Temperature

Figure 25. $V_{CC}$ Undervoltage (-) vs. Temperature

Figure 26A. Output Source Current vs. Temperature

Figure 26B. Output Source Current vs. Voltage
Functional Block Diagram

Lead Definitions

<table>
<thead>
<tr>
<th>Lead Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Logic supply</td>
</tr>
<tr>
<td>HIN</td>
<td>Logic input for high side gate driver output (HO), in phase</td>
</tr>
<tr>
<td>SD</td>
<td>Logic input for shutdown</td>
</tr>
<tr>
<td>LIN</td>
<td>Logic input for low side gate driver output (LO), in phase</td>
</tr>
<tr>
<td>VSS</td>
<td>Logic ground</td>
</tr>
<tr>
<td>VB</td>
<td>High side floating supply</td>
</tr>
<tr>
<td>HO</td>
<td>High side gate drive output</td>
</tr>
<tr>
<td>Vs</td>
<td>High side floating supply return</td>
</tr>
<tr>
<td>VCC</td>
<td>Low side supply</td>
</tr>
<tr>
<td>LO</td>
<td>Low side gate drive output</td>
</tr>
<tr>
<td>COM</td>
<td>Low side return</td>
</tr>
</tbody>
</table>
IR2110L4
Case Outline and Dimensions — MO-036AB

NOTES:
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MO-036AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.